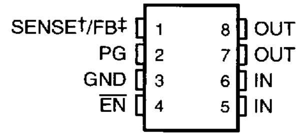
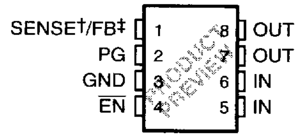
- **Available in 5-V, 4.85-V, and 3.3-V Fixed-Output and Adjustable Versions**
- **Dropout Voltage <85 mV Max at I_O = 100 mA (TPS7250)**
- **Low Quiescent Current, Independent of Load, 155 μA Typ**
- **8-Pin SOIC and 8-Pin TSSOP Package (Product Preview)**
- **Output Regulated to ±2% Over Full Operating Range for Fixed-Output Versions**
- **Extremely Low Sleep-State Current, 0.5 μA Max**
- **Power-Good (PG) Status Output**

D PACKAGE (TOP VIEW)



PW PACKAGE (TOP VIEW)



† SENSE – Fixed voltage options only (TPS7233, TPS7248, and TPS7250)
‡ FB – Adjustable version only (TPS7201)

description

The TPS72xx family of low-dropout (LDO) voltage regulators offers the benefits of low-dropout voltage, micropower operation and miniaturized packaging. These regulators feature extremely low dropout voltages and quiescent currents compared to conventional LDO regulators. Offered in small-outline integrated-circuit (SOIC) packages and (product preview only) 8-terminal thin shrink small-outline (TSSOP), the TPS72xx series devices are ideal for cost-sensitive designs and where board space is at a premium.

A combination of new circuit design and process innovation has enabled the usual pnp pass transistor to be replaced by a PMOS device. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is very low – maximum of 85 mV at 100 mA of load current (TPS7250) – and is directly proportional to the load current (see Figure 1). Since the PMOS pass element is a voltage-driven device, the quiescent current is very low (300 μA maximum) and is stable over the entire range of output load current (0 mA to 250 mA). Intended for use in portable systems such as laptops and cellular phones, the low-dropout voltage feature and micropower operation result in a significant increase in system battery operating life.

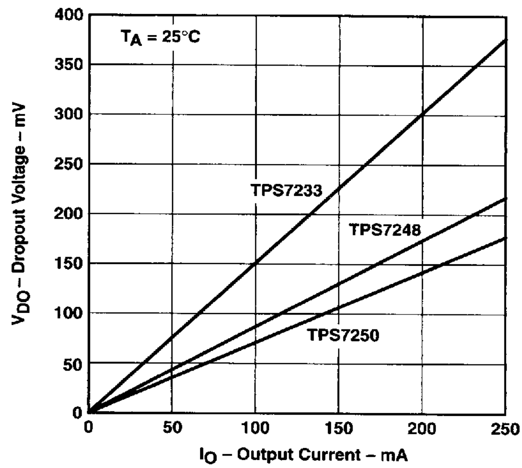


Figure 1. Typical Dropout Voltage Versus Output Current

This document contains information on products in more than one phase of development. The status of each device is indicated on the page(s) specifying its electrical characteristics.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

AVAILABLE OPTIONS

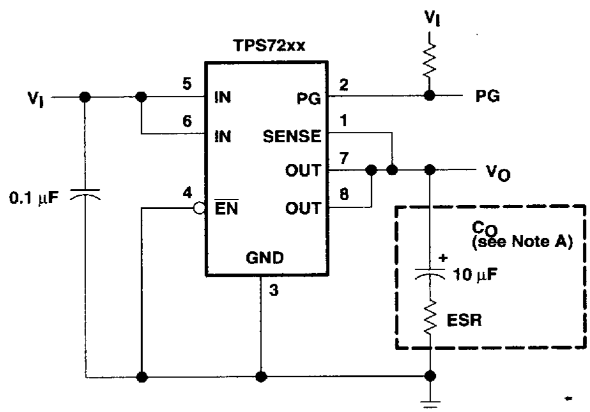
T_J	OUTPUT VOLTAGE (V)			PACKAGED DEVICES		CHIP FORM (Y)
	MIN	TYP	MAX	SMALL OUTLINE (D)	TSSOP (PW)	
−55°C to 150°C	4.9	5	5.1	TPS7250QD	TPS7250QPWLE	TPS7250Y
	4.75	4.85	4.95	TPS7248QD	TPS7248QPWLE	TPS7248Y
	3.23	3.3	3.37	TPS7233QD	TPS7233QPWLE	TPS7233Y
	Adjustable§ 1.2 V to 9.75 V			TPS7201QD	TPS7201QPWLE	TPS7201Y

The D package is available taped and reeled. Add R suffix to device type (e.g., TPS7250QDR). The PW package is only available left-end taped and reeled. The TPS7201Q is programmable using an external resistor divider (see application information). The chip form is tested at 25°C.

description (continued)

The TPS72xx also features a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to 0.5 μA maximum at T_J = 25°C. Other features include a power-good function that reports low output voltage and may be used to implement a power-on reset or a low-battery indicator.

The TPS72xx is offered in 3.3-V, 4.85-V, and 5-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.2 V to 9.75 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges (3% for adjustable version).



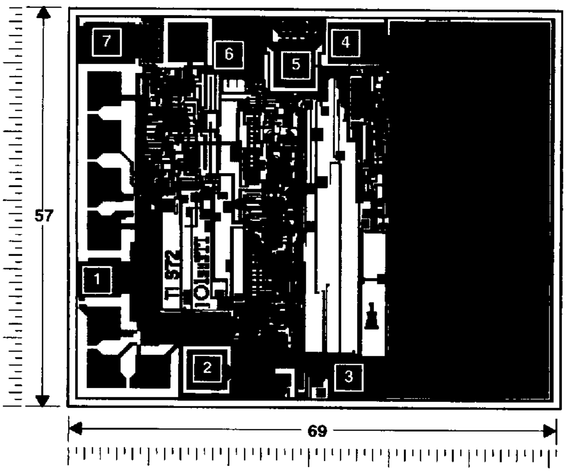
NOTE A. Capacitor selection is nontrivial. See application information section for details.

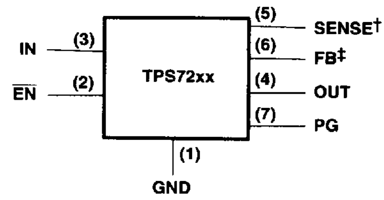
Figure 2. Typical Application Configuration

TPS72xx chip information

These chips, when properly assembled, display characteristics similar to the TPS72xxQ. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

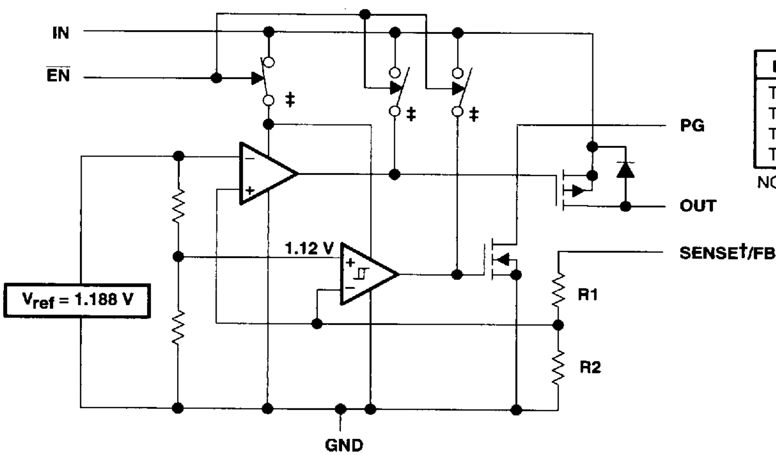
TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

† Fixed-voltage options only (TPS7233, TPS7248, and TPS7250)
‡ Adjustable version only (TPS7201)

NOTE A. For most applications, OUT and SENSE should be tied together as close as possible to the device; for other implementations, refer to SENSE-pin connection discussion in the application information section of this data sheet.

functional block diagram



RESISTOR DIVIDER OPTIONS

DEVICE	R1	R2	UNIT
TPS7201	0	∞	Ω
TPS7233	420	233	kΩ
TPS7248	726	233	kΩ
TPS7250	756	233	kΩ

NOTE : Resistors are nominal values only.

† For most applications, SENSE should be externally connected to OUT as close as possible to the device. For other implementations, refer to the SENSE-pin connection discussion in application information section.
‡ Switch positions are shown with EN low (active).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range‡, V_I, PG, SENSE, $\overline{EN}$ . . . . –0.3 to 10 V
Output current, I_O . . . . 1.5 A
Continuous total power dissipation . . . . See Dissipation Rating Tables 1 and 2
Operating virtual junction temperature range, T_J . . . . –55°C to 150°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE (see Note 1 and Figure 3)

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
PW§	525 mW	4.2 mW/°C	336 mW	273 mW	105 mW

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE (see Note 1 and Figure 4)

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25°C$	$T_C = 70°C$ POWER RATING	$T_C = 85°C$ POWER RATING	$T_C = 125°C$ POWER RATING
D	2063 mW	16.5 mW/°C	1320 mW	1073 mW	413 mW
PW§	2900 mW	23.2 mW/°C	1856 mW	1508 mW	580 mW

§ The PW package information is product preview only and is not yet available.
NOTE 1: Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum of 150°C. For guidelines on maintaining junction temperature within the recommended operating range, see application information section.

MAXIMUM CONTINUOUS DISSIPATION vs FREE-AIR TEMPERATURE

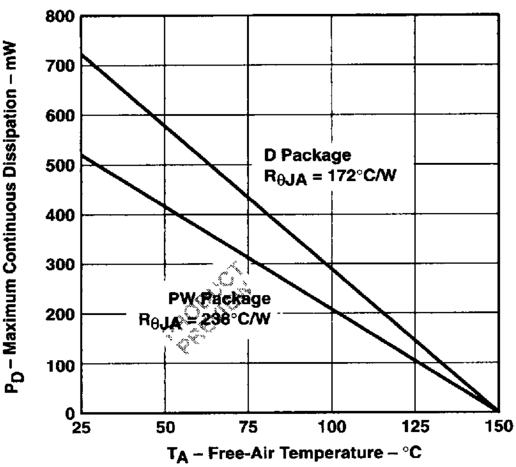


Figure 3

MAXIMUM CONTINUOUS DISSIPATION vs CASE TEMPERATURE

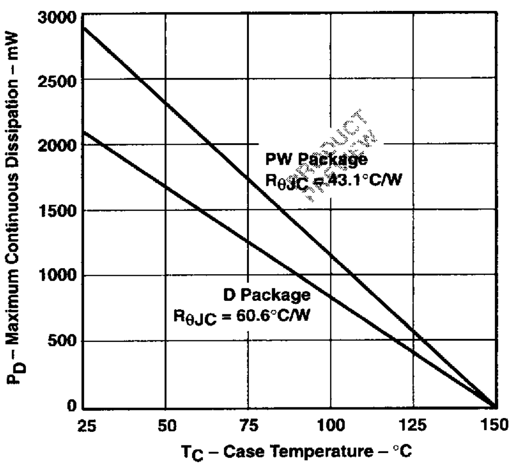


Figure 4

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I†	TPS7201Q	2.5	10	V
	TPS7233Q	3.98	10	
	TPS7248Q	5.24	10	
	TPS7250Q	5.41	10	
High-level input voltage at $\overline{EN}$, V_{IH}		2		V
Low-level input voltage at $\overline{EN}$, V_{IL}			0.5	V
Output current, I_O		0	250	mA
Operating virtual junction temperature, T_J		−40	125	°C

† Minimum input voltage defined in the recommended operating conditions is the maximum specified output voltage plus dropout voltage at the maximum specified load range. Since dropout voltage is a function of output current, the usable range can be extended for lighter loads. To calculate the minimum input voltage for the maximum load current used in a given application, use the following equation:

$$V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$$

Because the TPS7201 is programmable, $r_{DS(on)}$ should be used to calculate V_{DO} before applying the above equation. The equation for calculating V_{DO} from $r_{DS(on)}$ is given in Note 3 under the TPS7201 electrical characteristics table. The minimum value of 2.5 V is the absolute lower limit for the recommended input-voltage range for the TPS7201.

electrical characteristics, I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF (CSR† = 1 Ω), SENSE/FB shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	T_J	TPS7201Q, TPS7233Q TPS7248Q, TPS7250Q MIN	TYP	MAX	UNIT
Ground current (active mode)	$\overline{EN}$ ≤ 0.5 V, $V_I = V_O + 1$ V, 0 mA ≤ I_O ≤ 250 mA	25°C		180	225	μA
		−40°C to 125°C			325	
Input current (standby mode)	$\overline{EN} = V_I$, 2.7 V ≤ V_I ≤ 10 V	25°C			0.5	μA
		−40°C to 125°C			1	
Output current limit threshold	V_O = 0 V, V_I = 10 V	25°C		0.6	1	A
		−40°C to 125°C			1.5	
Pass-element leakage current in standby mode	$\overline{EN} = V_I$, 2.7 V ≤ V_I ≤ 10 V	25°C			0.5	μA
		−40°C to 125°C			1	
PG leakage current	V_{PG} = 10 V, Normal operation	25°C			0.5	μA
		−40°C to 125°C			0.5	
Output voltage temperature coefficient		−40°C to 125°C		31	75	ppm/°C
Thermal shutdown junction temperature				165		°C
$\overline{EN}$ logic high (standby mode)	2.5 V ≤ V_I ≤ 6 V	−40°C to 125°C	2			V
	6 V ≤ V_I ≤ 10 V		2.7			
$\overline{EN}$ logic low (active mode)	2.7 V ≤ V_I ≤ 10 V	25°C			0.5	V
		−40°C to 125°C			0.5	
$\overline{EN}$ hysteresis voltage		25°C		50		mV
$\overline{EN}$ input current	0 V ≤ V_I ≤ 10 V	25°C	−0.5		0.5	μA
		−40°C to 125°C	−0.5		0.5	
Minimum V_I for active pass element		25°C		1.9	2.5	V
		−40°C to 125°C			2.5	
Minimum V_I for valid PG	I_{PG} = 300 μA	25°C		0.95	1.5	V
		−40°C to 125°C			1.9	

† CSR(compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7201Q electrical characteristics, I_O = 10 mA, V_I = 3.5 V, $\overline{EN}$ = 0 V, C_O = 4.7 μF (CSR† = 1 Ω), FB shorted to OUT at device leads (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7201Q MIN	TPS7201Q TYP	TPS7201Q MAX	UNIT
Reference voltage (measured at FB with OUT connected to FB)	V_I = 3.5 V,	I_O = 10 mA	25°C		1.188		V
	2.5 V ≤ V_I ≤ 10 V, See Note 2	5 mA ≤ I_O ≤ 250 mA,	–40°C to 125°C	1.152		1.224	V
Reference voltage temperature coefficient			–40°C to 125°C		31	75	ppm/°C
Pass-element series resistance (see Note 3)	V_I = 2.4 V,	50 μA ≤ I_O ≤ 100 mA	25°C		2.1	4.2	Ω
			–40°C to 125°C			4.8	
	V_I = 2.4 V,	100 mA ≤ I_O ≤ 200 mA	25°C		2.9	4.4	
			–40°C to 125°C			4.6	
	V_I = 2.9 V,	50 μA ≤ I_O ≤ 250 mA	25°C		1.6	2.7	
			–40°C to 125°C			4.5	
	V_I = 3.9 V,	50 μA ≤ I_O ≤ 250 mA	25°C		1		
	V_I = 5.9 V,	50 μA ≤ I_O ≤ 250 mA	25°C		0.8		
Input regulation	V_I = 2.5 V to 10 V, See Note 2	50 μA ≤ I_O ≤ 250 mA,	25°C			23	mV
			–40°C to 125°C			36	
Output regulation	I_O = 5 mA to 250 mA, See Note 2	2.5 V ≤ V_I ≤ 10 V,	25°C		15	25	mV
			–40°C to 125°C			36	
	I_O = 50 μA to 250 mA, See Note 2	2.5 V ≤ V_I ≤ 10 V,	25°C		17	27	
			–40°C to 125°C			43	
Ripple rejection	f = 120 Hz	I_O = 50 μA	25°C	49	60		dB
			–40°C to 125°C	32			
		I_O = 250 mA, See Note 2	25°C	45	50		
			–40°C to 125°C	30			
Output noise spectral density	f = 120 Hz		25°C		2		μV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF	25°C		235		μVrms
		C_O = 10 μF	25°C		190		
		C_O = 100 μF	25°C		125		
PG trip-threshold voltage§	V_{FB} voltage decreasing from above V_{PG}		–40°C to 125°C		0.95 × $V_{FB(nom)}$		V
PG hysteresis voltage§	Measured at V_{FB}		25°C		12		mV
PG output low voltage§	I_{PG} = 400 μA,	V_I = 2.13 V	25°C		0.1	0.4	V
			–40°C to 125°C			0.4	
FB input current			25°C	–10	0.1	10	nA
			–40°C to 125°C	–20		20	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.
§ Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

NOTES: 2. When V_I < 2.9 V and I_O > 100 mA simultaneously, pass element $r_{DS(on)}$ increases (see Figure 10) to a point such that the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.

3. To calculate dropout voltage, use equation:

$$V_{DO} = I_O \cdot r_{DS(on)}$$

$r_{DS(on)}$ is a function of both output current and input voltage. The parametric table lists $r_{DS(on)}$ for V_I = 2.4 V, 2.9 V, 3.9 V, and 5.9 V, which corresponds to dropout conditions for programmed output voltages of 2.5 V, 3 V, 4 V, and 6 V, respectively. For other programmed values, refer to Figures 10 and 11.

TPS7233Q electrical characteristics, $I_O = 10$ mA, $V_I = 4.3$ V, $\overline{EN} = 0$ V, $C_O = 4.7\ \mu F$ (CSR† = 1 Ω), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7233Q MIN	TPS7233Q TYP	TPS7233Q MAX	UNIT
Output voltage	$V_I = 4.3$ V,	$I_O = 10$ mA	25°C		3.3		V
	$4.3\ V \le V_I \le 10$ V,	$5\ mA \le I_O \le 250$ mA	−40°C to 125°C	3.23		3.37	
Dropout voltage	$I_O = 10$ mA,	$V_I = 3.23$ V	25°C		14	20	mV
			−40°C to 125°C			30	
	$I_O = 100$ mA,	$V_I = 3.23$ V	25°C		140	180	
			−40°C to 125°C			232	
	$I_O = 250$ mA,	$V_I = 3.23$ V	25°C		360	460	
			−40°C to 125°C			610	
Pass-element series resistance	$(3.23\ V - V_O)/I_O$, $I_O = 250$ mA	$V_I = 3.23$ V,	25°C		1.5	1.84	Ω
			−40°C to 125°C			2.5	
Input regulation	$V_I = 4.3$ V to 10 V,	$50\ \mu A \le I_O \le 250$ mA	25°C		8	25	mV
			−40°C to 125°C			33	
Output regulation	$I_O = 5$ mA to 250 mA,	$4.3\ V \le V_I \le 10$ V	25°C		32	42	mV
			−40°C to 125°C			71	
	$I_O = 50\ \mu A$ to 250 mA,	$4.3\ V \le V_I \le 10$ V	25°C		41	55	
			−40°C to 125°C			98	
Ripple rejection	f = 120 Hz	$I_O = 50\ \mu A$	25°C	40	52		dB
			−40°C to 125°C	38			
		$I_O = 250$ mA	25°C	35	44		
			−40°C to 125°C	33			
Output noise spectral density	f = 120 Hz		25°C		2		µV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	$C_O = 4.7\ \mu F$	25°C		265		µVrms
		$C_O = 10\ \mu F$	25°C		212		
		$C_O = 100\ \mu F$	25°C		135		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		−40°C to 125°C		0.95 × $V_{O(nom)}$		V
PG hysteresis voltage			25°C		32		mV
PG output low voltage	$I_{PG} = 1$ mA,	$V_I = 2.8$ V	25°C		0.22	0.4	V
			−40°C to 125°C			0.4	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7248Q electrical characteristics, $I_O = 10$ mA, $V_I = 5.85$ V, $\overline{EN} = 0$ V, $C_O = 4.7\ \mu F$ (CSR† = 1 Ω), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7248Q MIN	TPS7248Q TYP	TPS7248Q MAX	UNIT
Output voltage	$V_I = 5.85$ V,	$I_O = 10$ mA	25°C		4.85		V
	$5.85\ V \le V_I \le 10$ V,	$5\ mA \le I_O \le 250$ mA	−40°C to 125°C	4.75		4.95	
Dropout voltage	$I_O = 10$ mA,	$V_I = 4.75$ V	25°C		10	19	mV
			−40°C to 125°C			30	
	$I_O = 100$ mA,	$V_I = 4.75$ V	25°C		90	100	
			−40°C to 125°C			150	
	$I_O = 250$ mA,	$V_I = 4.75$ V	25°C		216	250	
			−40°C to 125°C			285	
Pass-element series resistance	$(4.75\ V - V_O)/I_O$, $I_O = 250$ mA	$V_I = 4.75$ V,	25°C		0.8	1	Ω
			−40°C to 125°C			1.4	
Input regulation	$V_I = 5.85$ V to 10 V,	$50\ \mu A \le I_O \le 250$ mA	25°C			34	mV
			−40°C to 125°C			50	
Output regulation	$I_O = 5$ mA to 250 mA,	$5.85\ V \le V_I \le 10$ V	25°C		43	55	mV
			−40°C to 125°C			95	
	$I_O = 50\ \mu A$ to 250 mA,	$5.85\ V \le V_I \le 10$ V	25°C		55	75	
			−40°C to 125°C			135	
Ripple rejection	f = 120 Hz	$I_O = 50\ \mu A$	25°C	42	53		dB
			−40°C to 125°C	36			
		$I_O = 250$ mA	25°C	36	46		
			−40°C to 125°C	34			
Output noise spectral density	f = 120 Hz		25°C		2		$\mu V/\sqrt{Hz}$
Output noise voltage	$10\ Hz \le f \le 100$ kHz, CSR† = 1 Ω	$C_O = 4.7\ \mu F$	25°C		370		µVrms
		$C_O = 10\ \mu F$	25°C		290		
		$C_O = 100\ \mu F$	25°C		168		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		−40°C to 125°C		$0.95 \times V_{O(nom)}$		V
PG hysteresis voltage			25°C		50		mV
PG output low voltage	$I_{PG} = 1.2$ mA,	$V_I = 4.12$ V	25°C		0.2	0.4	V
			−40°C to 125°C			0.4	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7250Q electrical characteristics, $I_O = 10$ mA, $V_I = 6$ V, $\overline{EN} = 0$ V, $C_O = 4.7\ \mu F$ (CSR† = 1 Ω), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7250Q MIN	TPS7250Q TYP	TPS7250Q MAX	UNIT
Output voltage	$V_I = 6$ V,	$I_O = 10$ mA	25°C		5		V
	$6\ V \le V_I \le 10$ V,	$5\ mA \le I_O \le 250$ mA	–40°C to 125°C	4.9		5.1	
Dropout voltage	$I_O = 10$ mA,	$V_I = 4.88$ V	25°C		8	12	mV
			–40°C to 125°C			30	
	$I_O = 100$ mA,	$V_I = 4.88$ V	25°C		76	85	
			–40°C to 125°C			136	
	$I_O = 250\ \mu A$,	$V_I = 4.88$ V	25°C		190	206	
			–40°C to 125°C			312	
Pass-element series resistance	$(4.88\ V - V_O)/I_O$, $I_O = 250$ mA	$V_I = 4.88$ V,	25°C		0.76	0.825	Ω
			–40°C to 125°C			1.25	
Input regulation	$V_I = 6$ V to 10 V,	$50\ \mu A \le I_O \le 250$ mA	25°C			28	mV
			–40°C to 125°C			35	
Output regulation	$I_O = 5$ mA to 250 mA,	$6\ V \le V_I \le 10$ V	25°C		46	61	mV
			–40°C to 125°C			100	
	$I_O = 50\ \mu A$ to 250 mA,	$6\ V \le V_I \le 10$ V	25°C		59	79	
			–40°C to 125°C			150	
Ripple rejection	f = 120 Hz	$I_O = 50\ \mu A$	25°C	41	52		dB
			–40°C to 125°C	37			
		$I_O = 250$ mA	25°C	36	46		
			–40°C to 125°C	32			
Output noise spectral density	f = 120 Hz		25°C		2		μV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	$C_O = 4.7\ \mu F$	25°C		390		μVrms
		$C_O = 10\ \mu F$	25°C		300		
		$C_O = 100\ \mu F$	25°C		175		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		–40°C to 125°C		0.95 × $V_{O(nom)}$		V
PG hysteresis voltage			25°C		50		mV
PG output low voltage	$I_{PG} = 1.2$ mA,	$V_I = 4.25$ V	25°C		0.19	0.4	V
			–40°C to 125°C			0.4	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics, I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 µF (CSR† = 1 Ω), T_J = 25°C, SENSE/FB shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	TPS7201Y, TPS7233Y TPS7248Y, TPS7250Y			UNIT
		MIN	TYP	MAX	
Ground current (active mode)	$\overline{EN}$ ≤ 0.5 V, $V_I = V_O + 1$ V, 0 mA ≤ I_O ≤ 250 mA		180		µA
Output current limit threshold	V_O = 0 V, V_I = 10 V		0.6		A
Thermal shutdown junction temperature			165		°C
$\overline{EN}$ hysteresis voltage			50		mV
Minimum V_I for active pass element			1.9		V
Minimum V_I for valid PG	I_{PG} = 300 µA		0.95		V

† CSR(compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics, I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF (CSR† = 1 Ω), T_J = 25°C, FB shorted to OUT at device leads (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		TPS7201Y MIN	TPS7201Y TYP	TPS7201Y MAX	UNIT
Reference voltage (measured at FB with OUT connected to FB)	V_I = 3.5 V,	I_O = 10 mA		1.188		V
Pass-element series resistance (see Note 3)	V_I = 2.4 V,	50 μA ≤ I_O ≤ 100 mA		2.1		Ω
	V_I = 2.4 V,	100 mA ≤ I_O ≤ 200 mA		2.9		
	V_I = 2.9 V,	50 μA ≤ I_O ≤ 250 mA		1.6		
	V_I = 3.9 V,	50 μA ≤ I_O ≤ 250 mA		1		
	V_I = 5.9 V,	50 μA ≤ I_O ≤ 250 mA		0.8		
Output regulation	2.5 V ≤ V_I ≤ 10 V, See Note 2	I_O = 5 mA to 250 mA,		15		mV
	2.5 V ≤ V_I ≤ 10 V, See Note 2	I_O = 50 μA to 250 mA,		17		
Ripple rejection	V_I = 3.5 V, f = 120 Hz	I_O = 50 μA		60		dB
		I_O = 250 mA, See Note 2		50		
Output noise spectral density	V_I = 3.5 V,	f = 120 Hz		2		μV/√Hz
Output noise voltage	V_I = 3.5 V, 10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF		235		μVrms
		C_O = 10 μF		190		
		C_O = 100 μF		125		
PG hysteresis voltage§	V_I = 3.5 V,	Measured at V_{FB}		12		mV
PG output low voltage§	V_I = 2.13 V,	I_{PG} = 400 μA		0.1		V
FB input current	V_I = 3.5 V			0.1		nA

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.
§ Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

NOTES: 2 When V_I < 2.9 V and I_O > 100 mA simultaneously, pass element $r_{DS(on)}$ increases (see Figure 10) to a point such that the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.

3 To calculate dropout voltage, use equation:

$$V_{DO} = I_O \cdot r_{DS(on)}$$

$r_{DS(on)}$ is a function of both output current and input voltage. The parametric table lists $r_{DS(on)}$ for V_I = 2.4 V, 2.9 V, 3.9 V, and 5.9 V, which corresponds to dropout conditions for programmed output voltages of 2.5 V, 3 V, 4 V, and 6 V, respectively. For other programmed values, refer to Figures 10 and 11.

electrical characteristics, I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF (CSR† = 1 Ω), T_J = 25°C, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		TPS7233Y MIN	TPS7233Y TYP	TPS7233Y MAX	UNIT
Output voltage	V_I = 4.3 V,	I_O = 10 mA		3.3		V
Dropout voltage	V_I = 3.23 V,	I_O = 10 mA		14		mV
	V_I = 3.23 V,	I_O = 100 mA		140		
	V_I = 3.23 V,	I_O = 250 mA		360		
Pass-element series resistance	(3.23 V – V_O)/I_O, I_O = 250 mA	V_I = 3.23 V,		1.5		Ω
Input regulation	V_I = 4.3 V to 10 V,	50 μA ≤ I_O ≤ 250 mA		8		mV
Output regulation	4.3 V ≤ V_I ≤ 10 V,	I_O = 5 mA to 250 mA		32		mV
	4.3 V ≤ V_I ≤ 10 V,	I_O = 50 μA to 250 mA		41		
Ripple rejection	V_I = 4.3 V, f = 120 Hz	I_O = 50 μA		52		dB
		I_O = 250 mA		44		
Output noise spectral density	V_I = 4.3 V,	f = 120 Hz		2		μV/√Hz
Output noise voltage	V_I = 4.3 V, 10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF		265		μVrms
		C_O = 10 μF		212		
		C_O = 100 μF		135		
PG hysteresis voltage	V_I = 4.3 V			32		mV
PG output low voltage	V_I = 2.8 V,	I_{PG} = 1 mA		0.22		V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

PARAMETER	TEST CONDITIONS‡		TPS7248Y MIN	TPS7248Y TYP	TPS7248Y MAX	UNIT
Output voltage	V_I = 5.85 V,	I_O = 10 mA		4.85		V
Dropout voltage	V_I = 4.75 V,	I_O = 10 mA		10		mV
	V_I = 4.75 V,	I_O = 100 mA		90		
	V_I = 4.75 V,	I_O = 250 mA		216		
Pass-element series resistance	(4.75 V – V_O)/I_O, I_O = 250 mA	V_I = 4.75 V,		0.8		Ω
Output regulation	5.85 V ≤ V_I ≤ 10 V	I_O = 5 mA to 250 mA		43		mV
	5.85 V ≤ V_I ≤ 10 V	I_O = 50 μA to 250 mA		55		
Ripple rejection	V_I = 5.85 V, f = 120 Hz	I_O = 50 μA		53		dB
		I_O = 250 mA		46		
Output noise spectral density	V_I = 5.85 V,	f = 120 Hz		2		μV/√Hz
Output noise voltage	V_I = 5.85 V, 10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF		370		μVrms
		C_O = 10 μF		290		
		C_O = 100 μF		168		
PG hysteresis voltage	V_I = 5.85 V			50		mV
PG output low voltage	V_I = 4.12 V,	I_{PG} = 1.2 mA		0.2		V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics, I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 µF (CSR† = 1 Ω), T_J = 25°C, SENSE shorted to OUT (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS‡		TPS7250Q MIN	TPS7250Q TYP	TPS7250Q MAX	UNIT
Output voltage	V_I = 6 V,	I_O = 10 mA		5		V
Dropout voltage	V_I = 4.88 V,	I_O = 10 mA		8		mV
	V_I = 4.88 V,	I_O = 100 mA		76		
	V_I = 4.88 V,	I_O = 250 µA		190		
Pass-element series resistance	(4.88 V – V_O)/I_O, I_O = 250 mA	V_I = 4.88 V,		0.76		Ω
Input regulation	V_I = 6 V to 10 V,	50 µA ≤ I_O ≤ 250 mA				mV
Output regulation	6 V ≤ V_I ≤ 10 V,	I_O = 5 mA to 250 mA		46		mV
	6 V ≤ V_I ≤ 10 V,	I_O = 50 µA to 250 mA		59		
Ripple rejection	V_I = 6 V, f = 120 Hz	I_O = 50 µA		52		dB
		I_O = 250 mA		46		
Output noise spectral density	V_I = 6 V,	f = 120 Hz		2		µV/√Hz
Output noise voltage	V_I = 6 V, 10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 µF		390		µVrms
		C_O = 10 µF		300		
		C_O = 100 µF		175		
PG hysteresis voltage	V_I = 6 V			50		mV
PG output low voltage	V_I = 4.25 V,	I_{PG} = 1.2 mA		0.19		V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_Q	Quiescent current	vs Output current	5
		vs Input voltage	6
ΔI_Q†	Change in quiescent current	vs Free-air temperature	7
V_{DO}	Dropout voltage	vs Output current	8
ΔV_{DO}	Change in dropout voltage	vs Free-air temperature	9
V_{DO}	Dropout voltage (TPS7201 only)	vs Output current	10
$r_{DS(on)}$	Pass-element series resistance	vs Input voltage	11
ΔV_O	Change in output voltage	vs Free-air temperature	12
V_O	Output voltage	vs Input voltage	13
	Line regulation		14
	Load regulation (TPS7233)		15
	Load regulation (TPS7248)		16
	Load regulation (TPS7250)		17
$V_{O(PG)}$	Power-good (PG) voltage	vs Output voltage	18
$r_{DS(on)PG}$	Power-good (PG) on-resistance	vs Input voltage	19
V_I	Minimum input voltage for valid PG	vs Free-air temperature	20
	Output voltage response from enable ($\overline{EN}$)		21
	Load transient response (TPS7201/TPS7233)		22
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	Line transient response (TPS7233)		25
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	Ripple rejection	vs Frequency	27
	Output Spectral Noise Density	vs Frequency	28
	Compensation series resistance (CSR)	vs Output current (C_O = 4.7 μF)	29
		vs Added ceramic capacitance (C_O = 4.7 μF)	30
		vs Output current (C_O = 10 μF)	31
		vs Added ceramic capacitance (C_O = 10 μF)	32

† This symbol is not currently listed within EIA or JEDEC standards for semiconductor symbology.

TYPICAL CHARACTERISTICS

QUIESCENT CURRENT vs OUTPUT CURRENT

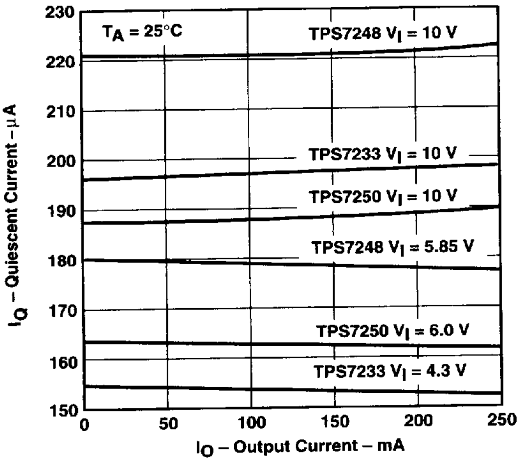


Figure 5

QUIESCENT CURRENT vs INPUT VOLTAGE

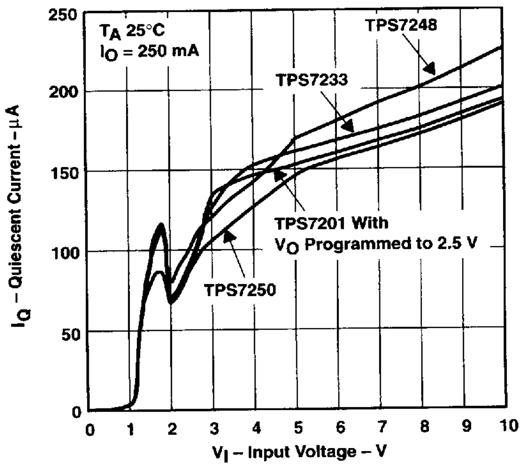


Figure 6

CHANGE IN QUIESCENT CURRENT vs FREE-AIR TEMPERATURE

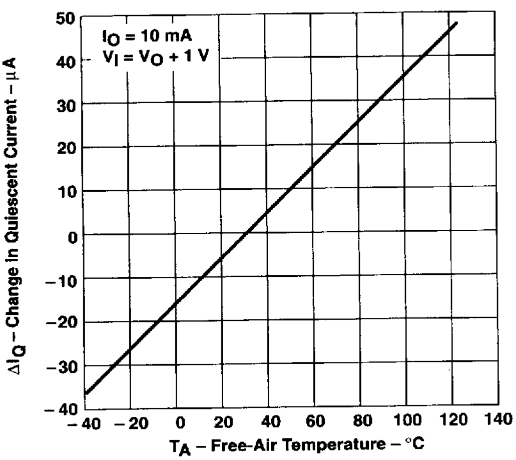


Figure 7

DROPOUT VOLTAGE vs OUTPUT CURRENT

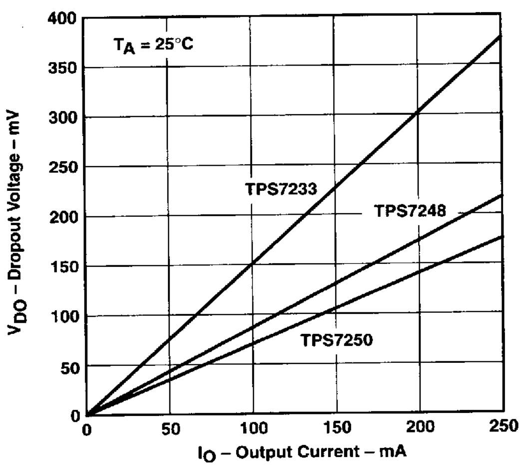


Figure 8

TYPICAL CHARACTERISTICS

CHANGE IN DROPOUT VOLTAGE vs FREE-AIR TEMPERATURE

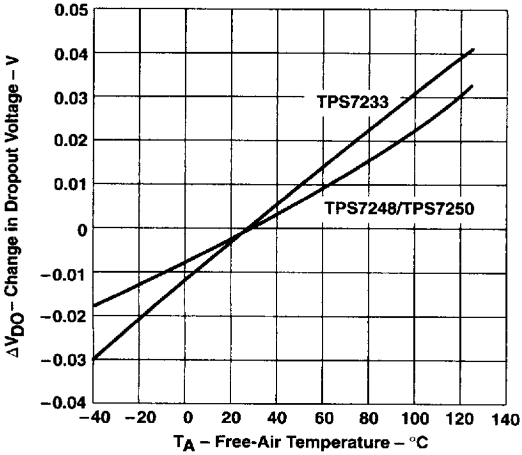


Figure 9

TPS7201 DROPOUT VOLTAGE vs OUTPUT CURRENT

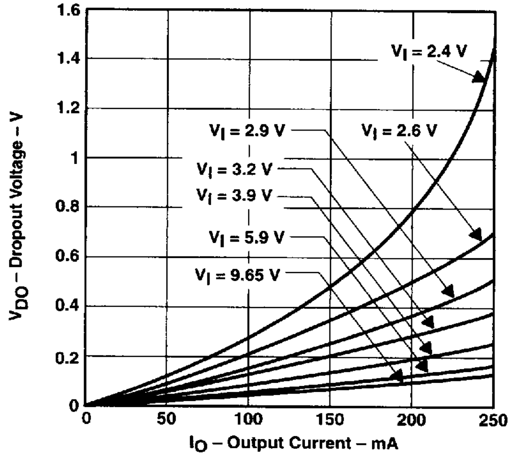


Figure 10

PASS ELEMENT SERIES RESISTANCE vs INPUT VOLTAGE

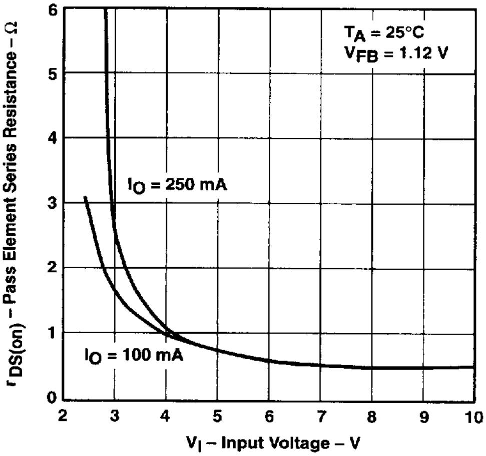


Figure 11

CHANGE IN OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

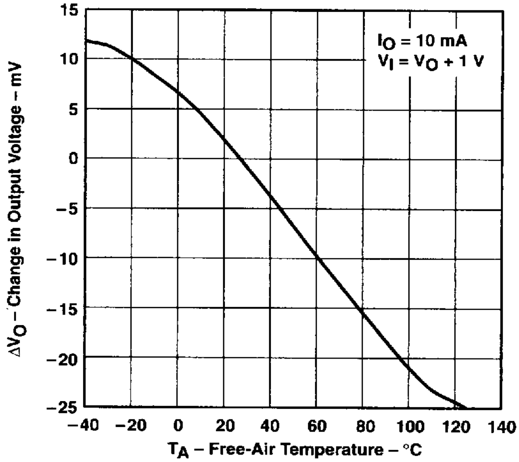


Figure 12

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

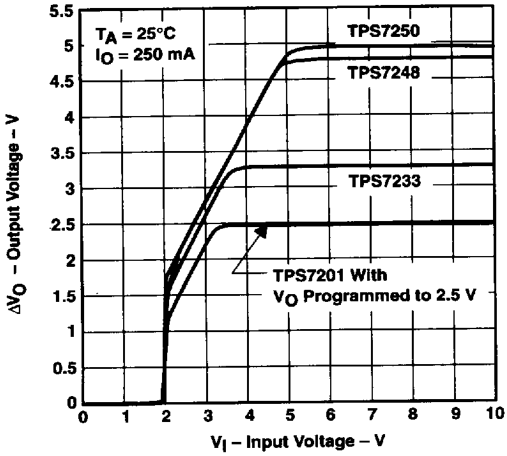


Figure 13

LINE REGULATION

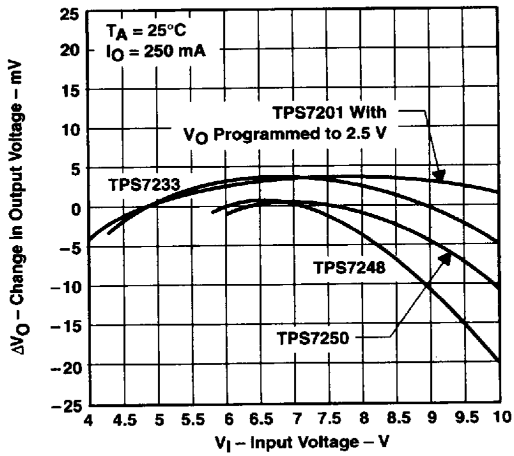


Figure 14

TPS7233
LOAD REGULATION

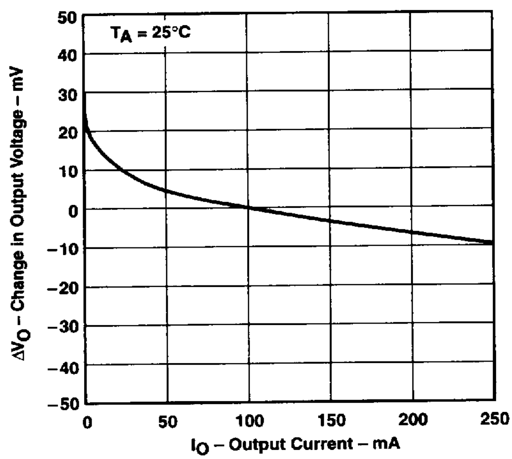


Figure 15

TPS7248
LOAD REGULATION

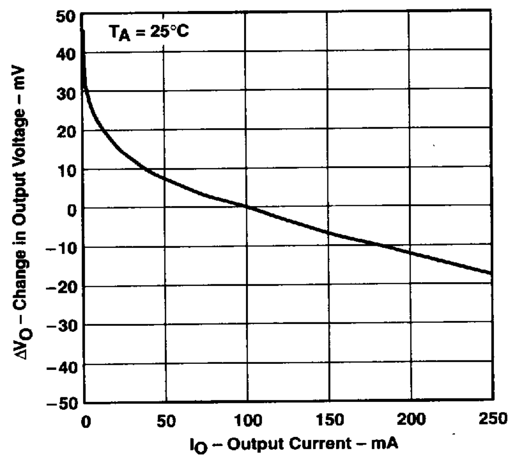


Figure 16

TYPICAL CHARACTERISTICS

TPS7250
LOAD REGULATION

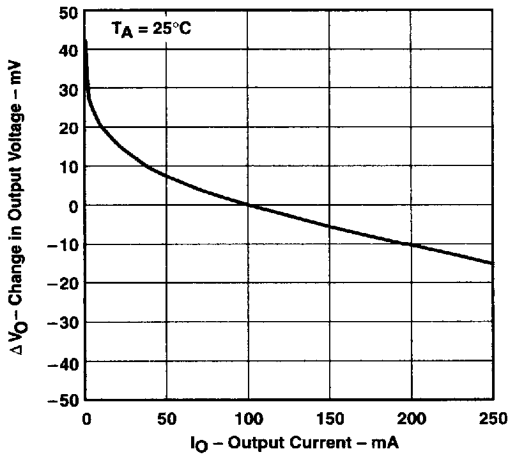
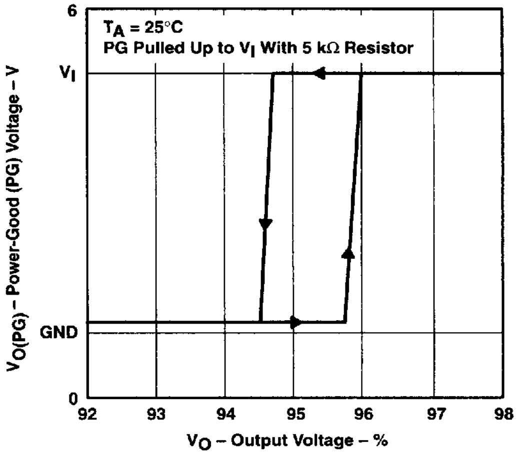


Figure 17

POWER-GOOD (PG) VOLTAGE
vs
OUTPUT VOLTAGE†



† V_O as a percent of V_{Onom}.

Figure 18

POWER-GOOD (PG) ON-RESISTANCE
vs
INPUT VOLTAGE

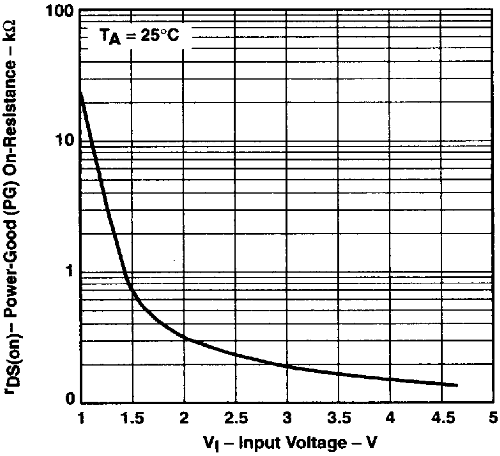


Figure 19

MINIMUM INPUT VOLTAGE FOR VALID PG
vs
FREE-AIR TEMPERATURE

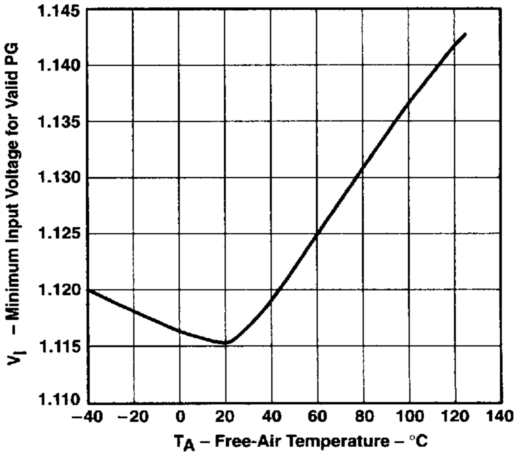


Figure 20

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE RESPONSE FROM ENABLE (EN)

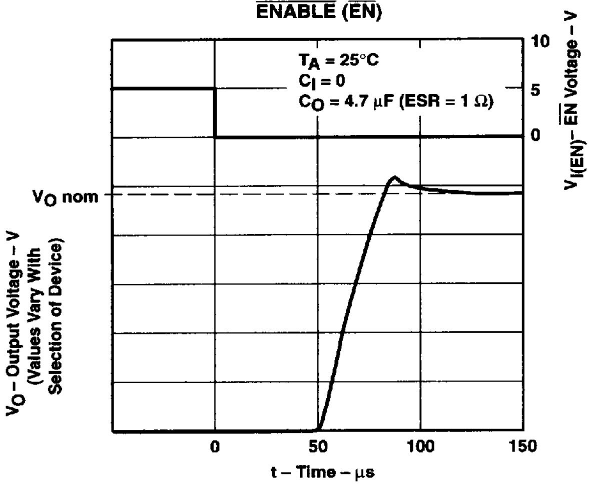


Figure 21

TPS7201 (WITH V_O PROGRAMMED TO 2.5 V), TPS7233 LOAD TRANSIENT RESPONSE

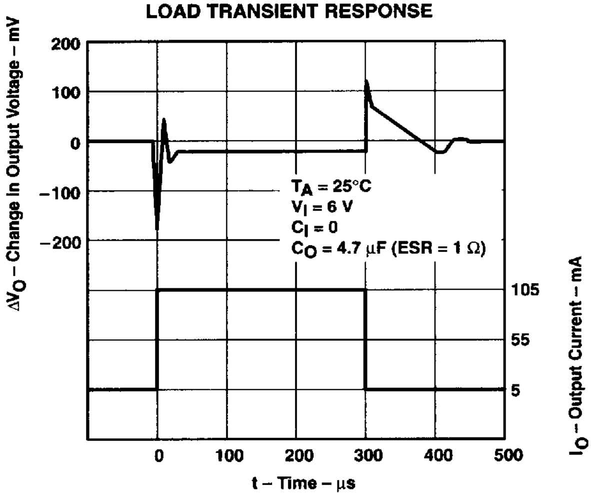


Figure 22

TYPICAL CHARACTERISTICS

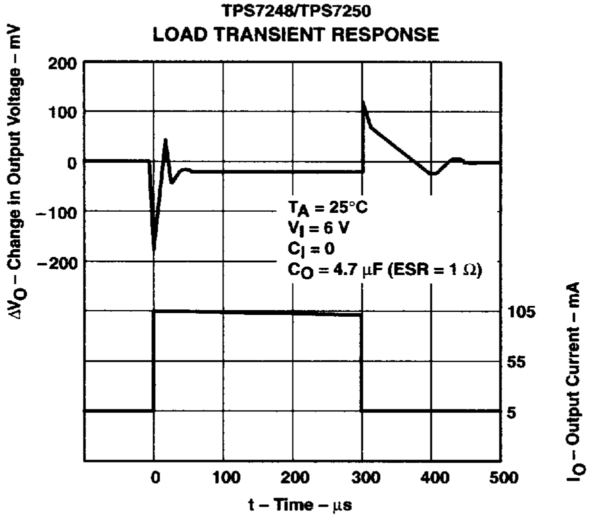


Figure 23

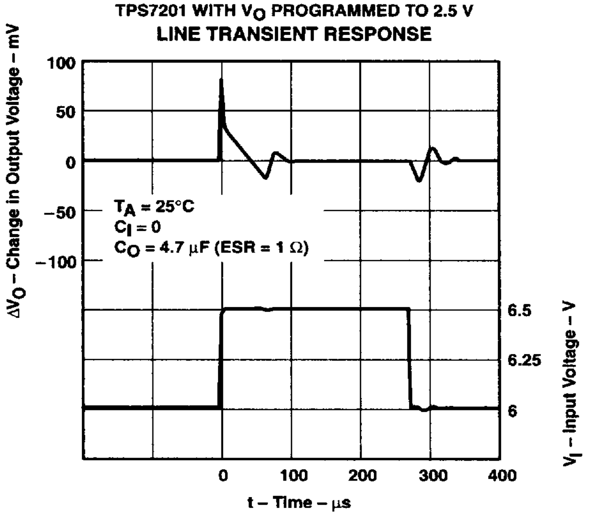


Figure 24

TYPICAL CHARACTERISTICS

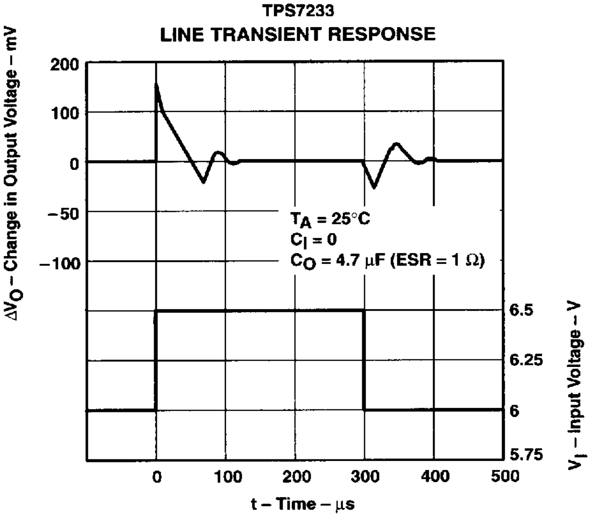


Figure 25

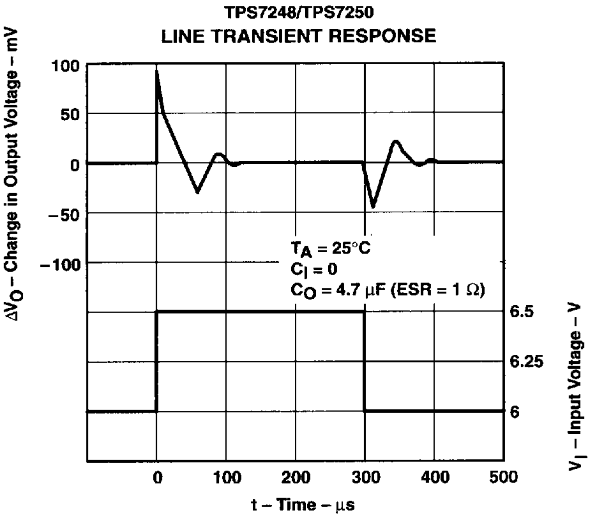


Figure 26

TYPICAL CHARACTERISTICS

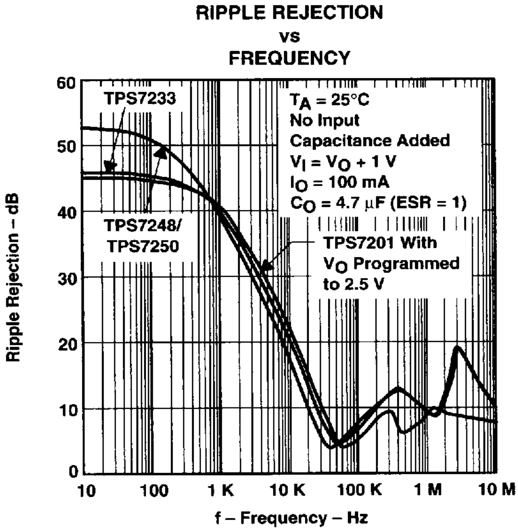


Figure 27

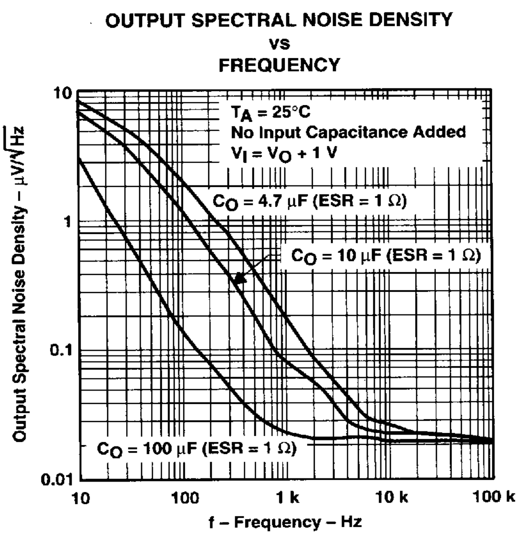


Figure 28

TYPICAL CHARACTERISTICS

**TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)†
vs
OUTPUT CURRENT**

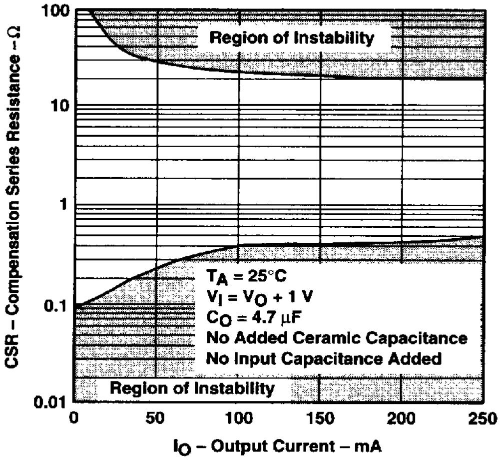


Figure 29

**TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)†
vs
ADDED CERAMIC CAPACITANCE**

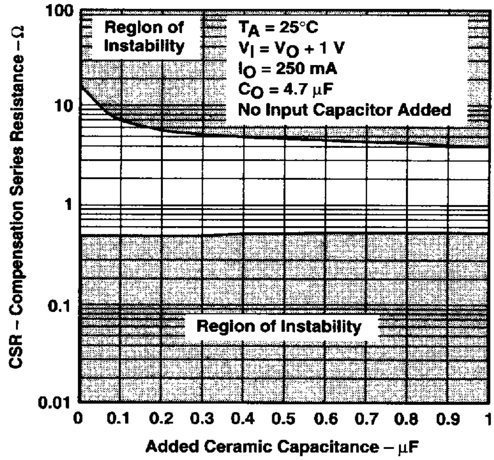


Figure 30

**TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)†
vs
OUTPUT CURRENT**

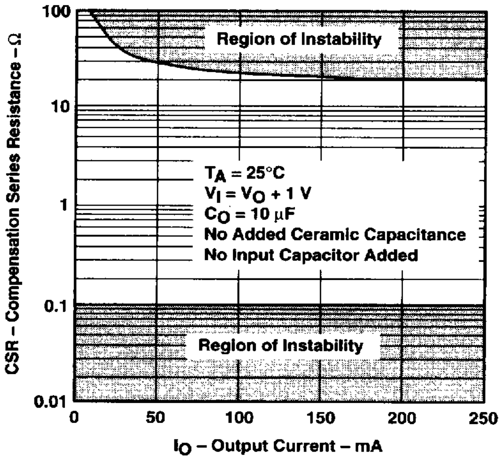


Figure 31

**TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)†
vs
ADDED CERAMIC CAPACITANCE**

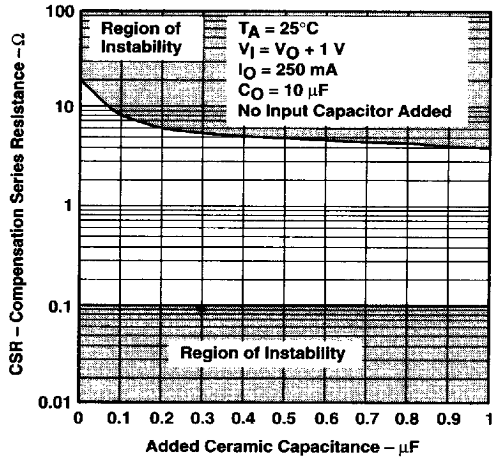


Figure 32

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

APPLICATION INFORMATION

The design of the TPS72xx family of low-dropout (LDO) regulators is based on the higher-current TPS71xx family. These new families of regulators have been optimized for use in battery-operated equipment and feature extremely low dropout voltages, low supply currents that remain constant over the full-output-current range of the device, and an enable input to reduce supply currents to less than 0.5 μA when the regulator is turned off.

device operation

The TPS72xx uses a PMOS pass element to dramatically reduce both dropout voltage and supply current over more conventional PNP-pass-element LDO designs. The PMOS transistor is a voltage-controlled device and, unlike a PNP transistor, does not require increased drive current as output current increases. Supply current in the TPS72xx is essentially constant from no-load to maximum.

Current limiting and thermal protection prevent damage by excessive output current and/or power dissipation. The device switches into a constant-current mode at approximately 1 A; further load increases reduce the output voltage instead of increasing the output current. The thermal protection shuts the regulator off if the junction temperature rises above 165°C. Recovery is automatic when the junction temperature drops approximately 5°C below the high temperature trip point. The PMOS pass element includes a back diode that safely conducts reverse current when the input voltage level drops below the output voltage level.

A logic high on the enable input, $\overline{EN}$, shuts off the output and reduces the supply current to less than 0.5 μA. $\overline{EN}$ should be grounded in applications where the shutdown feature is not used.

Power good (PG) is an open-drain output signal used to indicate output-voltage status. A comparator circuit continuously monitors the output voltage. When the output drops to approximately 95% of its nominal regulated value, the comparator turns on and pulls PG low.

A typical application circuit is shown in Figure 33.

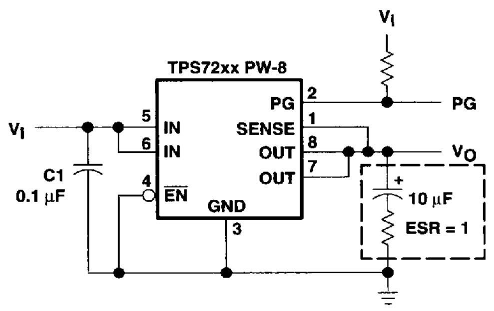


Figure 33. Typical Application Circuit

APPLICATION INFORMATION

external capacitor requirements

Although not required, a 0.047-µF to 0.1-µF ceramic bypass input capacitor, connected between IN and GND and located close to the TPS72xx, is recommended to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

An output capacitor is required to stabilize the internal feedback loop. For most applications, a 10-µF to 15-µF solid-tantalum capacitor with a 0.5-Ω resistor (see capacitor selection table) in series is sufficient. The maximum capacitor ESR should be limited to 1.3 Ω to allow for ESR doubling at cold temperatures. Figure 34 shows the transient response of a 5-mA to 85-mA load using a 10-µF output capacitor with a total ESR of 1.7 Ω.

A 4.7-µF solid-tantalum capacitor in series with a 1-Ω resistor may also be used (see Figures 29 and 30) provided the ESR of the capacitor does not exceed 1 Ω at room temperature and 2 Ω over the full operating temperature range.

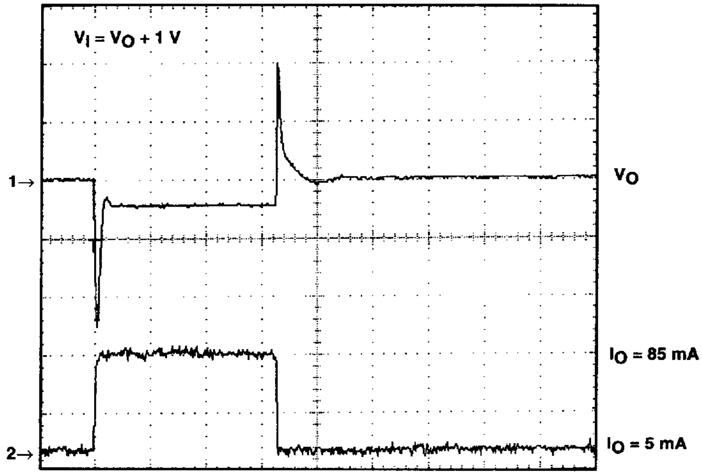


Figure 34. Load Transient Response (ESR total = 1.7 Ω), TPS7248Q

A partial listing of surface-mount capacitors usable with the TPS72xx family is provided below. This information (along with the stability graphs, Figures 29 through 32) is included to assist the designer in selecting suitable capacitors.

CAPACITOR SELECTION

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
592D156X0020R2T	Sprague	15 µF, 20 V	1.1	1.2 × 7.2 × 6
595D156X0025C2T	Sprague	15 µF, 25 V	1	2.5 × 7.1 × 3.2
595D106X0025C2T	Sprague	10 µF, 25 V	1.2	2.5 × 7.1 × 3.2
695D106X0035G2T	Sprague	10 µF, 35 V	1.3	2.5 × 7.6 × 2.5

† Size is in mm. ESR is maximum resistance in ohms at 100 kHz and T_A = 25°C. Listings are sorted by height.

APPLICATION INFORMATION

sense-pin connection

SENSE must be connected to OUT for proper operation of the regulator. Normally this connection should be as short as possible; however, remote sense may be implemented in critical applications when proper care of the circuit path is exercised. SENSE internally connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network, and any noise pickup on the PCB trace will feed through to the regulator output. SENSE must be routed to minimize noise pickup. Filtering SENSE using an RC network is not recommended because of the possibility of inducing regulator instability.

output voltage programming

The output voltage of the TPS7201 adjustable regulator is programmed using an external resistor divider as shown in Figure 35. The output voltage is calculated using:

$$V_O = V_{ref} \cdot \left(1 + \frac{R1}{R2}\right) \qquad (1)$$

where

V_{ref} = 1.188 V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 7-µA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 169 kΩ to set the divider current at 7 µA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \cdot R2 \qquad (2)$$

OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE (V)	DIVIDER RESISTANCE (kΩ)†	
	R1	R2
2.5	191	169
3.3	309	169
3.6	348	169
4	402	169
5	549	169
6.4	750	169

† 1% values shown.

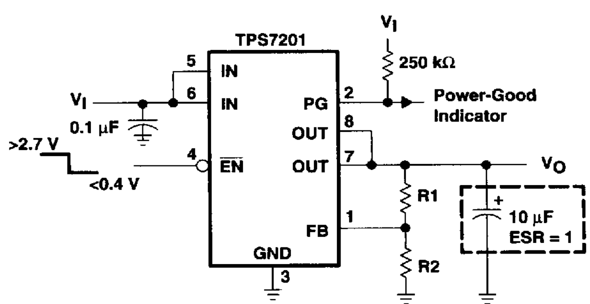


Figure 35. TPS7201 Adjustable LDO Regulator Programming

APPLICATION INFORMATION

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature allowable to avoid damaging the device is 150°C. These restrictions limit the power dissipation that the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where

$T_J max$ is the maximum allowable junction temperature, i.e.,150°C absolute maximum and 125°C recommended operating temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 172°C/W for the 8-terminal SOIC and 238°C/W for the 8-terminal TSSOP.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \cdot I_O$$

Power dissipation resulting from quiescent current is negligible.