

ACT-F512K8 High Speed 4 Megabit Monolithic FLASH

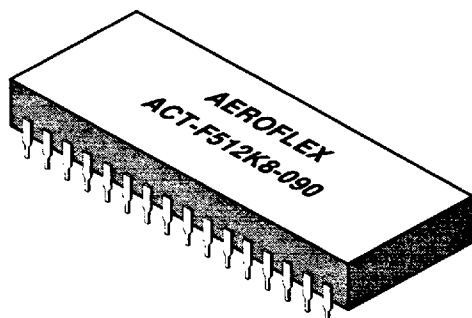
AEROFLEX CIRCUIT TECHNOLOGY

Features

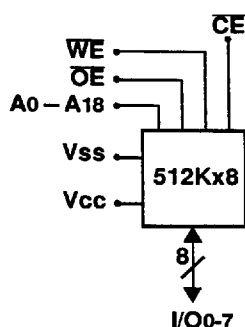
- Low Power Monolithic 512K x 8 FLASH
- TTL Compatible Inputs and CMOS Outputs
- Access Times of 90, 120 and 150nS
- +5V Programing, 5V $\pm 10\%$ Supply
- 100,000 Erase/Program Cycles
- Low Power CMOS, Standby Current 1 mA
- Page Program Operation and Internal Program Control Time
- Supports Full Chip Erase
- Embedded Erase and Program Algorithms
- Supports Full Chip Erase
- Internal Decoupling Capacitors
- MIL-PRF-38534 Compliant Circuits Available

- Industry Standard Pinouts
- Packaging – Hermetic Ceramic
 - 32 Lead, 1.6" x .6" x .20" Dual-in-line Package (DIP), Aeroflex code# "P4"
 - 36 Lead, .92" x .51" x .13" Ceramic Flat Package (FP), Preliminary, Aeroflex code# "F3"
- Sector Architecture
 - 8 Equal size sectors of 64K bytes each
 - Any Combination of Sectors can be Concurrently Erased
- Commercial, Industrial and Military Temperature Ranges
- DESC SMD (Standard Military Drawing) Pending

ACT-F512K8 DIP Package



Block Diagram – DIP(P4) & Flat Package(F3)



Pin Description

I/O0-7	Data I/O
A0-18	Address Inputs
WE	Write Enable
CE	Chip Enable
OE	Output Enable
Vcc	Power Supply
Vss	Ground
NC	Not Connected

General Description

The ACT-F512K8 is a high speed, 4 megabit CMOS monolithic Flash module designed for full temperature range military, space, or high reliability applications.

The MCM is input TTL and output CMOS compatible. The command register is written by bringing WE to a logic low level (V_{IL}), while CE is low and OE is at logic high level (V_{IH}). Reading is accomplished by chip Enable (CE) and Output Enable (OE) being logically active, see Figure 9. Access time grades of 90nS, 120nS and 150nS maximum are standard.

The ACT-S512K8 is available in a choice of hermetically sealed ceramic packages; a 36 lead .92"x.51" x.13" flat package or a 32 pin 1.6"x.60" x.20" DIP package for operation over the temperature range -55°C to +125°C and

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0047156 0000492 676

General Description, Cont'd.

military environmental conditions.

The flash memory is organized as 512K bytes of 8 bits and is designed to be programmed in-system with the standard system 5.0V V_{CC} supply. A 12.0V V_{PP} is not required for write or erase operations. The MCM can also be reprogrammed with standard EPROM programmers (with the proper socket).

The standard ACT-F512K8 offers access times between 90ns and 150ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the device has separate chip enable (CE), write enable (WE) and output enable (OE) controls. The ACT-F512K8 is command set compatible with JEDEC standard 1 Mbit EEPROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations.

Reading data out of the device is similar to reading from 12.0V Flash or EPROM devices. The ACT-F512K8 is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in less than 0.3 second. Erase is accomplished by

executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array, (if it is not already programmed before) executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The module is typically erased and verified in 1.5 seconds (if already completely preprogrammed).

Also the device features a sector erase architecture. The sector mode allows for 64K byte blocks of memory to be erased and reprogrammed without affecting other blocks. The ACT-F512K8 is erased when shipped from the factory.

The device features single 5.0V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by Data Polling of D7 or by the Toggle Bit feature on D6. Once the end of a program or erase cycle has been completed, the device internally resets to the read mode.

All bits of each die in the ACT-F512K8 can be electrically erased, or all bits within a sector of the die, via Fowler-Nordhiem tunneling. Bytes are programmed one byte at a time by hot electron injection.

A DESC Standard Military Drawing (SMD) number is pending.

Absolute Maximum Ratings

Parameter	Range	Units
Case Operating Temperature	-55 to +125	°C
Storage Temperature Range	-65 to +150	°C
Supply Voltage Range (Vcc)	-2.0 to +7.0	V
Signal Voltage Range (Any Pin Except A9) Note 1	-2.0 to +7.0	V
Maximum Lead Temperature (10 seconds)	300	°C
Data Retention	10	Years
Endurance (Write/Erase cycles)	100,000 Minimum	
A9 Voltage for sector protect (Vid) Note 2	-2.0 to +14.0	V

Note 1. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may over shoot to -2.0V for periods of up to 20nS. Maximum DC voltage on output and I/O pins is Vcc + 0.5V. During voltage transitions, outputs may overshoot to Vcc + 2.0V for periods up to 20 nS.

Note 2. Minimum DC input voltage on A9 is -0.5V. During voltage transitions, A9 may overshoot Vss to -2.0V for periods of up to 20 nS. Maximum DC input voltage on A9 is +13.5V which may overshoot to 14.0V for periods up to 20 nS.

Normal Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
VCC	Power Supply Voltage	+4.5	+5.5	V
VIH	Input High Voltage	+2.0	V _{CC} + 0.5	V
VIL	Input Low Voltage	-0.5	+0.8	V
TA	Operating Temperature (Military)	-55	+125	°C
VID	A9 Voltage for sector protect	11.5	12.5	V

Capacitance

(VIN= 0V, f = 1MHz, TA = 25°C)

Symbol	Parameter	Maximum	Units
CAD	A0 – A18 Capacitance	15	pF
COE	OE Capacitance	15	pF
CWE	Write Enable Capacitance	15	pF
CCE	Chip Enable Capacitance	15	pF
CI/O	I/O0 – I/O7 Capacitance	15	pF

Parameters Guaranteed but not tested

DC Characteristics – CMOS Compatible

(Vcc = 5.0V, Vss = 0V, TA = -55°C to +125°C)

Parameter	Sym	Conditions	Speeds 90, 120 & 150nS		
			Minimum	Maximum	Units
Input Leakage Current	ILI	VCC = 5.5V, VIN = GND to VCC		10	µA
Output Leakage Current	ILOX32	VCC = 5.5V, VIN = GND to VCC		10	µA
Active Operating Supply Current for Read (1)	Icc1	CE = VIL, OE = VIH, f = 5MHz		50	mA
Active Operating Supply Current for Program or Erase(2)	Icc2	CE = VIL, OE = VIH		60	mA
Operating Standby Supply Current	Icc3	VCC = 5.5V, CE = VIH, f = 5MHz		1.6	mA
Output Low Voltage	VOL	IOL = +12.0 mA, VCC = 4.5V		0.45	V
Output High Voltage	VOH1	Ioh = -2.5 mA, VCC = 4.5V	0.85 x VCC		V
Low Power Supply Lock-Out Voltage	VLKO		3.2	4.2	V

Note 1. The Icc current listed includes both the DC operating current and the frequency dependent component (At 6 MHz). The frequency component typically is less than 2 mA/MHz, with OE at VIN.

Note 2. Icc active while Embedded Algorithm (Program or Erase) is in progress.

Note 3. DC Test conditions: VIL = 0.3V, VIN = Vcc - 0.3V

AC Characteristics – Read Only Operations

(Vcc = 5.0V, Vss = 0V, TA = -55°C to +125°C)

Parameter	Symbol		-90		-120		-150		Units
	JEDEC	Stand'd	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tAVAV	trc	90		120		150		nS
Address Access Time	tAVQV	tACC		90		120		150	nS
Chip Enable Access Time	tELQV	tCE		90		120		150	nS
Output Enable to Output Valid	tGLOV	tOE		35		50		55	nS
Chip Enable to Output High Z (1)	tEHQZ	tDF		20		30		35	nS
Output Enable High to Output High Z(1)	tGHQZ	tDF		20		30		35	nS
Output Hold from Address, \overline{CE} or \overline{OE} Change, Whichever is First	tAXQX	tOH	0		0		0		nS

Note 1. Guaranteed by design, but not tested

AC Characteristics – Write/Erase/Program Operations, WE Controlled

(Vcc = 5.0V, Vss = 0V, TA = -55°C to +125°C)

Parameter	Symbol		-90		-120		-150		Units
	JEDEC	Stand'd	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAC	tWC	90		120		150		nS
Chip Enable Setup Time	tELWL	tCE	0		0		0		nS
Write Enable Pulse Width	tWLWH	tWP	45		50		50		nS
Address Setup Time	tAVWL	tAS	0		0		0		nS
Data Setup Time	tdVWH	tDS	45		50		50		nS
Data Hold Time	tWHDX	tDH	0		0		0		nS
Address Hold Time	tWLAX	tAH	45		50		50		nS
Write Enable Pulse Width High	tWHWL	tWPH	20		20		20		nS
Duration of Byte Programming Operation Typ = 16 μ S	tWHWH1		16		16		16		μ S
Chip and Sector Erase	tWHWH2		1.5	30	1.5	30	1.5	30	Sec
Read Recovery Time before Write	tGHWL		0		0		0		μ S
Vcc Setup Time		tVCE	50		50		50		μ S
Chip Programming Time				50		50		50	Sec

AC Characteristics – Write/Erase/Program Operations, \overline{CE} Controlled

(Vcc = 5.0V, Vss = 0V, TA = -55°C to +125°C)

Parameter	Symbol		-90		-120		-150		Units
	JEDEC	Stand'd	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAC	tWC	90		120		150		nS
Write Enable Setup Time	tWLEL	tWS	0		0		0		nS
Chip Enable Pulse Width	tELEH	tCP	45		50		55		nS
Address Setup Time	tAVEL	tAS	0		0		0		nS
Data Setup Time	tdVEH	tDS	45		50		55		nS
Data Hold Time	tENDX	tDH	0		0		0		nS
Address Hold Time	tELAX	tAH	45		50		55		nS
Chip Select Pulse Width High	tEHLEL	tCPH	20		20		20		nS
Duration of Byte Programming	tWHWH1		16		16		16		μ S
Chip and Sector Erase Time	tWHWH2		1.5	30	1.5	30	1.5	30	Sec
Read Recovery Time	tGHLEL		0		0		0		nS
Chip Programming Time				12.5		12.5		12.5	Sec

Device Operation

The ACT-F512K8 MCM is composed of One (1), four (1) megabit flash device. Programming of the ACT-F512K8 is accomplished by executing the program command sequence. The program algorithm, which is an internal algorithm, automatically times the program pulse widths and verifies proper cell status. Sectors can be programmed and verified in less than 0.3 second. Erase is accomplished by executing the erase command sequence. The erase algorithm, which is internal, automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell status. The entire memory is typically erased and verified in 1.5 seconds (if pre-programmed). The sector mode allows for 64K byte blocks of memory to be erased and reprogrammed without affecting other blocks.

Bus Operation

READ

The ACT-F512K8 has two control functions, both of which must be logically active, to obtain data at the outputs. Chip Enable (\overline{CE}) is the power control and should be used for device selection. Output-Enable (\overline{OE}) is the output control and should be used to gate data to the output pins of the chip selected. Figure 7 illustrates AC read timing waveforms.

OUTPUT DISABLE

With Output-Enable at a logic high level (V_{IH}), output from the device is disabled. Output pins are placed in a high impedance state.

STANDBY MODE

The ACT-F512K8 standby mode consumes less than 6.5 mA. In the standby mode the outputs are in a high impedance state, independent of the \overline{OE} input. If the device is deselected during erasure or programming, the device will draw active current until the operation is completed.

WRITE

Device erasure and programming are accomplished via the command register. The contents of the register serve as input to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy an addressable memory location. The register is a latch used to store the command, along with address and data information needed to execute the command. The command register is written by bringing \overline{WE} to a logic low level (V_{IL}), while \overline{CE} is low and \overline{OE} is at V_{IH} . Addresses are latched on the falling edge of \overline{WE} or \overline{CE} , whichever happens later. Data is latched on the rising edge of the \overline{WE} or \overline{CE} whichever occurs first. Standard microprocessor write timings are used. Refer to AC Program Characteristics and Waveforms, Figures 3, 8 and 13.

Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. Table 3 defines these register command sequences.

READ/RESET COMMAND

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard Microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Figure 7 for the specific timing parameters.

Table 1 – Bus Operations

Operation	\overline{CE}	\overline{OE}	\overline{WE}	A0	A1	A9	I/O
READ	L	L	H	A0	A1	A9	DOUT
STANDBY	H	X	X	X	X	X	HIGH Z
OUTPUT DISABLE	L	H	H	X	X	X	HIGH Z
WRITE	L	H	L	A0	A1	A9	DIN
ENABLE SECTOR PROTECT	L	V_{ID}	L	X	X	V_{ID}	X
VERIFY SECTOR PROTECT	L	L	H	L	H	V_{ID}	Code

Table 2 – Sector Addresses Table

	A16	A15	A14	Address Range
SA0	0	0	0	00000h – 03FFFh
SA1	0	0	1	04000h – 07FFFh
SA2	0	1	0	08000h – 0BFFFh
SA3	0	1	1	0C000h – 0FFFFh
SA4	1	0	0	10000h – 13FFFh
SA5	1	0	1	14000h – 17FFFh
SA6	1	1	0	18000h – 1BFFFh
SA7	1	1	1	1C000h – 1FFFFh

Table 3 — Commands Definitions

Command Sequence	Bus Write Cycles	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
Required		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	1	XXXH	F0H										
Read/Reset	4	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD				
Autoselect	4	5555H	AAH	2AAAH	55H	5555H	90H						
Byte Program	6	5555H	AAH	2AAAH	55H	5555H	A0H	PA	PD				
Chip Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H
Sector Erase Suspend	Erase can be suspended during sector-erase with Address (Don't care), Data (B0H)												
Sector Erase Resume	Erase can be resumed after suspend with Address (Don't care), Data (30H)												

NOTES:

1. Address bit A15, A16, A17 and A18 = X = Don't Care. Write Sequences may be initiated with A15 in either state.
2. Address bit A15, A16, A17 and A18 = X = Don't Care for all address commands except for Program Address (PA) and Sector Address (SA).
3. RA = Address of the memory location to be read
PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the WE pulse.
SA = Address of the sector to be erased. The combination of A18, A17, A16 will uniquely select any sector.
4. RD = Data read from location RA during read Operation.
PD = Data to be programmed at location PA. Data is latched on the rising edge of WE.

BYTE PROGRAMING

The device is programmed on a byte-by-byte basis. Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of \overline{CE} or \overline{WE} , whichever occurs later, while the data is latched on the rising edge of \overline{CE} or \overline{WE} whichever occurs first. The rising edge of \overline{CE} or \overline{WE} begins programming. Upon executing the program algorithm command sequence the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell status. The automatic programming operation is completed when the data on D7 is equivalent to data written to this bit at which time the device returns to the read mode and addresses are no longer latched. The device requires a valid address be supplied by the System at this time. Data Polling must be performed at the memory location which is being programmed.

Programming is allowed in any address sequence and across sector boundaries.

Figure 3 illustrates the programming algorithm using typical command strings and bus operations.

CHIP ERASE

Chip erase is a six bus cycle operation. There are two 'unlock' write cycles. These are followed by writing the 'set-up' command. Two more 'unlock' write cycles are then followed by the chip erase command. Chip erase does not require the user to program the device prior to erase. Upon executing the erase algorithm (Figure 4) sequence the device automatically will program and verify the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last \overline{WE} pulse in the command sequence and terminates when the data in D7 is "1" (see Write Operation

Status section - Table 4) at which time the device returns to read the mode. See Figures 4 and 9.

SECTOR ERASE

Sector erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "setup" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of \overline{WE} , while the command (data) is latched on the rising edge of \overline{WE} . A time-out of 100 μ s from the rising edge of the last sector erase command will initiate the sector erase command(s).

Multiple sectors may be erased concurrently by writing the six bus cycle operations as described above. This sequence is followed with writes of the sector erase command 30H to address in other sectors desired to be concurrently erased. A time-out of 100 μ s from the rising edge of the \overline{WE} pulse for the last sector erase command will initiate the sector erase. If another sector erase command is written within the 100 μ s time-out window the timer is reset. Any command other than sector erase within the time-out window will reset the device to the read mode, ignoring the previous command string. Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 7).

Sector erase does not require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

Data Protection

The ACT-F512K8 is designed to offer protection against accidental erasure or programming caused

by spurious system level singles that may exist during power transitions. During power up the device automatically resets the internal state machine in the read mode. Also, with its control register architecture, alteration of the memory content only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

LOW V_{CC} WRITE INHIBIT

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.2V (typically 3.7V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO} . It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above 3.2V.

WRITE PULSE GLITCH PROTECTION

Noise pulses of less than 5nS (typical) on \overline{OE} , \overline{CE} or \overline{WE} will not initiate a write cycle.

LOGICAL INHIBIT

Writing is inhibited by holding anyone of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle \overline{CE} and \overline{WE} must be logical zero while \overline{OE} is a logical one.

POWER-UP WRITE INHIBIT

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of \overline{WE} . The internal state machine is automatically reset to the read mode on power-up.

Write Operation Status

D7

DATA POLLING

The ACT-F512K8 features $\overline{\text{Data}}$ Polling as a method to indicate to the host that the internal algorithms are in progress or completed. During the program algorithm, an attempt to read the device will produce compliment data of the data last written to D7. During the erase algorithm, an attempt to read the device will produce a "0" at the D7 Output. Upon completion of the erase algorithm an attempt to read the device will produce a "1" at the D7 Output.

For chip Erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth \overline{WE} pulse in the six write pulse sequence. For sector erase, the $\overline{\text{Data}}$ Polling is valid after the last rising edge of the sector erase \overline{WE}

pulse. $\overline{\text{Data}}$ polling must be performed at a sector address within any of the sectors being erased and not a protected sector. Otherwise, the status may not be valid. Once the algorithm operation is close to being completed, data pins (D7) change asynchronously while the output enable (\overline{OE}) is asserted low. This means that the device is driving status information on D7 at one instance of time and then that byte's valid data at the next instant of time. Depending on when the system samples the D7 Output, it may read the status or valid data. Even if the device has completed internal algorithm operation and D7 has a valid data, the data outputs on D0 - D6 may be still invalid. The valid data on D0 - D7 will be read on the successive read attempts. The $\overline{\text{Data}}$ Polling feature is only active during the programming algorithm, erase algorithm, or sector erase time-out.

See Figures 6 and 10 for the Data Polling specifications.

D6

TOGGLE BIT

The ACT-F512K8 also features the "Toggle Bit" as a method to indicate to the host system that algorithms are in progress or completed.

During a program or erase algorithm cycle, successive attempts to read data from the device will result in D6 toggling between one and zero. Once the program or erase algorithm cycle is completed, D6 Will stop toggling and valid data will be read on successive attempts. During programming the Toggle Bit is valid after the rising edge of the fourth \overline{WE} pulse in the four write pulse sequence. For chip erase the Toggle Bit is valid after the rising edge of the sixth \overline{WE} pulse in the six write pulse sequence. For Sector erase, the Toggle Bit is valid after the last rising edge of the sector erase \overline{WE} pulse. The Toggle Bit is active during the sector time out.

See Figure 1 and 5.

D5

EXCEEDED TIMING LIMITS

D5 will indicate if the program or erase time has exceeded the specified limits. Under these conditions D5 will produce a "1". The Program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is the only operation function of the device under this condition. The \overline{CE} circuit will partially power down the device under these conditions by approximately 2 mA. The \overline{OE} and \overline{WE} pins will control the output disable functions as shown in Table 1. To reset the device, write the reset command sequence to the device. This allows the system to continue to use the other active sectors in the device.

D3

SECTOR ERASE TIMER

After the completion of the initial sector erase command sequence the sector erase time-out will begin. D3 will remain low until the time-out is complete.

Data Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit indicates the device has been written with a valid erase command, D3 may be used to determine if the sector erase timer window is still open. If D3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by Data Polling or Toggle Bit. If D3 is low ("0"), the device will accept additional sector erase commands. To ensure the command has been accepted, the software should check the status of D3 prior to and following each subsequent sector erase command. If D3 were high on the second status check, the command may not have been accepted. See Table 4

Sector Protection Algorithms

SECTOR PROTECTION

The ACT-F512K8 features hardware sector protection which will disable both program and erase operations to an individual sector or any group of sectors. To activate this mode, the programming equipment must force V_{DD} on control pin $\overline{\text{OE}}$ and address pin A9. The sector addresses should be set using higher address lines A18, A17, and A16. The protection mechanism begins on the falling edge of the $\overline{\text{WE}}$ pulse and is terminated with the rising edge of the same.

To verify programming of the protection circuitry, the programming equipment must force V_{DD} on address

pin A9 with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ at V_{IL} and $\overline{\text{WE}}$ at V_{IH} . Scanning the sector addresses (A16, A17, and A18) while (A6, A1, A0) = (0, 1, 0,) will produce a logical "1" code at device output D0 for a protected sector. Otherwise the device will read 00H for unprotected sector. In this mode, the lower order addresses, except for 0, A1, and A6 are don't care.

It is also possible to verify if a sector is protected during the sector protection operation. This is done by setting A6 = $\overline{\text{CE}}$ = $\overline{\text{OE}}$ = V_{IL} and $\overline{\text{WE}}$ = V_{IH} (A9 remains high at V_{DD}). Reading the device at address location XXX2H, where the higher order addresses (A18, A17, and A16) define a particular sector, will produce 01H at data outputs (D0 - D7) for a protected sector.

SECTOR UNPROTECT

The ACT-F512K8 also features a sector unprotect mode, so that a protected sector may be unprotected to incorporate any changes in the code. All sectors should be protected prior to unprotecting any sector.

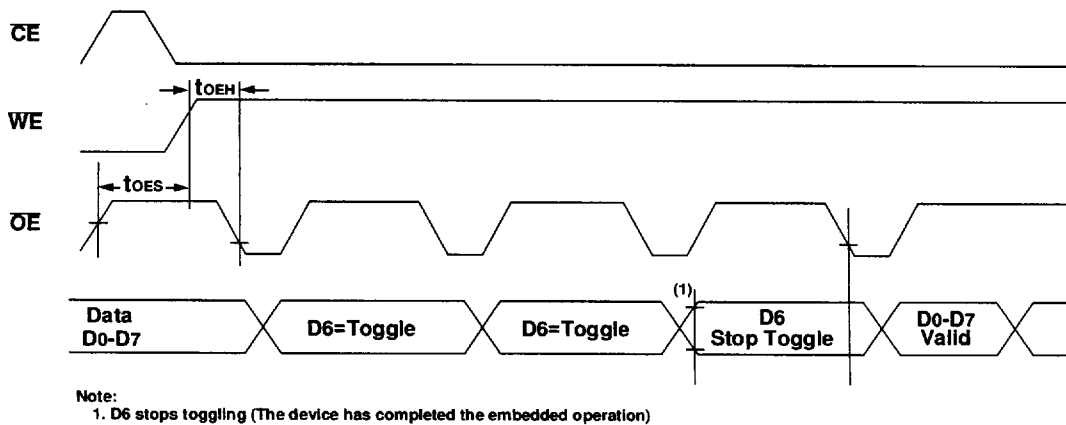
To activate this mode, the programming equipment must force V_{DD} on control pins $\overline{\text{OE}}$, $\overline{\text{CE}}$, and address pin A9. The address pins A6, A16, and A12 should be set to V_{IH} . The unprotection mechanism begins on the falling edge of the $\overline{\text{WE}}$ pulse and is terminated with the rising edge of the same.

It is also possible to determine if a sector is unprotected in the system by writing the autoselect command and A6 is set at V_{IH} . Performing a read operation at address location XXX2H, where the higher order addresses (A18, A17, and A16) define a particular sector address, will produce 00H at data outputs (D0-D7) for an unprotected sector.

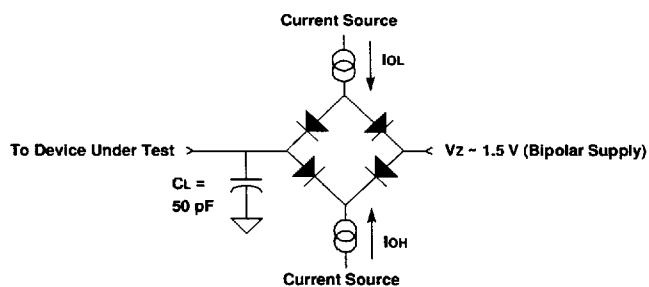
Table 4 — Hardware Sequence Flags

	Status	D7	D6	D5	D3	D2 – D0
In Progress	Auto-Programming	D7	Toggle	0	0	D
	Programming in Auto Erase	0	Toggle	0	1	
Exceeding Time Limits	Auto-Programming	D7	Toggle	1	1	D
	Programming in Auto Erase	0	Toggle	1	1	

**Figure 1
AC Waveforms for Toggle Bit During Embedded Algorithm Operations**



**Figure 2
AC Test Circuit**



Parameter	Typical	Units
Input Pulse Level	0 – 3.0	V
Input Rise and Fall	5	nS
Input and Output Timing Reference	1.5	V
Output Lead Capacitance	50	pF

Notes:

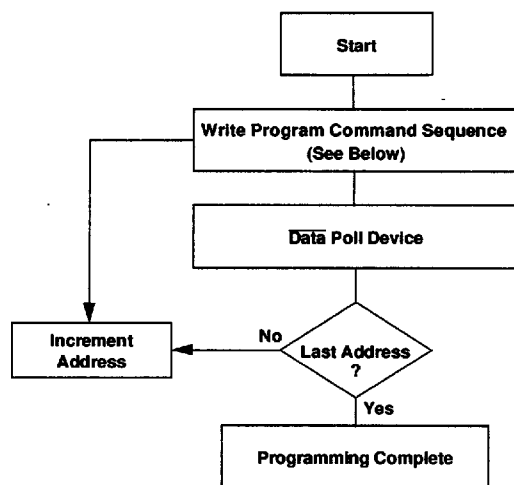
1) V_Z is programmable from -2V to +7V. 2) I_{OL} and I_{OH} programmable from 0 to 16 mA. 3) Tester Impedance $Z_0 = 75\Omega$. 4) V_Z is typically the midpoint of V_{OH} and V_{OL} . 5) I_{OL} and I_{OH} are adjusted to simulate a typical resistance load circuit. 6) ATE Tester includes jig capacitance.

Figure 3
Programming Algorithm

Bus Operations	Command Sequence	Comments
Standby ⁽¹⁾		
Write	Program	Valid Address/Data Sequence
Read		Data Polling to Verify Programming
Standby ⁽¹⁾		Compare Data Output to Data Expected

Note:

1. Device is either powered-down, erase or program inhibit.



Program Command Sequence (Address/Command):

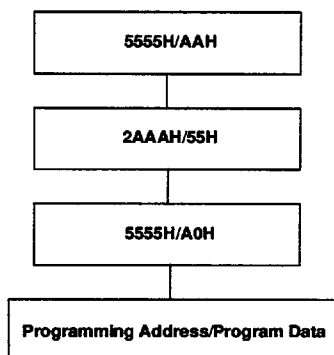
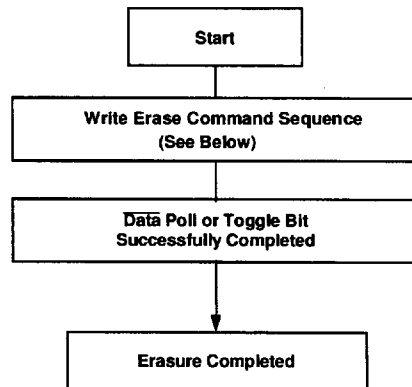
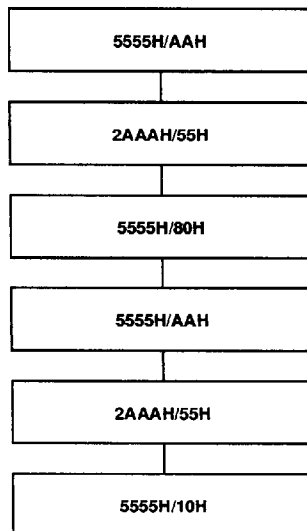


Figure 4
Erase Algorithm

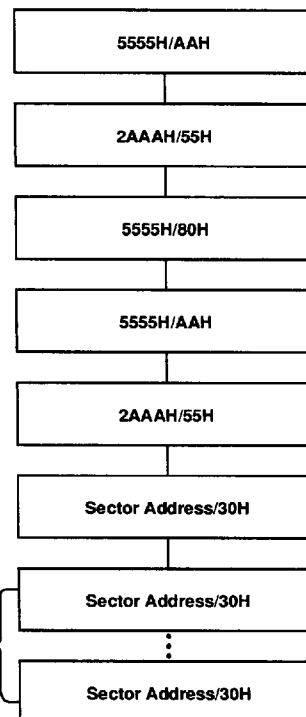
Bus Operations	Command Sequence	Comments
Standby		
Write	Erase	
Read		Data Polling to Verify Erasure
Standby		Compare Output to FFH



**Chip Erase Command Sequence
(Address/Command)**

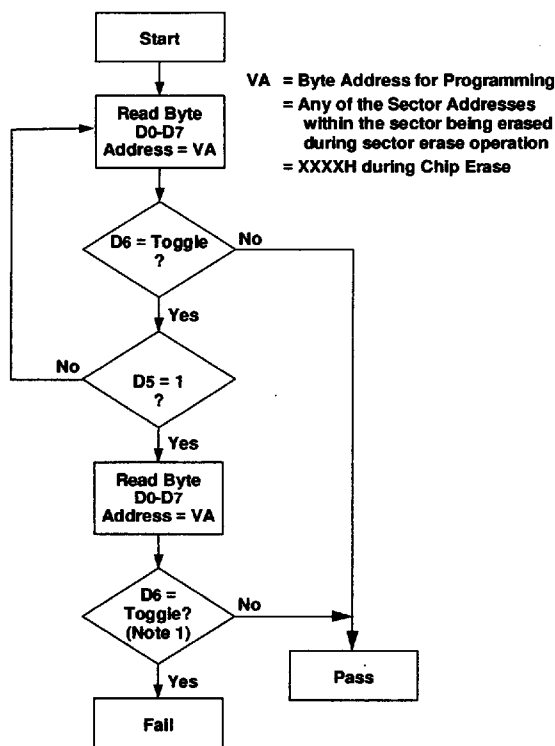


**Individual Sector/Multiple Sector
Erase Command Sequence
(Address/Command)**



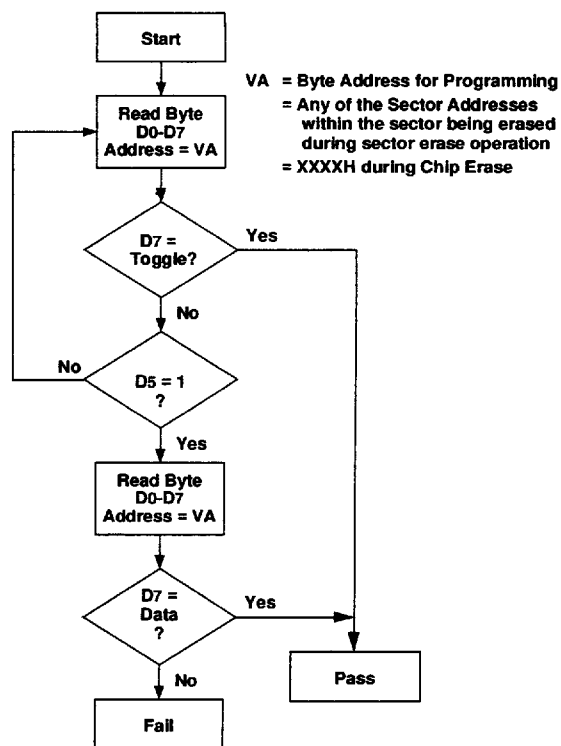
Additional Sector
Erase Commands
are Optional

Figure 5
Toggle Bit Algorithm



Note 1. D6 is rechecked even if D5 = "1" because D6 may stop toggling at the same time as D5 changes to "1".

Figure 6
Data Polling Algorithm



Note 1. D7 is rechecked even if D5 = "1" because D7 may change simultaneously with D5.

Figure 7
AC Waveforms for Read Operations

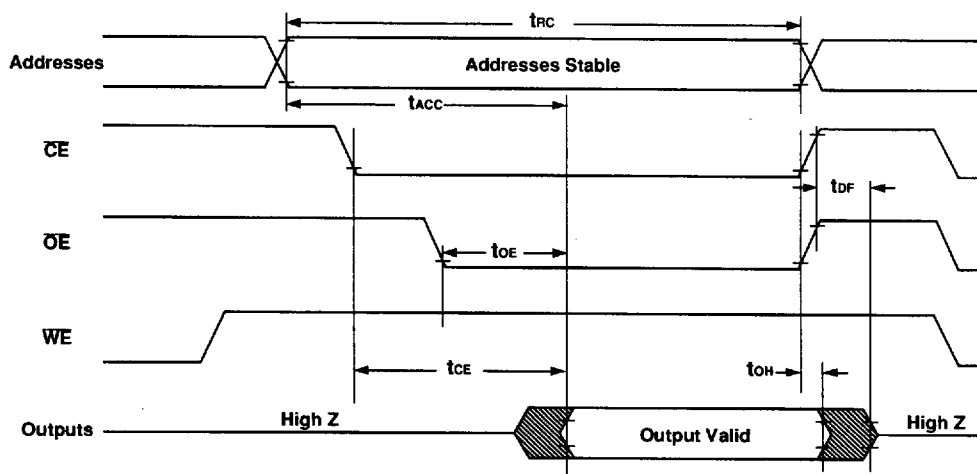
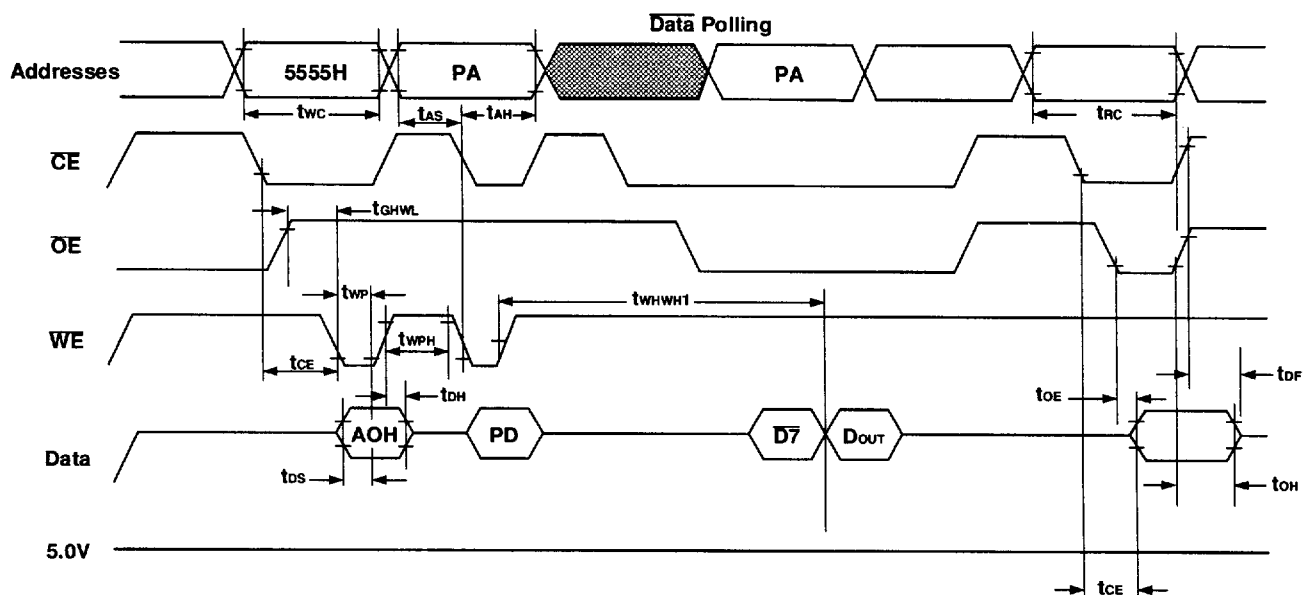


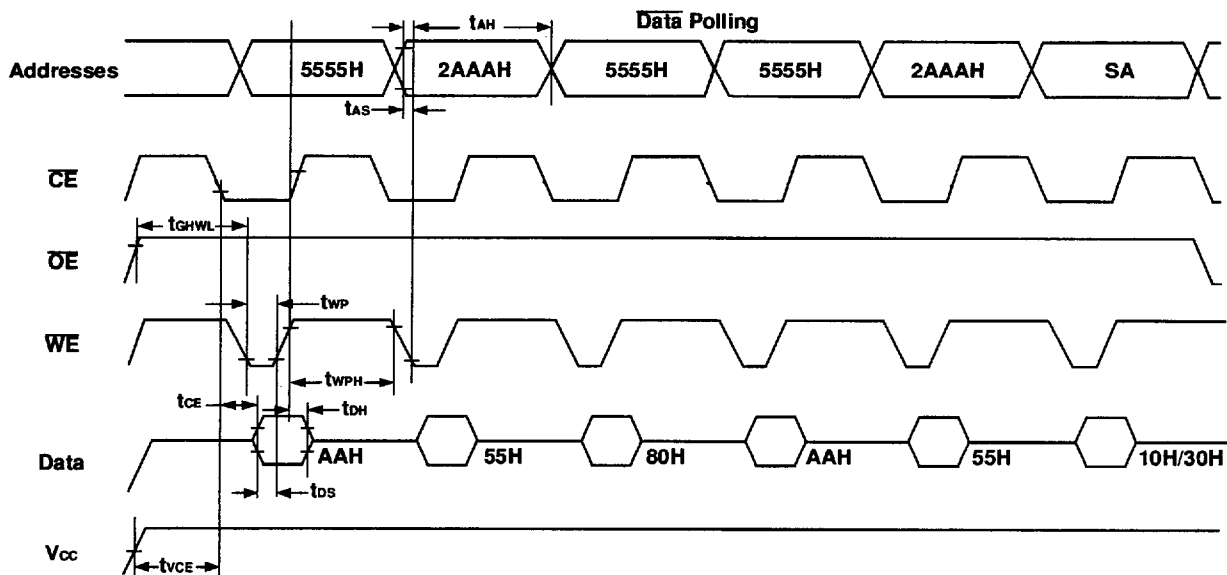
Figure 8
Write/Erase/Program Operation, WE Controlled



Notes:

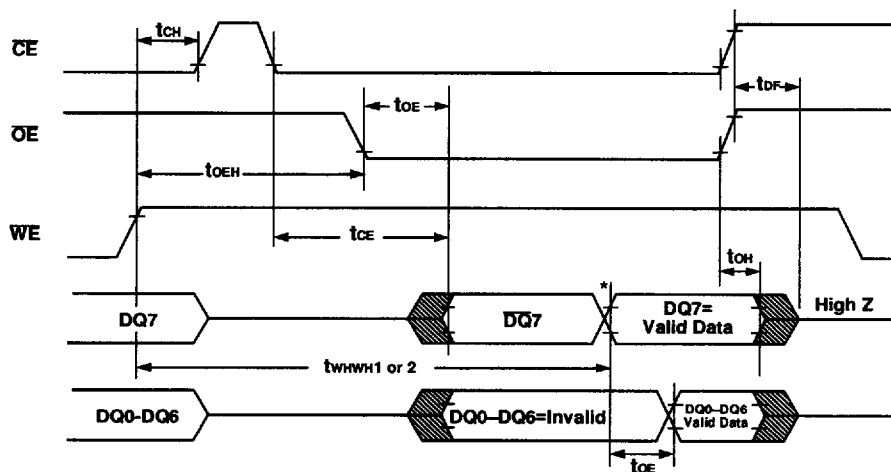
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. D7 is the Output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

Figure 9
AC Waveforms Chip/Sector
Erase Operations



Notes:
 1. SA is the sector address for sector erase.

Figure 10
AC Waveforms for Data Polling
During Embedded Algorithm Operations



* DQ7=Valid Data (The device has completed the Embedded operation).

Figure 11
Sector Protection Algorithm

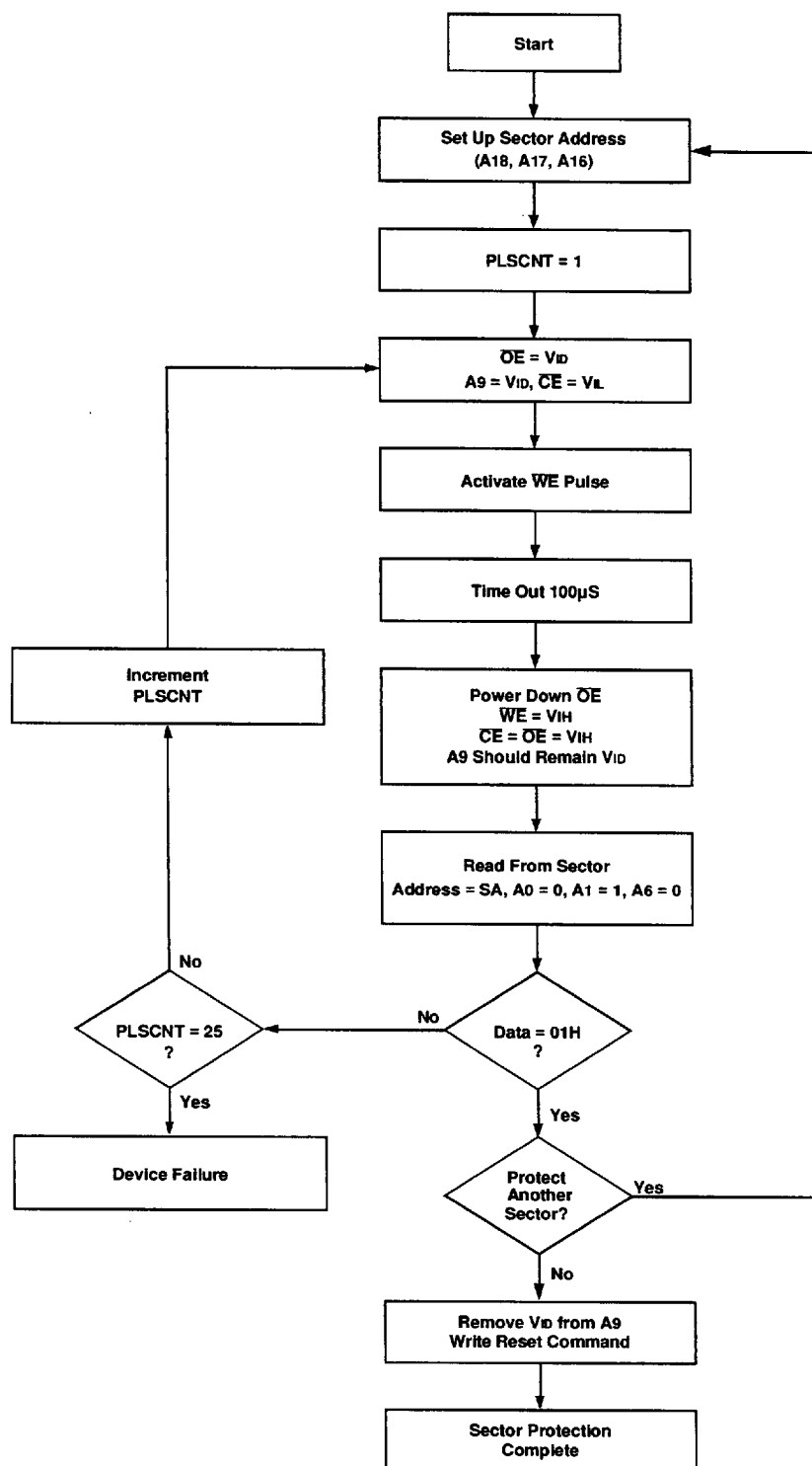
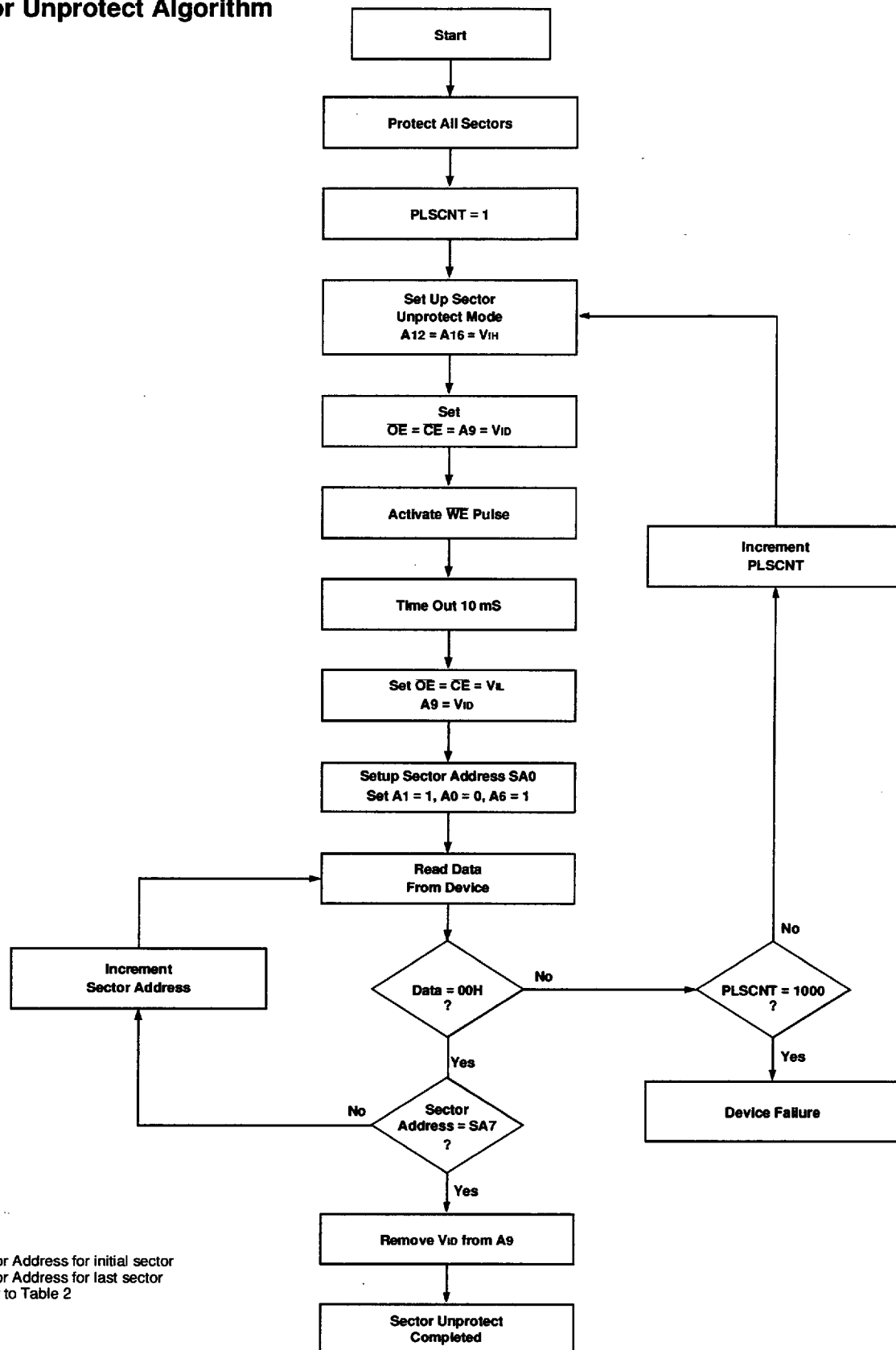
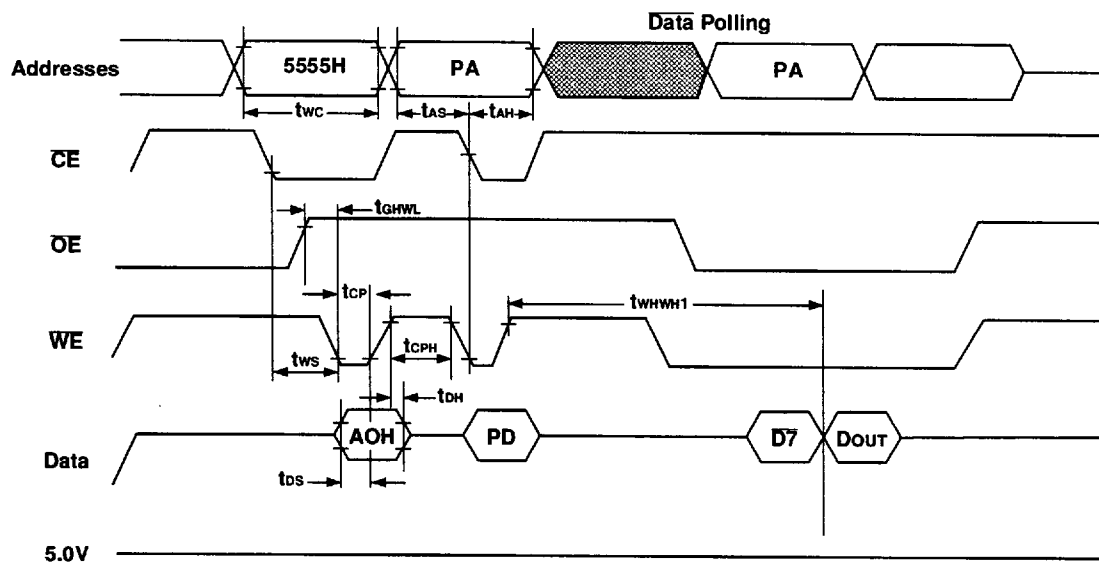


Figure 12
Sector Unprotect Algorithm



Notes:
SA0 = Sector Address for initial sector
SA7 = Sector Address for last sector
Please refer to Table 2

Figure 13
Alternate \overline{CE} Controlled Programming Operation Timings



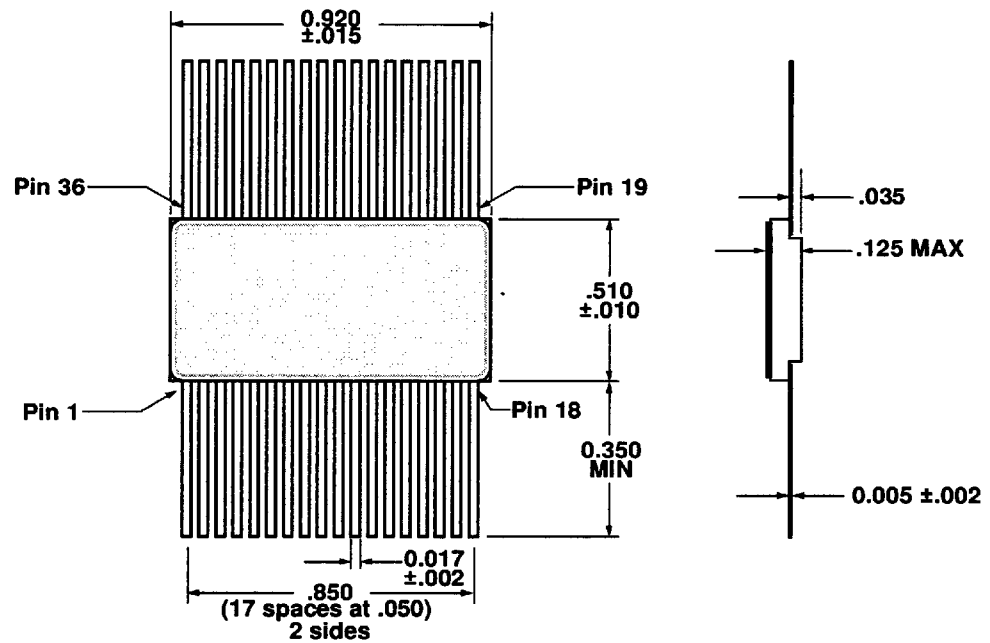
Notes:

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. D7 is the Output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

Pin Numbers & Functions

36 Pins — Flat Package			
Pin #	Function	Pin #	Function
1	NC	19	NC
2	A18	20	I/O3
3	A16	21	I/O4
4	A15	22	I/O5
5	A12	23	I/O6
6	A7	24	I/O7
7	A6	25	\overline{CS}
8	A5	26	A10
9	A4	27	\overline{OE}
10	A3	28	A11
11	A2	29	A9
12	A1	30	A8
13	A0	31	A13
14	I/O0	32	A14
15	I/O1	33	A17
16	I/O2	34	\overline{WE}
17	V _{ss}	35	V _{cc}
18	NC	36	NC

Package Outline "F3" — Small Flat Package

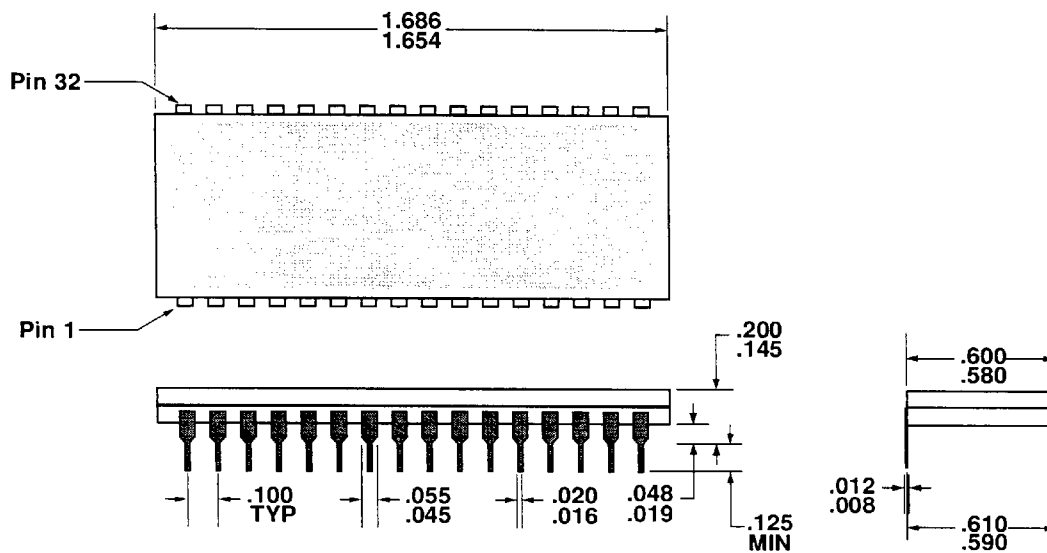


All dimensions in inches

Pin Numbers & Functions

32 Pins — DIP Package			
1	A18	17	I/O3
2	A16	18	I/O4
3	A15	19	I/O5
4	A12	20	I/O6
5\	A7	21	I/O7
6	A6	22	\overline{CS}
7	A5	23	A10
8	A4	24	\overline{OE}
9	A3	25	A11
10	A2	26	A9
11	A1	27	A8
12	A0	28	A13
13	I/O0	29	A14
14	I/O1	30	A17
15	I/O2	31	\overline{WE}
16	V _{SS}	32	V _{CC}

Package Outline "P4" — .590" x 1.67" DIP Package



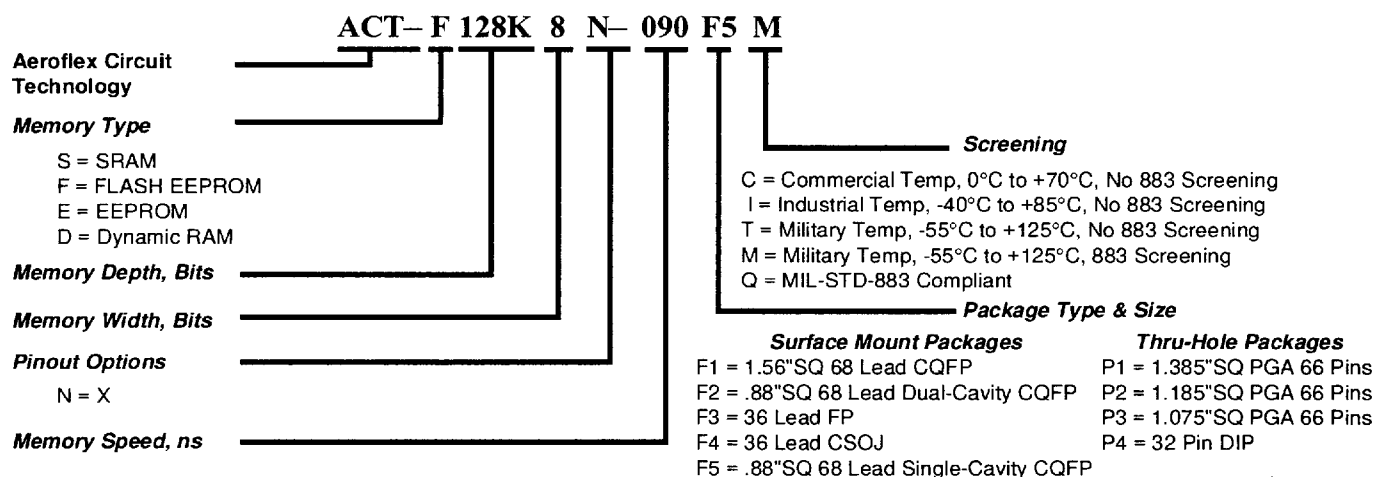
All dimensions in inches



Ordering Information

Model Number	DESC Drawing Number	Speed	Package
ACT-F512K8-090F3M	5962-TBD	90 nS	Flat Pack
ACT-F512K8-120F3M	5962-TBD	120 nS	Flat Pack
ACT-F512K8-150F3M	5962-TBD	150 nS	Flat Pack
ACT-F512K8-090P4M	5962-TBD	90 nS	DIP
ACT-F512K8-120P4M	5962-TBD	120 nS	DIP
ACT-F512K8-150P4M	5962-TBD	150 nS	DIP

Part Number Breakdown



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