Features

64Kx16 bit CMOS Static
Random Access Memory Module

- Access Times
  30 through 55ns
- Fully Static, No Clocks
- Inputs and Outputs Directly TTL Compatible

Jedec Approved Pinout

- 40 Pin DIP, No. 67

Single +5V (±10%) Supply Operation

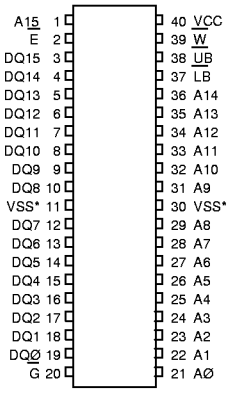
64Kx16 Static RAM CMOS, Module

The EDI8F1664C is a high speed 64Kx16 CMOS Static RAM Module consisting of four (4) 32Kx8 CMOS Static RAMs. The 32Kx8 RAMs are organized as two banks of 32Kx16 bits each. Functional equivalence to proposed monolithic mega-bit Static RAMs is achieved with an on-board decoder that interprets the higher order address (A15) to select one of the two banks as the x16 output, and using LB and UB as two extra chip select functions for Lower Byte (DQØ-DQ7) and Upper Byte (DQ8-DQ15) control, respectively.

All outputs and inputs are TTL-compatible and operate from a +5V supply. Fully asynchronous circuitry requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

Pin Configurations and Block Diagram

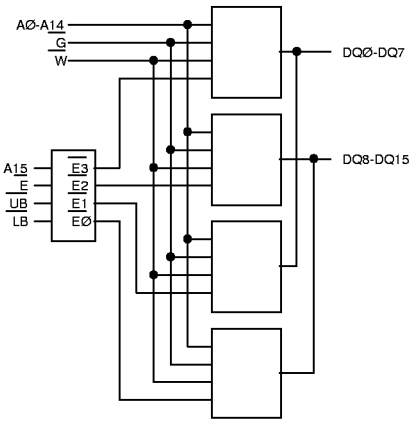
EDI8M1664
EDI8F1664



Pin Names

AØ-A15	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ15	Data Input/Output
$\overline{UB}$	Upper Byte Control
$\overline{LB}$	Lower Byte Control
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection

*Note: Both ground pins (VSS) need to be grounded for proper operation.



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Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0 ℃ to +70 ℃
Industrial	-40 ℃ to +85 ℃
Storage Temperature, Plastic	-55 ℃ to +125 ℃
Power Dissipation	4 Watts
Output Current.	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1TTL, CL = 50pF

(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current, x16 mode	ICC1	$\overline{W}$, $\overline{E}$, $\overline{LB}$, $\overline{UB}$ = VIL, II/O = 0mA, Min Cycle	--	250	425	mA
Operating Power Supply Current, x8 mode	ICC1	$\overline{W}$, $\overline{E}$ = VIL; $\overline{LB}$ or $\overline{UB}$ =VIL; II/O = 0mA, Min Cycle	--	125	195	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ • VIH or $\overline{LB}$ & $\overline{UB}$ • VIH	--	150	200	mA
Full Standby (CMOS) Power Supply Current	ICC3	$\overline{E}$ • VCC-0.2V or $\overline{LB}$ & $\overline{UB}$ • VCC-0.2V VIN • VCC-0.2V or VIN - 0.2V	--	5	80	mA
Input Leakage Current	ILI	VIN = 0V to VCC	--	--	±10	µA
Output Leakage Current	ILO	V I/O = 0V to VCC	--	--	±10	µA
Output High Voltage	VOH	IOH = -4.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL = +8.0mA	--	--	0.4	V

*Typical: TA = 25 ℃, VCC = 5.0V

Truth Table

$\overline{E}$	$\overline{UB}$	$\overline{LB}$	$\overline{W}$	$\overline{G}$	Mode	Output	Power
H	X	H	X	X	Standby	HIGH Z	ICC2, ICC3
L	H	H	X	X	Standby	HIGH Z	ICC2, ICC3
L	X	X	H	H	Read, Output Deselect	HIGH Z	ICC1
L	L	H	L	X	UB Write	DIN(8-15)	ICC1
L	H	L	L	X	LB Write	DIN(0-7)	ICC1
L	L	L	L	X	Write	DIN(0-15)	ICC1
L	L	H	H	L	UB Read	DOUT(8-15)	ICC1
L	H	L	H	L	LB Read	DOUT(0-7)	ICC1
L	L	L	H	L	Read	DOUT(0-15)	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Pins	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	$\overline{G}$,A	CI	35	pF
Capacitance Control (DQ Pins)	CD/Q	CD/Q	20	pF
Input Capacitance Control Lines	$\overline{E}$, $\overline{UB}$, $\overline{LB}$	CC	10	pF
Input Capacitance $\overline{W}$ Line	$\overline{W}$	CW	35	pF

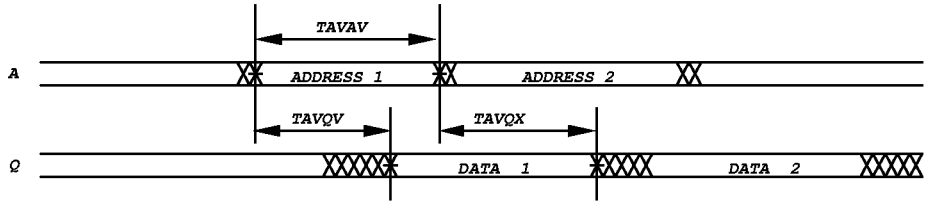
These parameters are sampled, not 100% tested.

AC Characteristics Read Cycle

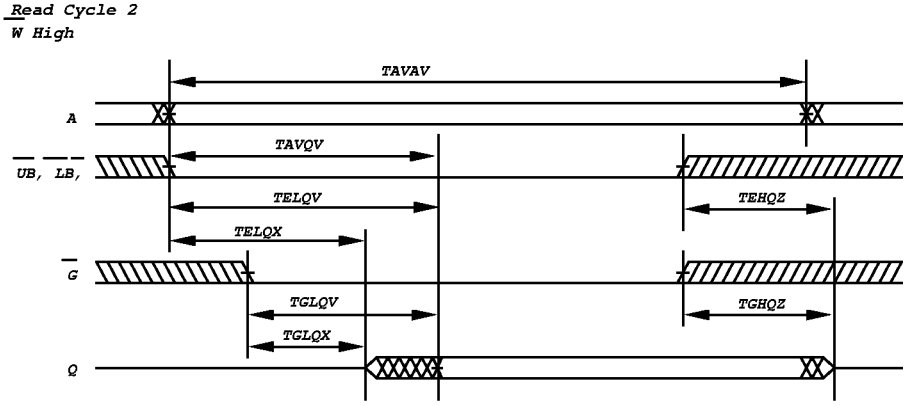
	Symbol		30ns		35ns		45ns		55ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Read Cycle Time	TAVAV	TRC	30		35		45		55		ns
Address Access Time	TAVQV	TAA		30		35		45		55	ns
Chip EnableAccess Time	TELQV	TACS		30		35		45		55	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	0		0		0		0		ns
Chip Enable to Output in High Z (1)	TEHQZ	TCHZ	0	20	0	20	0	20	0	20	ns
Output Hold from Address Change	TAVQX	TOH	5		5		5		5		ns
Output Enable to Output Valid	TGLQV	TOE		25		30		40		50	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		0		ns
Output Enable to Output in High Z (1)	TGHQZ	TOHZ	0	20	0	20	0	20	0	20	ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1 - $\overline{W}$ High, $\overline{G}$, $\overline{E}$ Low



Read Cycle 2 - $\overline{W}$ High

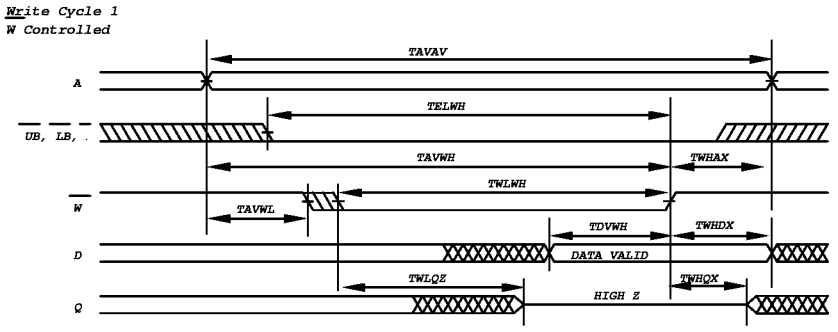


AC Characteristics Write Cycle

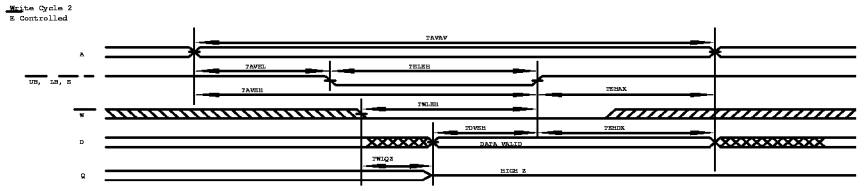
	Symbol		30ns		35ns		45ns		55ns		
Parameter	**Symbol**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Write Cycle Time	TAVAV	TWC	30		35		45		55		ns
Chip Enable to End of Write	TWLWH	TCW	25		30		40		50		ns
	TWLEH	TCW	25		30		40		50		ns
Address Setup Time	TAVWL	TAS	0		0		0		0		ns
	TAVEL	TAS	0		0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	25		30		40		50		ns
	TAVEH	TAW	25		30		40		50		ns
Write Pulse Width	TWLWH	TWP	25		30		40		50		ns
	TELEH	TWP	25		30		40		50		ns
Write Recovery Time	TWHAX	TWR	5		5		5		5		ns
	TEHAX	TWR	5		5		5		5		ns
Data Hold Time	TWHDX	TDH	5		5		5		5		ns
	TEHDX	TDH	5		5		5		5		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	15	0	15	0	15	0	15	ns
Data to Write Time	TDVWH	TDW	25		30		40		50		ns
	TDVEH	TDW	25		30		40		50		ns
Output Active from End of Write (1)	TWHQX	TWLZ	5		5		5		5		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1 - $\overline{W}$ Controlled



Write Cycle 2 - $\overline{E}$ Controlled



Ordering Information

Part Number	Speed (ns)	Package No.
EDI8F1664C30M6C	30	67
EDI8F1664C35M6C	35	67
EDI8F1664C45M6C	45	67
EDI8F1664C55M6C	55	67

Package Description

Package No. 67
40 Pin Module