Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 64K (16K x 4-BIT) with CONDITIONAL WRITE

ADVANCE INFORMATION
IDT10498
IDT100498
IDT101498

FEATURES:

- 16,384-words x 4-bit organization
- Address access time: 12/15ns
- Read Data output latch for extended hold time
- Short Write Cycle input data and address valid time
- Write Cycle may be terminated very late in the cycle
- Pin compatible with standard 16K x 4
- Through-hole DIP and surface-mount packages

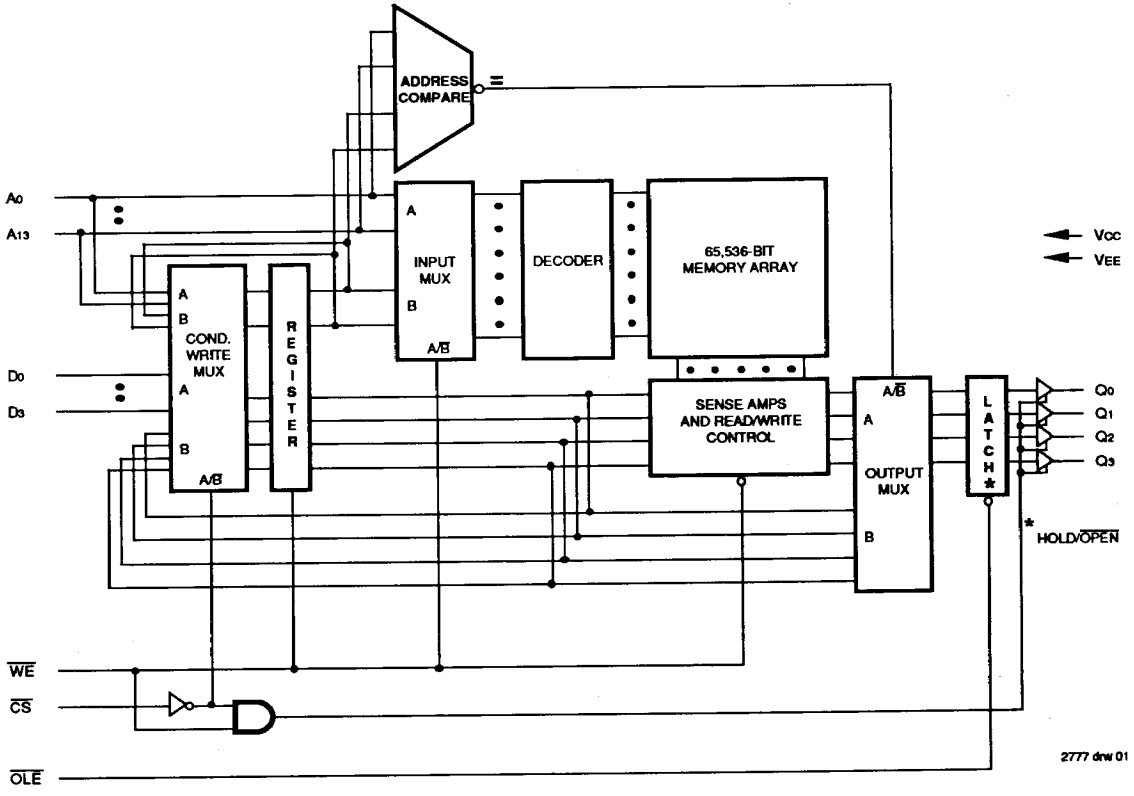
DESCRIPTION:

The IDT10498, IDT100498 and IDT101498 are 65,536-bit high-speed BiCEMOS™ ECL static random access memories organized as 16K x 4, with inputs and outputs fully compatible with ECL levels. Internal registers on inputs provide enhanced Write Cycle performance over conventional RAMs, while output read data latch allows longer output data hold time providing easier design and improved system level cycle times.

In the read mode, this device is pinout and timing compatible with the standard asynchronous SRAMs (IDT10494), yet the addition of an output latch with separate enable control allow output data to be captured and held long into the next cycle. This minimizes noise on the data bus and provides better set-up time margin for the next logic stage in pipelined applications.

In the write mode, the device adds an invisible pipeline stage in the write address and data paths, allowing very short set-up and hold times for these inputs and less stringent requirements for the write pulse input. Additionally, the address and data paths to the input register are gated by the Conditional Write Multiplexor, which allows termination of a Write cycle late in the cycle.

FUNCTIONAL BLOCK DIAGRAM



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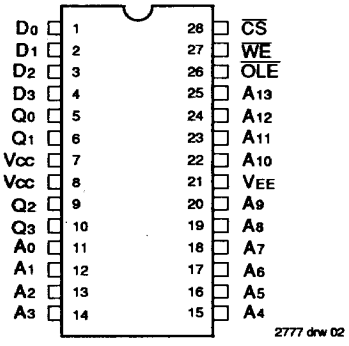
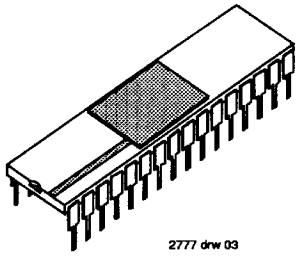
COMMERCIAL TEMPERATURE RANGE **SEPTEMBER 1990**

DSC-8012/1
1

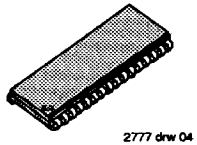
PIN CONFIGURATION



TOP VIEW



400-Mil-Wide
CERAMIC PACKAGE
C32



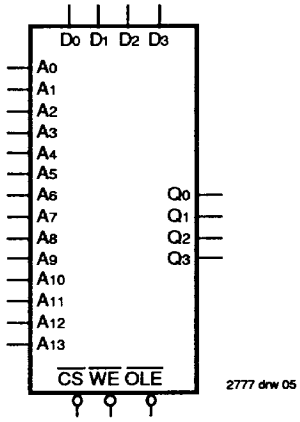
300-Mil-Wide
PLASTIC SOJ PACKAGE
Y32

PIN DESCRIPTIONS

Symbol	Pin Name
A0 through A13	Address Inputs
D0 through D3	Data Inputs
Q0 through Q3	Data Outputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input (Internal pull down)
$\overline{OLE}$	Output Latch Enable
VEE	More Negative Supply Voltage
VCC	Less Negative Supply Voltage

2777 tbl 01

LOGIC SYMBOL



16Kx4
SRAM

AC OPERATING RANGES(1)

I/O	VEE	Temperature
10K	-5.2V ±5%	0 TO 75°C, air flow exceeding 2 m/sed
100K	-4.5V ±5%	0 TO 85°C, air flow exceeding 2 m/sed
101K	-4.75V to -5.46V	0 TO 75°C, air flow exceeding 2 m/sed

2777 tbl 02

NOTE:
1. Referenced to VCC

CAPACITANCE (TA=+25°C, f=1.0MHz)

Symbol	Parameter	DIP Typ.	DIP Max.	SOJ Typ.	SOJ Max.	Unit
CIN	Input Capacitance	4	–	3	–	pF
COUT	Output Capacitance	6	–	3	–	pF

2777 tbl 03

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	$\overline{OLE}$	Data OUT (2)	Function
H	X	X	L	Deselected
L	H	L	RAM Data	Read
L	H	H	RAM Data	Output Held
L	L	X	L	Write

2777 tbl 04

NOTES:
1. H=High, L=Low, X=Don't Care
2. DATAOUT initiated by falling edge of $\overline{OLE}$.

ECL-10K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2777 tbl 05

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions

ECL-10K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L =50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit	T_A
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA	–
			Others	–	–	110	µA	–
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA	–
			Others	-50	–	90	µA	–
I_{EE}	Supply Current	All Inputs and Outputs Open		-260	-200	–	mA	–

2777 tbl 06

NOTE:
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

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ECL-100K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to + 85	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2777 tbl 07

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-100K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.5V, R_L =50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	V_{IN} = V_{IHB} or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	V_{IN} = V_{IHB} or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	V_{IN} = V_{IHA}	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	V_{IN} = V_{ILB}	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-240	-180	–	mA

2777 tbl 08

NOTE:
1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.

ECL-101K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2778 tbl 09

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-101K DC ELECTRICAL CHARACTERISTICS

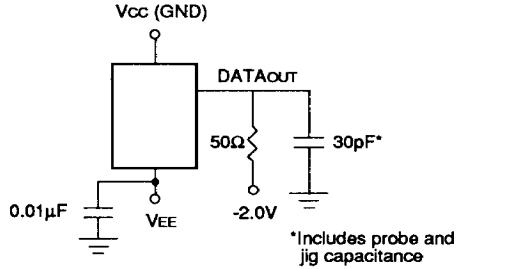
(V_{EE} = -5.2V, R_L =50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Condition		Min. (B)	Typ.(1)	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-260	-200	–	mA

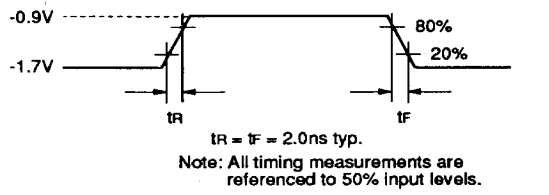
2778 tbl 10

NOTE:
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

AC TEST LOAD CONDITION



AC TEST INPUT PULSE



RISE/FALL TIME

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_R	Output Rise Time	–	–	2	–	ns
t_F	Output Fall Time	–	–	2	–	ns

2779 tbl 11

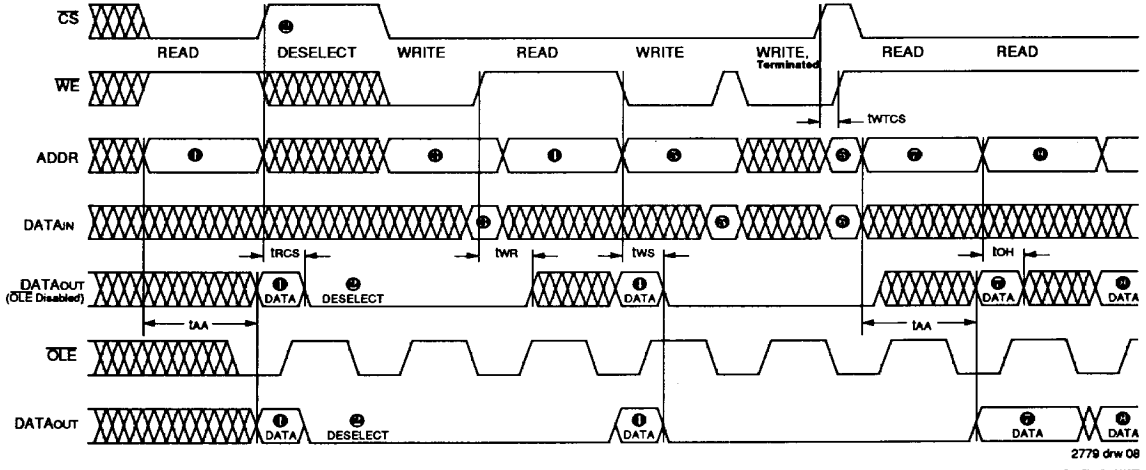
FUNCTIONAL DESCRIPTION

The IDT10498, IDT100498, and IDT101498 BiCMOS ECL static RAMs (SRAM) with CONDITIONAL WRITE provide high speed with low power dissipation typical of BiCMOS ECL. On-chip logic additionally helps improve system performance, yet the device is pinout-compatible with asynchronous equivalents (i.e... IDT10494, IDT100494, and IDT101494 respectively). The ECL-101K meets electrical specifications that combine the ECL-100K temperature and voltage compensated output levels with the high-speed of ECL-10K VEE compatibility (-5.2V).

As can be seen in the Functional Block Diagram on the title page, this device contains clocked input registers to sample and hold addresses and input data, during a write cycle only. Inputs are sampled on the rising edge of the Write Enable ($\overline{WE}$). The write cycle is pipelined: the memory cell is written during the $\overline{WE}$-low time in the next cycle. Additionally, the address and data paths to the input register are gated by the Conditional Write Multiplexor, which allows termination of a Write cycle late in the cycle.

Read cycles are not pipelined and operate identically to an asynchronous device, except that an output latch is provided to capture and hold Read data.

FUNCTIONAL DESCRIPTION TIMING EXAMPLE



READ TIMING

The read timing on the device is asynchronous. DataOUT is held low until the device is selected by Chip Select ($\overline{CS}$). Then Address (ADDR) settles and data appears on the output after time t_{AA}, as at ❶ below.

DataOUT is held for a short time (t_{OH}) after the address begins to change for the next access, as can be seen at ❼ — allowing addresses to begin to change early for the next cycle — then ambiguous data is on the bus until a new time t_{AA}.

To avoid this noise on the bus and provide for longer output hold time, this device includes an output Read data latch which allows Read data to flow out while Output Latch Enable ($\overline{OLE}$) is low, and then hold when $\overline{OLE}$ is high. Thus in the example below Read data at ❼ is held until Read data at ❽ is ready for output.

Note that DataOUT is disabled (held low) by $\overline{CS}$ high or $\overline{WE}$ low, regardless of the state of the Output Latch.

DESELECT TIMING

Deselect timing is identical to a standard asynchronous device. This case occurs at ❷ below. Outputs attain the disable state (low) t_{RCS} later Chip Select ($\overline{CS}$) is taken to a high logic state. Status of other inputs do not effect the disabling of the device when chip select is de-asserted.

WRITE TIMING

Write cycles pipelined to allow easier design and higher system performance. The write pulse created on the $\overline{WE}$ input is used as a strobe to clock in the Write Address and Data into a register. This address and data are held in the register until the next write cycle, when they are used to write into the memory array through the Input Multiplexor.

Note the very short valid window required for Write Address and Data inputs. This is because these signals are captured by the input register. This means that input data may arrive late in the cycle, as at ❸ below, or data and address may arrive late, as at ❻ below.

DataOUT is disabled during the Write Cycle. If $\overline{CS}$ is held low (active) and addresses remain unchanged, the DataOUT pins will output the written data after "Write Recovery Time" (t_{WR}), as for a standard asynchronous device.

There is a special case when a Read cycle follows directly a Write Cycle to the same address. The memory array has not yet been updated with the Write data — it is still in the input register. This case is handled by including an address comparator and Output Multiplexor on the device: if the address being presented on the input pins is the same as the address stored in the input register, the data presented to the output pins is also from the input register.

CONDITIONAL WRITE

In certain system architectures, the decision whether to write data within a cycle occurs late in the cycle. An example might be cache hit logic taking time to decide if a cache line needs to be updated. This device allows a write to be initiated, yet terminated very late in the cycle by using Chip Select should a write not be required by the system.

The Conditional Write Multiplexor controlled by Chip Select makes this possible. In a normal Write cycle, $\overline{CS}$ is low and the Multiplexor delivers the state of the addresses and data on the input pins to the Input Multiplexor and Input Register, respectively. Because $\overline{CS}$ does not gate the Write Pulse logic, it has a short valid window requirement.

To terminate the Write cycle, as shown at ❹ below, all that is required is to bring $\overline{CS}$ to a high logic state. This switches the Conditional Write Multiplexor to circulate the previously written address and data (held in the Input Register) around to be clocked again into the Input Register. No Write cycle is apparent to the system.

5

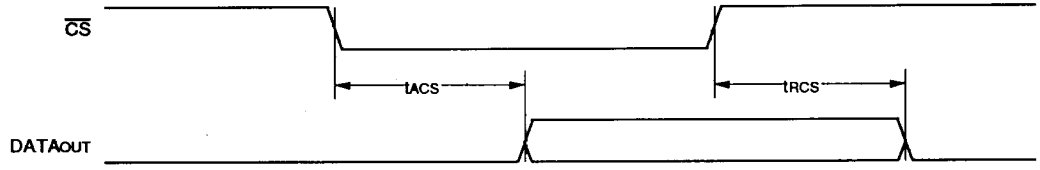
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10498S12 100498S12 101498S12 Min.	10498S12 100498S12 101498S12 Max.	10498S15 100498S15 101498S15 Min.	10498S15 100498S15 101498S15 Max.	Unit
Read Cycle							
t_{AA}[2]	Address Access Time	–	–	12	–	15	ns
t_{ACS}	Chip Select Access Time	–	–	5	–	5	ns
t_{RCS}	Chip Select Recovery Time	–	–	5	–	5	ns
t_{OH}	Data Hold from Address Change	–	3	–	3	–	ns
t_{OLEL}	Latch Enable Low Pulse Width	–	5	–	5	–	ns
t_{AHO}	Address Valid to $\overline{OLE}$ High	–	14	–	17	–	ns
t_{DH}	Data Hold from Clock Low	–	0	–	0	–	ns
t_{DR}	Data Ready from Clock Low	–	0	4	0	4	ns

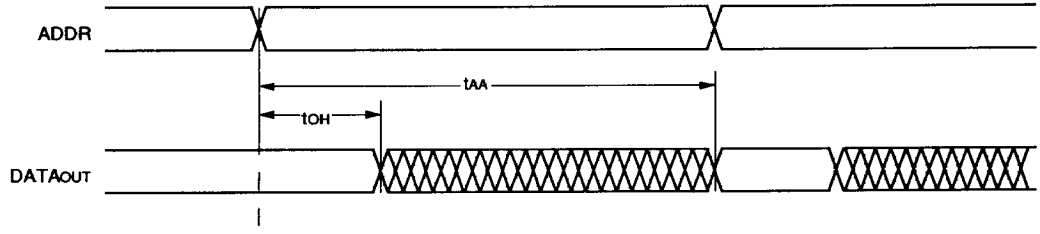
2779 tbl 12

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. Read Data is valid at t_{AA} or t_{AHO} - t_{OLEL} + t_{DR}, whichever is larger; that is, Read Data is valid at the access time unless Output Latch Enable is high, and then access is t_{DR} after $\overline{OLE}$ goes low.

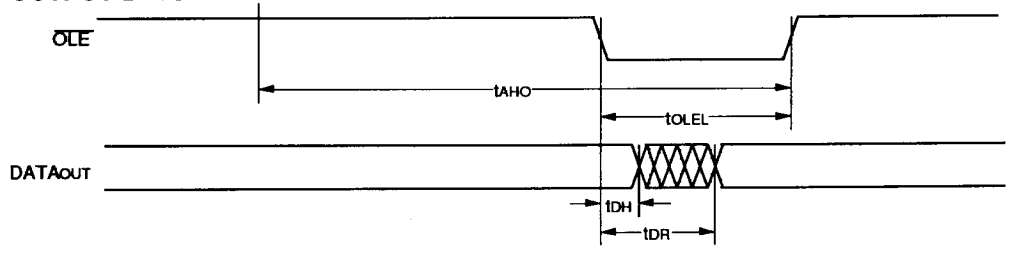
READ CYCLE GATED BY CHIP SELECT



READ CYCLE GATED BY ADDRESS



OUTPUT LATCH TIMING



2779 drw 09

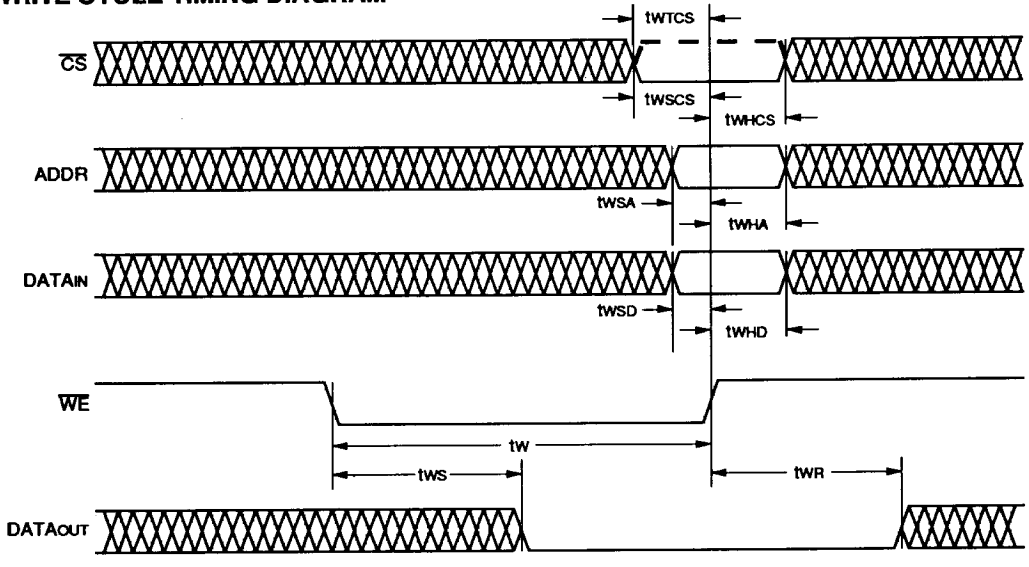
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10498S12 100498S12 101498S12		10498S15 100498S15 101498S15		Unit
			Min.	Max.	Min.	Max.	
Write Cycle							
tW	Write Pulse Width	–	10	–	12	–	ns
tWSCS	Setup Time for Chip Select	–	1	–	1	–	ns
tWTCS	$\overline{CS}$ Set-Up, Terminated Write	–	2	–	2	–	ns
tWSA	Setup Time for Address	–	1	–	1	–	ns
tWSD	Setup Time for Data In	–	1	–	1	–	ns
tWHCS	Hold Time for Chip Select	–	2	–	2	–	ns
tWHA	Hold Time for Address	–	2	–	2	–	ns
tWHD	Hold Time for Data In	–	2	–	2	–	ns
tWS	Write Disable Time	–	–	5	–	5	ns
tWR	Write Recovery Time	–	–	5	–	5	ns

2779 tbl 13

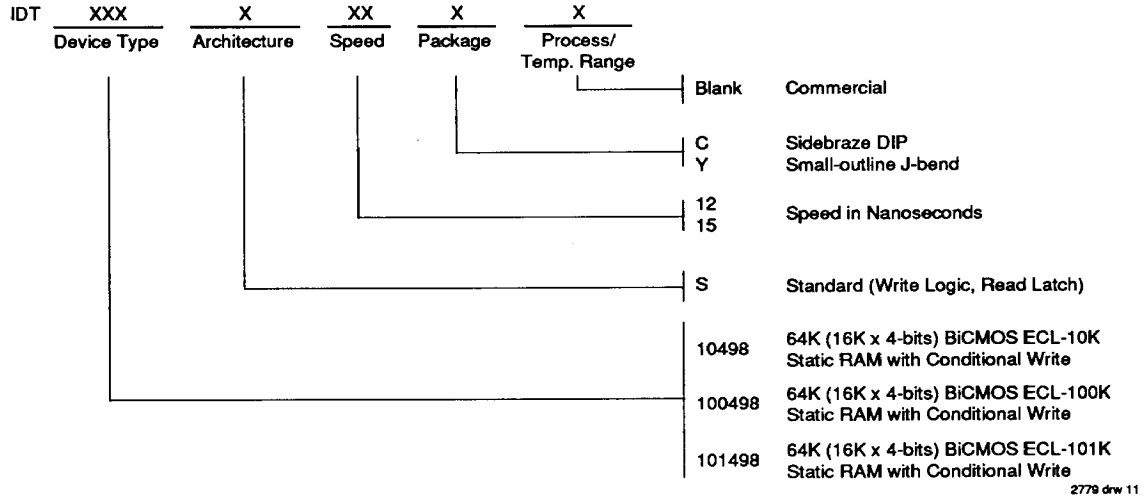
NOTES:
1. Input and Output reference level is 50% point of waveform.

WRITE CYCLE TIMING DIAGRAM



2779 drw 10

ORDERING INFORMATION



2779 drw 11