National Semiconductor

PRELIMINARY

NMC9817 16,384-Bit (2k x 8) E²PROM

General Description

The NMC9817 is a fast 5V-only E²PROM which offers many desired features, making it ideally suited for efficiency and ease in system design. The added features on the NMC9817 include: 5V-only operation provided by an on-chip V_{PP} generator during erase-write; address and data latches to reduce part count and to free the microprocessor while the chip is busy during erase-write; 'Ready' line indicator to indicate status of chip to the microprocessor; and automatic erase before byte-write. It can meet applications requiring up to 10^4 write cycles per byte. The NMC9817 is a product of National's advanced E²PROM stepper technology and uses the powerful XMOS™ process for reliable, non-volatile data storage.

The NMC9817 sharply minimizes the interfacing hardware logic and firmware required to perform data writes. The device has complete self-timing which leaves the processor free to perform other tasks until the NMC9817 signals 'ready'. With an automatic erase before write, the user benefits by saving an erase command contributing to efficient usage of system processing time. On-chip address and data latching further enhances system performance.

The NMC9817's very fast read access times make it compatible with high performance microprocessor applications. It uses the proven two line control architecture which eliminates bus contention in a system environment. Combining these features with the NMC9817's open-drain 'Ready' signal makes the device an extremely powerful, yet simple to use, E²PROM memory.

The density, and level of integrated control, make the NMC9817 suitable for users requiring minimum hardware overhead, high system performance, minimal board space and design ease. Designing with and using the NMC9817 is extremely cost effective as the required high voltage and interfacing hardware required for other E²PROM devices has been eliminated by 5V-only operation and on-chip latches. See *Figures 1*, *2* and *3* for the NMC9817 block diagram, pinout, and simple interface requirements.

Features

- Single 5V supply (eliminates an external 21V V_{PP})
- Self-timed byte-write with auto erase
- No external capacitor or pulse shaping circuits
- On-chip address and data latches
- Two line output control
- TRI-STATE® outputs
- RDY pin indicator
- Fast byte-writing
  Write cycle (2 ms typical)
  E/W cycle (4 ms typical)
- Very fast access times
  NMC9817-20—200 ns
  NMC9817-25—250 ns
  NMC9817-35—350 ns
- Direct microprocessor interface capability
- No support components needed
- Reliable E²PROM XMOS stepper technology

Block and Connection Diagrams

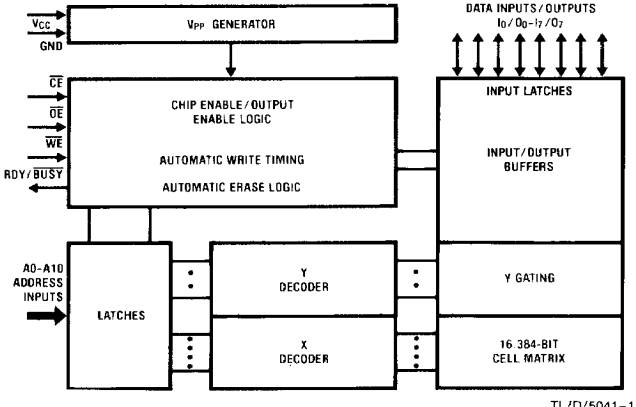

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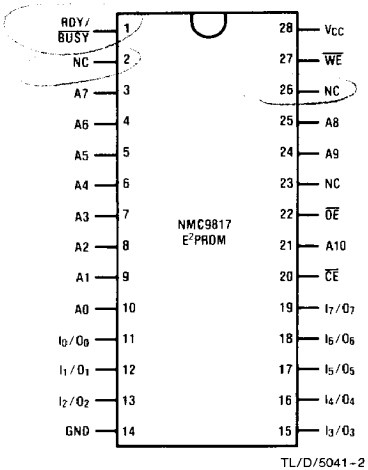
FIGURE 1

Pin Names

A0–A10	Addresses	I_0–I_7	Data Inputs
$\overline{CE}$	Chip Enable	RDY/$\overline{BUSY}$	Device Ready/Busy (Open-Drain Output)
$\overline{OE}$	Output Enable	NC	No Connect
O_0–O_7	Data Outputs		

Dual-In-Line Package



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Top View
FIGURE 2

Order Number NMC9817J-20, NMC9817J-25 or NMC9817-35
See NS Package Number J28A

Absolute Maximum Ratings

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input or Output Voltages with Respect to Ground	+6V to −0.3V
Lead Temp. (Soldering, 10 seconds)	300°C

Operating Conditions

Temperature Range	0°C to +70°C
V_{CC} Power Supply (Notes 2 and 3)	5V ±5%

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics $T_A = 0°C$ to 70°C, $V_{CC} = 5V \pm 5\%$ (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
READ OPERATION						
I_{LI}	Input Leakage Current	$V_{IN} = 5.25V$			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.25V$			10	μA
I_{CCA}	V_{CC} Current (Active)	$\overline{OE} = \overline{CE} = V_{IL}$		40	80	mA
I_{CCS}	V_{CC} Current (Standby)	$\overline{CE} = V_{IH}$		12	25	mA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC}+1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ μA	2.4			V
WRITE OPERATION						
I_{CCW}	V_{CC} Current (Write)	$RDY/\overline{BUSY} = V_{OL}$		40	80	mA

Capacitance $T_A = 25°C$, f = 1 MHz (Note 1)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$		5	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$			10	pF

AC Test Conditions

Output Load	1 TTL gate and $C_L = 100$ pF
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Read Mode AC Electrical Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ (Notes 2 and 3)

Symbol	Parameter	Conditions	NMC9817-20			NMC9817-25			NMC9817-35			Units
			Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150	200		200	250		300	350	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150	200		200	250		300	350	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	10		75	10		100	10		120	ns
t_{DF}	Output Disable to Output Float	$\overline{CE}$ or $\overline{OE} = V_{IL}$	0		80	0		100	0		100	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE}$, $\overline{OE} = V_{IL}$	0			0			0			ns

Write Mode AC Electrical Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
t_{AS}	Address to Write Set-Up Time		20			ns
t_{CS}	$\overline{CE}$ to Write Set-Up Time (Note 5)		20			ns
t_{WP}	Write Pulse Width		100			ns
t_{AH}	Address Hold Time		50			ns
t_{DS}	Data Set-Up Time	$\overline{OE} = V_{IH}$	50			ns
t_{DH}	Data Hold Time	$\overline{OE} = V_{IH}$	20			ns
t_{CH}	$\overline{CE}$ Hold Time		20			ns
t_{DB}	Time to Device Busy				120	ns
t_{WR}	Byte-Write Cycle Time			4	10	ms

Note 1: This parameter only sampled and not 100% tested.

Note 2: To prevent spurious device erase or write, $\overline{WE}$ or $\overline{CE} = V_{IH}$ must be applied simultaneously or before application of V_{CC}. $\overline{WE}$ or $\overline{CE} = V_{IH}$ must be removed simultaneously or after V_{CC}.

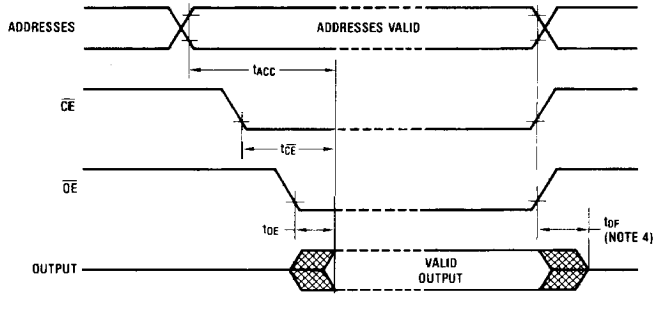
Note 3: To prevent damage to the device it must not be inserted into or removed from a board with power applied.

Note 4: t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Note 5: T_{CS} = 35 ns on −25 and −35 devices.

Switching Time Waveforms

Read



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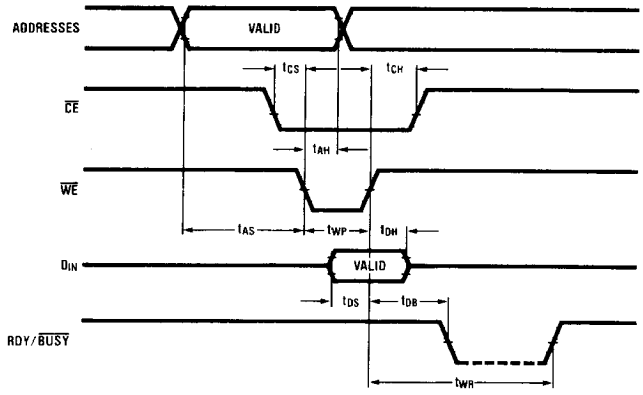
Switching Time Waveforms (Continued)

Write



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Device Operation

The NMC9817 has 4 modes of user operation which are detailed in Table 1. All modes are designed to enhance the NMC9817's functionality to the user and provide total microprocessor compatibility.

TABLE I. V_{CC} = 5V

Pin Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$I_0/O_0-I_7/O_7$	RDY/$\overline{BUSY}$
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Hi-Z
Standby	V_{IH}	X	X	Hi-Z	Hi-Z
Write	V_{IL}	V_{IH}	⊓	D_{IN}	V_{OL}
Busy	X	X	X	Hi-Z	V_{OL}

WRITE MODE

The NMC9817 is programmed electrically in-circuit, yet it provides the non-volatility usually obtained by optical erasure in EPROMS and by batteries with CMOS RAM. Writing to non-volatile memory has never been easier as no high voltage, external latching, erasing or timing is needed. When commanded to byte-write, the NMC9817 automatically latches the address, data, and control signals and starts the write cycle. Concurrently, the 'Ready' line goes low, indicating that the NMC9817 is busy and that it can be deselected to allow the processor to perform other tasks. The Ready/$\overline{Busy}$ signal is an open-drain output. During the write, a high V_{PP} is generated on-chip to perform an automatic byte-erase, then write.

As a precaution against spurious signals which may cause an inadvertant write cycle, or interfere with a valid signal, it is recommended that a pullup resistor be used on the $\overline{WE}$ pin, pin 27 (see *Figure 4*).

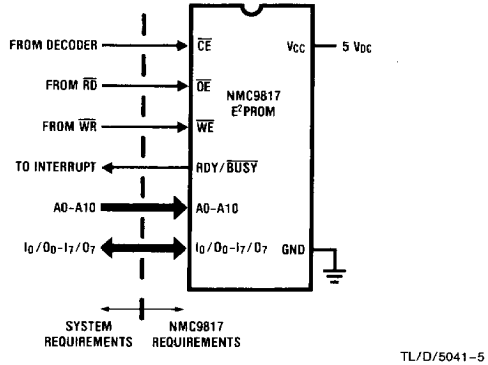

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FIGURE 3. Simple NMC9817 Interface Requirements

Device Operation (Continued)

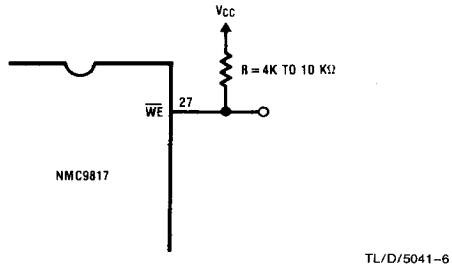

FIGURE 4. Pullup R on $\overline{WE}$

READ MODE

One aspect of the NMC9817's high performance is its very fast read access time—typically less than 200 ns. Its read cycle is similar to that of EPROMS and static RAMs. It offers a two line control architecture to eliminate bus contention. The NMC9817 can be selected using decoded system address lines to $\overline{CE}$ and then the device can be read, within the device selection time, using the processor's $\overline{RD}$ signal connected to $\overline{OE}$.

STANDBY MODE

The NMC9817 has a standby mode in which power consumption is reduced by 70%. This offers the user power supply cost benefits when designing a system with NMC9817s. This mode occurs when the device is deselected ($\overline{CE} = V_{IH}$). The data pins are put into the high impedance state regardless of the signals applied to $\overline{OE}$ and $\overline{WE}$ concurrent with the reading and writing of other devices.

SYSTEM IMPLEMENTATION AND APPLICATION

The NMC9817 is compatible with industry standard microprocessors. It requires no interface circuitry and no support circuitry.

The NMC9817 is ideal for non-volatile memory requirements in applications requiring storage of user defined functions, calibration constants, configuration parameters and accumulated totals. Soft key configuration in a graphics terminal is an example where user defined functions, such as protocol, color, margins and character fonts can be keyed in by the user. Calibration constants could be stored by the NMC9817 in the smart interface for a robot's axis of movement. Movement constants, compensation algorithms and learned axis characteristics can be stored. In programmable controllers and data loggers, configuration parameters for polling time, sequence and location, could be stored in the NMC9817. Accumulated totals for dollars, energy consumption, volume and even the logging of service done on computer boards or systems can be stored in the NMC9817.

The NMC9817 is cost effective for lower density E²PROM applications and can therefore be used to provide a lower system cost to the user compared to the 2816 or 2817. The user will find that tangible cost savings per system include: board space and component reductions, reduced assembly costs, savings in inventory costs, handling costs and quality assurance. The designer will find the NMC9817 reduces design time by a sizable factor over the 2816 or 2817 due to the integration of timing, logic, latching and 5V-only operation.

The NMC9817 will also open up new applications in environments where flexible parameter/data storage could not be implemented before. For example, applications with board space constraints are ideal for the NMC9817. Several NMC9817s can reside in the same space as one (1) 2816 with its support circuits. This is due to the reduction of all components required including the V_{PP} generator.

WRITE TIME CHARACTERISTICS

The NMC9817's internal write cycle contains an automatic erase feature. The 2816 does not have this capability and must be given an external erase cycle prior to a write. Typically, these devices will write in times less than 9 ms, but the worst-case bit defines the minimum specification.

The NMC9817's internal cycle consists of an automatic 2 ms (typical) erase followed by a 2 ms (typical) write. The total cycle is then typically 4 ms. This cycle is the time that 'Ready' is held low by the device. The NMC9817 maximum specification is 10 ms.