128Kx32 12V FLASH MODULE, SMD 5962-94610

FEATURES

- Access Times of 120, 150, 200ns
- Packaging
  - 66 pin, PGA Type, 1.075 inch square, Hermetic Ceramic HIP (Package 400)
  - 68 lead, 40mm, Hermetic CQFP (Package 501)
  - 68 lead, Hermetic CQFP (G2), 22mm (0.880 inch) square (Package 500). Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 3)
- Chip Erase
- 10,000 Erase/Program Cycles Minimum at 125°C; 100,000 Typical at 25°C
- Organized as 128Kx32
- Commercial, Industrial and Military Temperature Ranges
- 12 Volt Programming; 5V (±10%) Supply
- Low Power CMOS, 4mA Standby Typical
- Hardware and Software Write Protection
- TTL Compatible Inputs and Outputs
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
  WF128K32-XG2X - 8 grams typical
  WF128K32-XH1X - 13 grams typical
  WF128K32-XG4X - 20 grams typical

FIG. 1 PIN CONFIGURATION FOR WF128K32N-XH1X, SMD 5962-94610

TOP VIEW

1	12	23		34	45	56
I/O8	$\overline{WE}_2$	I/O15		I/O24	VCC	I/O31
I/O9	$\overline{CS}_2$	I/O14		I/O25	$\overline{CS}_4$	I/O30
I/O10	GND	I/O13		I/O26	$\overline{WE}_4$	I/O29
A14	I/O11	I/O12		A7	I/O27	I/O28
A16	A10	$\overline{OE}$		A12	A4	A1
A11	A9	NC		VPP	A5	A2
A0	A15	$\overline{WE}_1$		A13	A6	A3
NC	VCC	I/O7		A8	$\overline{WE}_3$	I/O23
I/O0	$\overline{CS}_1$	I/O6		I/O16	$\overline{CS}_3$	I/O22
I/O1	NC	I/O5		I/O17	GND	I/O21
I/O2	I/O3	I/O4		I/O18	I/O19	I/O20
11	22	33		44	55	66

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
VPP	Program/Erase Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

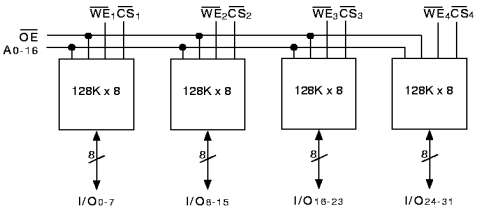
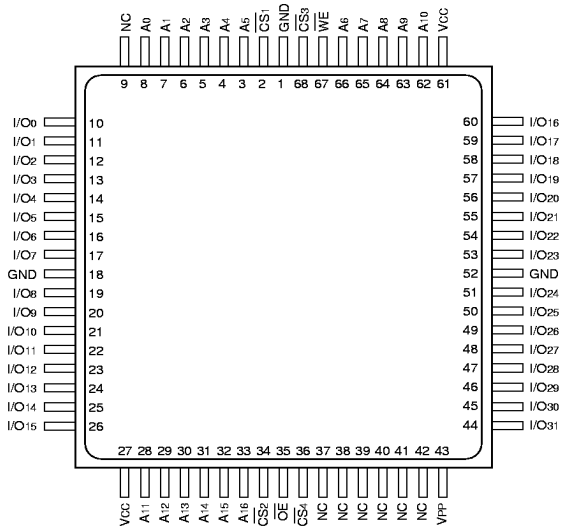


FIG. 2 PIN CONFIGURATION FOR WF128K32-XG4X

TOP VIEW



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
VPP	Program/Erase Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

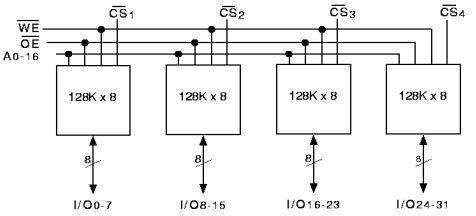
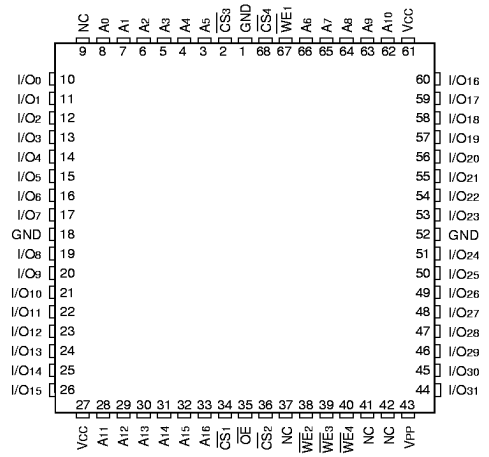
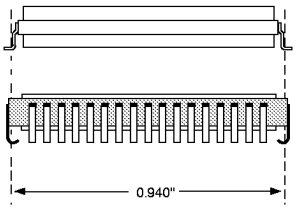


FIG. 3 PIN CONFIGURATION FOR WF128K32-XG2X, PACKAGE UNDER DEVELOPMENT

TOP VIEW



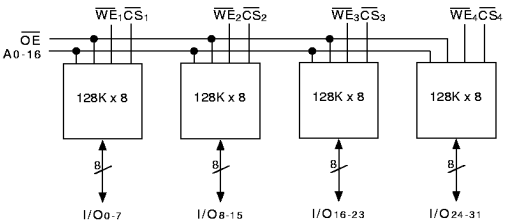


The White 68 lead G2 CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2 has the TCE and lead inspection advantage of the CQFP form.

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
VPP	Program/Erase Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Operating Temperature	-55 to +125	°C
Storage Temperature	-65 to +150	°C
Voltage on Any Pin With Respect to Ground	-2.0 to +7.0	V(1)
Voltage on Pin A9 With Respect to Ground	-2.0 to +13.5	V(1,2)
VPP Supply Voltage With Respect to Ground During Erase	-2.0 to +14.0	V(1,2)
VCC Supply Voltage With Respect to Ground	-2.0 to +7.0	V(1)
Output Short Circuit Current	100	mA(3)

NOTES:
1. Minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods less than 20ns. Maximum DC voltage on output pins is VCC +0.5V, which may overshoot to VCC + -2.0V for periods less than 20ns.
2. Maximum DC voltage on A9 or Vpp may overshoot to +14.0V for periods less than 20ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

NOTICE: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the Operating Conditions shown below, is not recommended and extended exposure beyond the Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	VCC	4.5	5.5	V
Input High Voltage	VIH	2.0	Vcc+0.3	V
Input Low Voltage	VIL	-0.5	+0.8	V
Operating Temp. (Mil.)	TA	-55	+125	°C
Operating Temp. (Ind.)	TA	-40	+85	°C

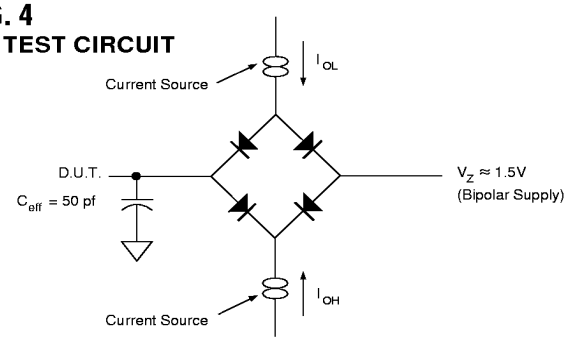
CAPACITANCE

(TA = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	COE	VIN = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}_{1-4}$ capacitance HIP (PGA)	CWE	VIN = 0 V, f = 1.0 MHz	20	pF
CQFP G4			50	
CQFP G2			20	
$\overline{CS}_{1-4}$ capacitance	CCS	VIN = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	CI/O	VI/O = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	CAD	VIN = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

FIG. 4
AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	VIL = 0, VIH = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
VZ is programmable from -2V to +7V.
IOL & IOH programmable from 0 to 16mA.
Tester Impedance $Z_0 = 75\ \Omega$.
VZ is typically the midpoint of VOH and VOL.
IOL & IOH are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

TABLE 1 - BUS OPERATIONS

Mode		Pins						
		V_{PP}[1]	A_0	A_9	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	DQ_0-DQ_7
Read-only	Read	V_{PPL}	A_0	A_9	V_{IL}	V_{IL}	V_{IH}	Data Out
	Output Disable	V_{PPL}	X	X	V_{IL}	V_{IH}	V_{IH}	Tri-State
	Standby	V_{PPL}	X	X	V_{IH}	X	X	Tri-State
read/write	Read	V_{PPH}	A_0	A_9	V_{IL}	V_{IL}	V_{IH}	Data Out
	Output Disable	V_{PPH}	X	X	V_{IL}	V_{IH}	V_{IH}	Tri-State
	Standby	V_{PPH}	X	X	V_{IH}	X	X	Tri-State
	Write	V_{PPH}	A_0	A_9	V_{IL}	V_{IH}	V_{IL}	Data In

NOTES:
1. Refer to DC Characteristics. When $V_{PP} = V_{PPL}$ memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 2. All other addresses low.
3. Read operations with $V_{PP} = V_{PPH}$ may access array data or the Intelligent Identifier codes.
4. With V_{PP} at high voltage, the standby current equals $I_{CC} + I_{PP}$ (standby).
5. X can be V_{IL} or V_{IH}.

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	-120		-150		-200		Unit
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND or V_{CC}		10		10		10	µA
Output Leakage Current	I_{LO}	V_{CC} = 5.5, V_{IN} = GND or V_{CC}		10		10		10	µA
V_{CC} Read Current x 32 Mode	I_{CCx32}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz		120		120		120	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz		6.5		6.5		6.5	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1, mA, V_{CC} = 4.5		0.45		0.45		0.45	V
Output High Voltage	V_{OH}	I_{OH} = -2.5mA, V_{CC} = 4.5	2.4		2.4		2.4		V
V_{CC} Programming Current	I_{CC2}	Programming in Progress		120		120		120	mA
V_{CC} Erase Current	I_{CC3}	Erasure in Progress		120		120		120	mA
V_{PP} Programming Current	I_{PP2}	Programming in Progress		120		120		120	mA
V_{PP} Erase Current	I_{PP3}	Erasure in Progress		120		120		120	mA
V_{PP} Read Current	I_{PPRx32}	$V_{PP} = V_{PPH}$ Max		800		800		800	µA
V_{PP} During Read Operation	V_{PPL}		0	6.5	0	6.5	0	6.5	V
V_{PP} During Read/Write	V_{PPH}		11.4	12.6	11.4	12.6	11.4	12.6	V
V_{PP} Leakage	I_{PPS}	$V_{PP} = V_{PPL}$		50		50		50	µA

NOTE: DC test conditions: $V_{IH} = V_{CC}$ -0.3V, V_{IL} = 0.3V

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		-120		-150		-200		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	120		150		200		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	20		20		20		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	80		80		80		ns
Address Setup Time	t_{AVWH}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	50		50		50		ns
Data Hold Time	t_{WHDX}	t_{DH}	10		10		15		ns
Address Hold Time	t_{WHAX}	t_{AH}	60		60		75		ns
Chip Select Hold Time	t_{WHEH}	t_{CH}	0		0		0		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	20		20		20		ns
Duration of Programming Operation	t_{WHWH1}		10		10		10		µs
Duration of Erase Operation	t_{WHWH2}		9.5		9.5		9.5		ms
Write Recovery Time before Read	t_{WHGL}		6		6		6		µs

AC CHARACTERISTICS – READ-ONLY OPERATIONS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		-120		-150		-200		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	120		150		200		ns
Address Access Time	t_{AVQV}	t_{ACC}		120		150		200	ns
Chip Select Access Time	t_{ELQV}	t_{CS}		120		150		200	ns
$\overline{OE}$ Access Time	t_{GLQV}	t_{OE}		60		65		75	ns
Chip Select to Output Low Z (1)	t_{ELQX}	t_{LZ}	0		0		0		ns
$\overline{OE}$ to Output Low Z (1)	t_{GLQX}	t_{OLZ}	0		0		0		ns
$\overline{OE}$ High to Output High Z (1)	t_{GHQZ}	t_{DF}		30		35		40	ns
Output Hold from Address, $\overline{CS}$ or $\overline{OE}$ Change, whichever is First		t_{OH}	0		0		0		ns

1. Guaranteed by design, but not tested.

FIG. 5 AC WAVEFORMS FOR PROGRAMMING OPERATIONS

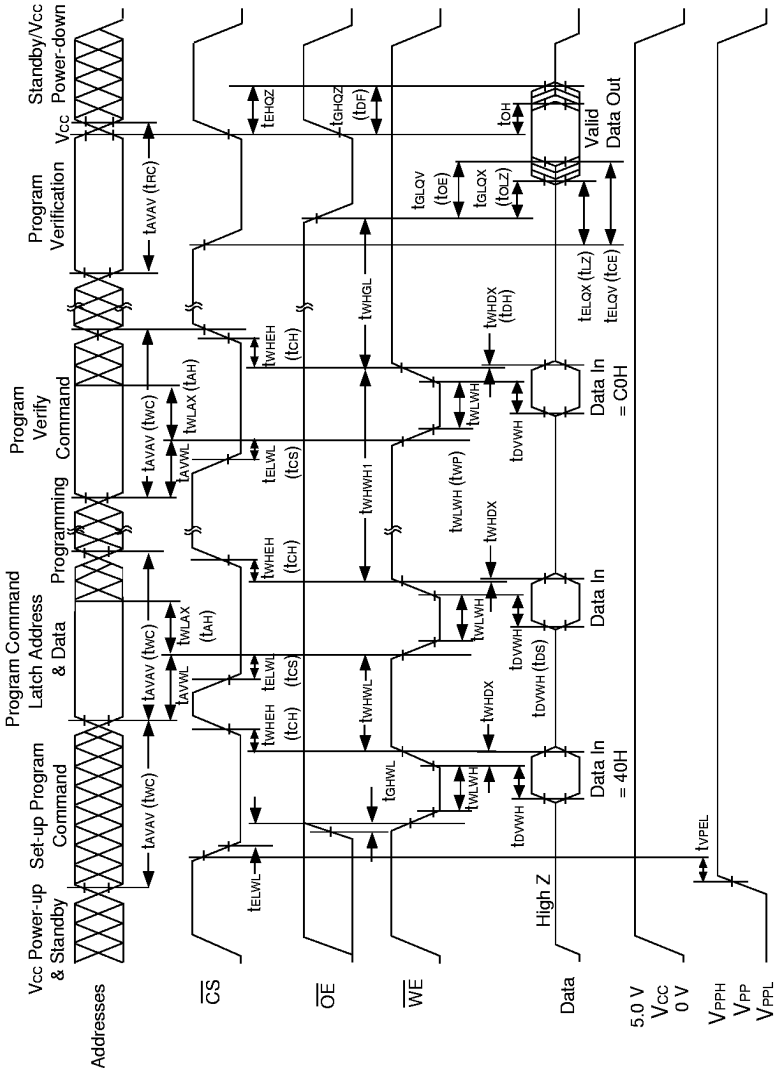


FIG. 6 AC WAVEFORMS FOR ERASE OPERATIONS

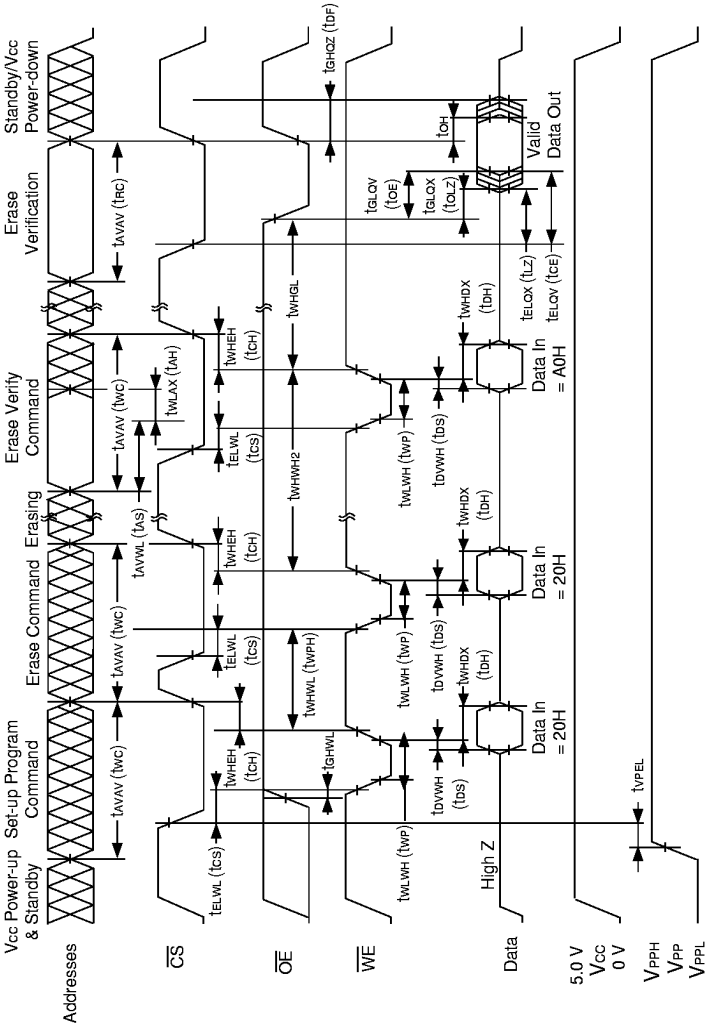
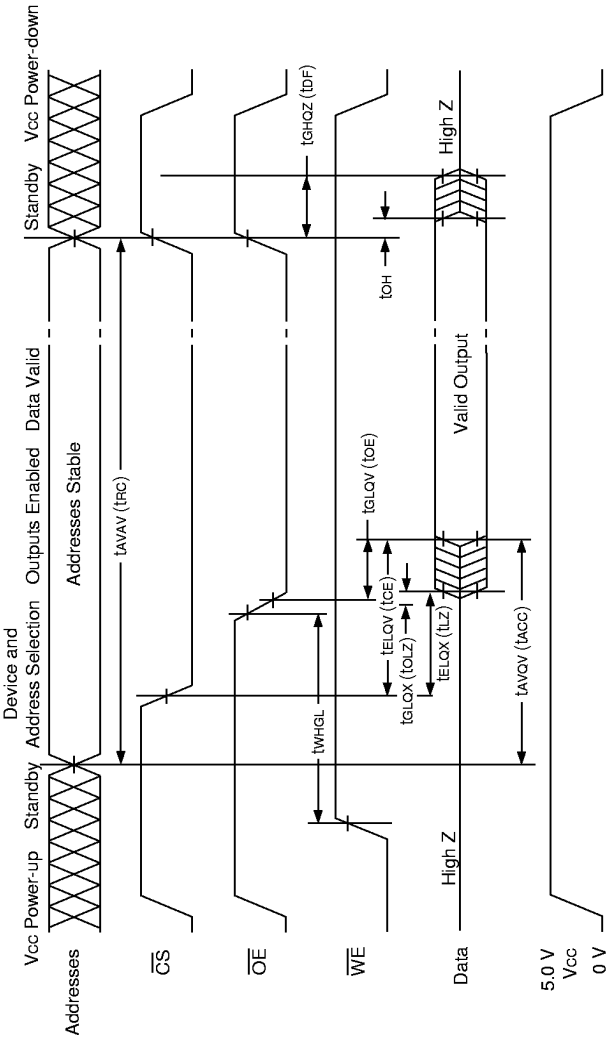


FIG. 7 AC WAVEFORMS FOR READ OPERATIONS



PRINCIPLES OF OPERATION

The following principles of operation of the WF128K32-XXX is applicable to each of the four memory chips inside the MCM. Chip 1 is distinquished by CS_1 and I/O_{0-7}, Chip 2 by CS_2 and I/O_{8-15}, Chip 3 by CS_3 and I/O_{16-23}, and Chip 4 by CS_4 and I/O_{24-31}.

The module requires both 5VDC supply voltage for operation, and a 12VDC supply for writing command register array erasure or array programming. In the absence of voltage on the V_{PP} pin, the device is a read-only memory. Manipulation of the external memory-control pins yields standard EPROM, read, standby, and output disable operations.

The read, standby, and output disable operations are still available when the 12 volts is applied to the V_{PP} pin. In addition, the high voltage to V_{PP} enables erasure and programming of the device. All functions associated with altering memory contents, erase, erase verify, program, and program verify are accessed via the command register.

Commands are written to the register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which control the erase and programming circuitry. Write cycles also internally latch page addresses and data needed for programming or erase operations. With the appropriate command written to the register, standard microprocessor read timings output data for erase and program verification.

WRITE PROTECTION

The command register is only active when V_{PP} is at high voltage. Depending on the application, the system designer may choose to make the V_{PP} power supply switchable and only available when memory updates are desired. When the high voltage is removed, the contents of the register default to the read command, the module turns back into a read-only memory, and the memory contents cannot be altered.

BUS OPERATIONS

READ

The WF128K32-XXX has two control functions, both of which must be logically active, to obtain data at the outputs. Chip-Select ($\overline{CS}$) is the power control and should be used for device selection. Output-Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Figure 7 illustrates read timing waveforms.

The read operation only accesses array data when V_{PP} is low (V_{PPL}). When V_{PP} is high (V_{PPH}), the read operation can be used to access array data, and to access data for program/erase verification.

OUTPUT DISABLE

With Output-Enable at a logic-high level (V_{IH}), output from the device is disabled. Output pins are placed in a high-impedance state.

STANDBY

With Chip-Select at a logic-high level, the standby operation disables most of the WF128K32-XXX's circuitry and substantially reduces device power consumption. The outputs are placed in a high-impedance state, independent of the Output-Enable signal. Note: If the WF128K32-XXX is deselected during erasure, programming or program/erase verification, the device draws active current until the operation is terminated.

WRITE

Device erasure and programming are accomplished via the command register, when high voltage is applied to the V_{PP} pin. The contents of the register serve as input to the internal state-machine. The state-machine outputs dictate the function of the device.

The command register itself does not occupy an addressable memory location. The register is a latch used to store the command, along with address and data information needed to execute the command. The command register is written by bringing Write-Enable to a logic-low level (V_{IL}), while Chip-Select is low. Addresses are latched on the falling edge of Write-Enable, while data is latched on the rising edge of the Write-Enable pulse. Standard microprocessor write timings are used.

COMMAND DEFINITIONS

When low voltage is applied to the V_{PP} pin of the chip selected, the contents of the command register default to 00H, enabling read-only operations.

Placing high voltage on the V_{PP} pin of the chip selected enables read/write operations. Device operations are selected by writing specific data patterns into the command register of the chip selected. Table 2 defines these register commands.

TABLE 2 - COMMAND DEFINITIONS

Command	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
		Oper	Addr	Data	Oper	Addr	Data
Read Memory	1	Write	X	00H			
Set-up Erase/Erase	2	Write	X	20H	Write	X	20H
Erase Verify	2	Write	EA	A0H	Read	X	EVD
Set-up Program/Program	2	Write	X	40H	Write	PA	PD
Program Verify	2	Write	X	C0H	Read	X	PVD
Reset	2	Write	X	FFH	Write	X	FFH

NOTES:
1. EA = Address of memory location to be read during erase verify.
   PA = Address of memory location to be programmed
   Addresses are latched on the falling edge of the Write-Enable pulse
2. EVD = Data read from location EA during erase verify.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of Write-Enable.
   PVD = Data read from location PA during program verify. PA is latched on the Program command.

READ COMMANDS

While V_{PP} is high, for erasure and programming, memory contents can be accessed via the read command. The read operation is initiated by writing 00H into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

The default contents of the register upon V_{PP} power-up is 00H. This default value ensures that no spurious alteration of memory contents occurs during the V_{PP} power transition. Where the V_{PP} supply is hard-wired to the WF128K32-XXX, the device powers-up and remains enabled for reads until the command-register contents are changed. Refer to the A.C. Read Characteristics and Waveforms for specific timing parameters. (Figure 7).

SET-UP ERASE/ERASE COMMANDS

Set-up Erase is a command-only operation that stages the device for electrical erasure of all bytes in the array. The set-up erase operation is performed by writing 20H to the command register.

To commence chip-erasure, the erase command (20H) must again be written to the register. The erase operation begins with the rising edge of the Write-Enable pulse and terminates with the rising edge of the next Write-Enable pulse (i.e., Erase-Verify Command).

This two-step sequence of set-up followed by execution ensures that memory contents are not accidentally erased. Also, chip erasure can occur only when high voltage is applied to the V_{PP} pin. In the absence of this high voltage, memory contents are protected against erasure.

ERASE-VERIFY COMMAND

The erase command erases all bytes of the array in parallel. After each erase operation, all bytes must be verified. The erase verify operation is initiated by writing A0H into the command register. The address for byte to be verified must be supplied as it is latched on the falling edge of the Write-Enable pulse. The register write terminates the erase operation with the rising edge of its Write-Enable pulse. Reading FFH from the addressed byte indicates that all bits in the byte are erased.

The erase-verify command must be written to the command register prior to each byte verification to latch its address. The process continues for each byte in the array until a byte does not return FFH data, or the last address is accessed.

In the case where the data read is not FFH, another erase operation is performed (refer to Set-up Erase/Erase). Verification then resumes from the address of the last-verified byte. Once all bytes in the array have been verified, the erase step is complete. The device can be programmed. At this point, the

verify operation is terminated by writing a valid command (e.g., Program Set-up) to the command register. Figure 9 illustrates how commands and bus operations are combined to perform electrical erasure of the WF128K32-XXX.

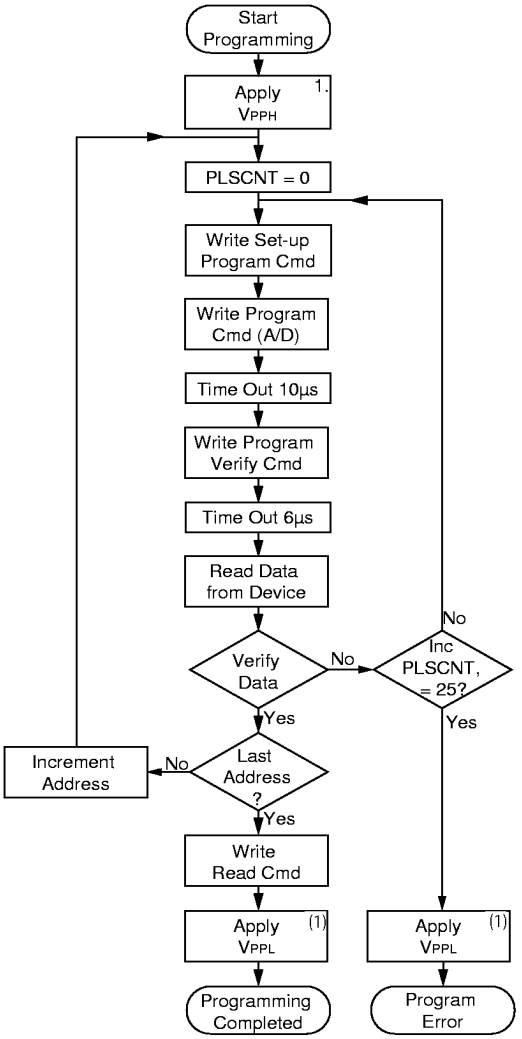
SET-UP PROGRAM/PROGRAM COMMANDS

Set-up program is a command-only operation that stages the device for byte programming. Writing 40H into the command register of the chip selected performs the set-up operation. Once the program set-up operation is performed, the next Write-Enable pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the Write-Enable pulse. Data is internally latched on the rising edge of the Write-Enable pulse. The rising edge of Write-Enable also begins the programming operation. The programming operation terminates with the next rising edge of Write-Enable, used to write the program-verify command.

PROGRAM-VERIFY COMMAND

The WF128K32-XXX is programmed on a byte-by-byte basis. Byte programming may occur sequentially or at random. Following each programming operation, the byte just programmed must be verified. The program-verify operation is initiated by writing C0H into the command register of the chip selected. The register write terminates the programming operation with the rising edge of its Write-Enable pulse. The program-verify operation stages the device for verification of the byte last programmed. No new address information is latched.

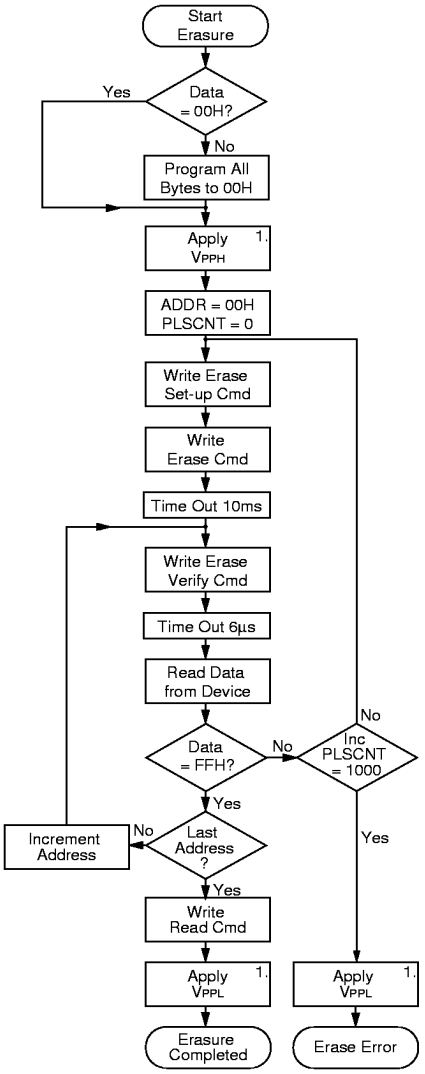
FIG. 8 PROGRAMMING ALGORITHM



Bus Operation	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (= 12.0V) (1)
		Initialize pulse- count
Write	Set-up Program	Data = 40H
Write	Program	Valid address/data
Standby		Duration of Program operation (t_{WHWH1})
Write	Program Verify (2)	Data = C0H; Stops Program Operation
Standby		t_{WHGL}
Read		Read byte to verify programming
Standby		Compare data output to data expected
Write	Read	Data = 00H, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (1)

NOTES:
1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no-connect with a resistor tied to ground, or less than V_{CC} + 2.0V. Refer to Principles of Operation.
2. Program Verify is only performed after byte programming. A final read/ compare may be performed (optional) after the register is written with the Read command.
3. **CAUTION:** The algorithm must be followed to ensure proper and reliable operation of the device.

FIG. 9 ERASE ALGORITHM

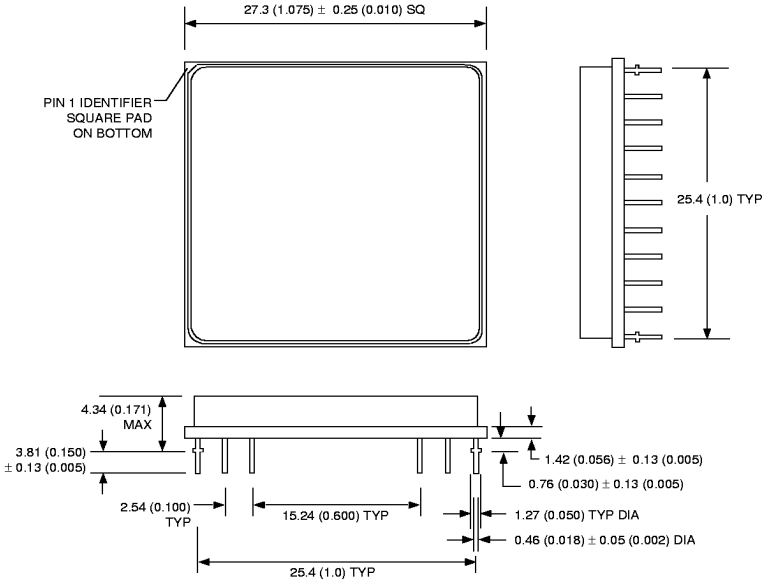


Bus Operation	Command	Comments
		Entire memory must = 00H before erasure
		NOTE: Use Programming algorithm (Fig. 8)
Standby		Wait for V_{PP} ramp to V_{PPH} (=12.0V)1.
		Initialize Addresses and Pulse Count
Write	Set-up Erase	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase operation (t_{WHWH2})
Write	Erase Verify[2]	Addr = Byte to verify; Data = A0H; Stops Erase Operation
Standby		t_{WHGL}
Read		Read byte to verify erasure
Standby		Compare output to FFH Increment pulse count
Write	Read	Data = 00H, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} 1.

NOTES:

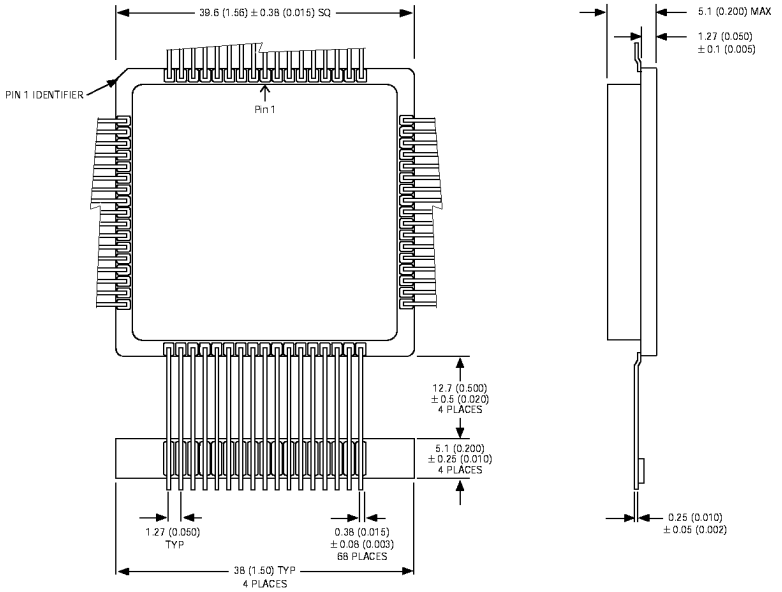
1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be no-connect with a resistor tied to ground, or less than Vcc + 2.0V. Refer to Principles of Operation.
2. Program Verify is only performed after byte programming. A final read/compare may be performed (optional) after the register is written with the Read command.
3. **CAUTION:** The algorithm must be followed to ensure proper and reliable operation of the device.

PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



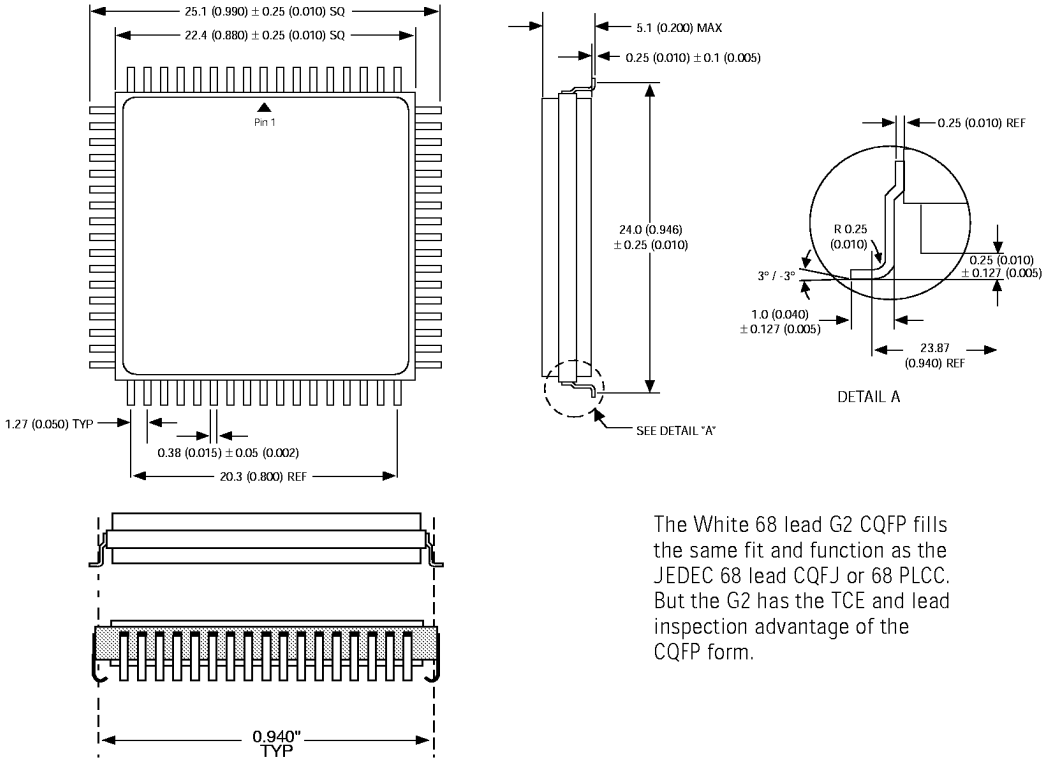
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 501: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G4)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

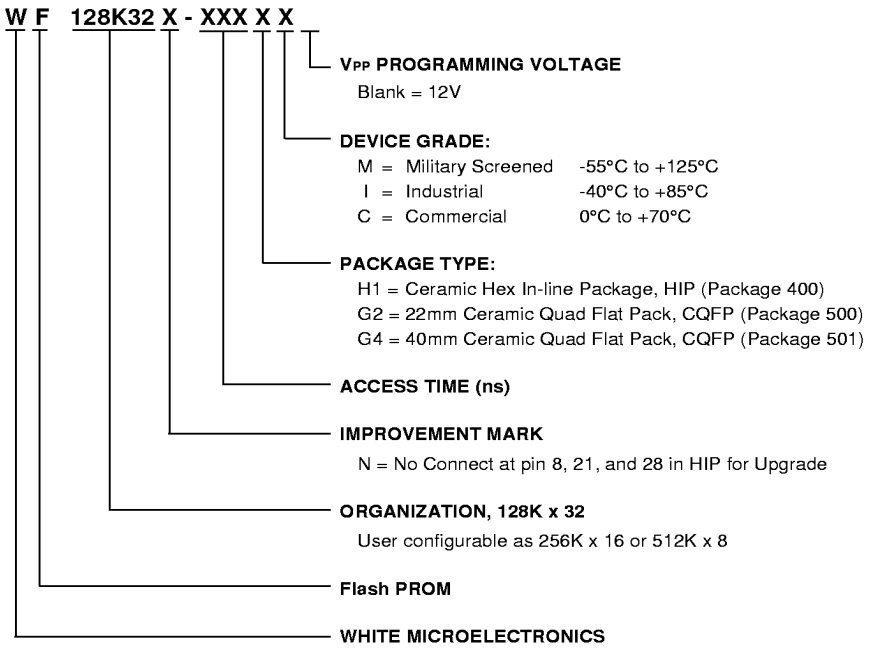
PACKAGE 500: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2)



The White 68 lead G2 CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2 has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION



DEVICE TYPE	SPEED	PACKAGE	SMD NO.
128K x 32 Flash	200ns	66 pin HIP (H1)	5962-94610 01HXX
128K x 32 Flash	150ns	66 pin HIP (H1)	5962-94610 02HXX
128K x 32 Flash	120ns	66 pin HIP (H1)	5962-94610 03HXX