

# AC821 • ACT821 • AC822 • ACT822

NATIONAL SEMICONDUCTOR LOGIC DE D 6501122 0062696 8

## 54AC/74AC821 • 54ACT/74ACT821 54AC/74AC822 • 54ACT/74ACT822

*T-4607-12*

### 10-Bit D-Type Flip-Flop

#### Description

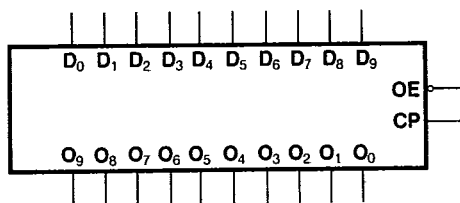
The 'AC/'ACT821 and 'AC/'ACT822 are 10-bit D-type flip-flops with 3-state outputs arranged in a broadside pinout.

The 'AC/'ACT821 and 'AC/'ACT822 are functionally identical to the AM29821 and AM29822.

- 3-State Outputs for Bus Interfacing
- Inverting ('822) or Noninverting ('821) Outputs
- Outputs Source/Sink 24 mA
- 'ACT821 and 'ACT822 have TTL-Compatible Inputs

Ordering Code: See Section 6

#### Logic Symbol ('AC/'ACT821)\*

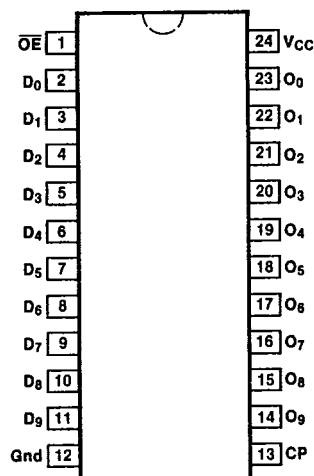


\*The 'AC/'ACT822 has inverting outputs.

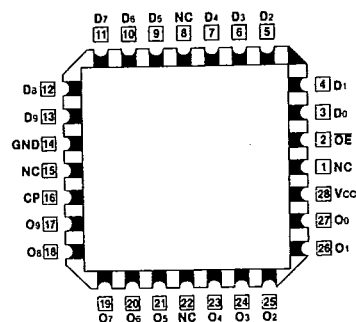
#### Pin Names

- D<sub>0</sub> - D<sub>9</sub> Data Inputs
- O<sub>0</sub> - O<sub>9</sub> Data Outputs ('AC/'ACT821)
- $\bar{O}_0$  -  $\bar{O}_9$  Data Outputs ('AC/'ACT822)
- $\bar{OE}$  Output Enable
- CP Clock Input

#### Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

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## Functional Description

The 'AC/ACT821 and 'AC/ACT822 consist of ten D-type edge-triggered flip-flops. The buffered Clock (CP) and buffered Output Enable ( $\overline{OE}$ ) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With  $\overline{OE}$  LOW the contents of the flip-flops are available at the outputs. When  $\overline{OE}$  is

HIGH the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

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The 'AC/ACT821 and 'AC/ACT822 are functionally and pin compatible with the AM29821 and AM29822.

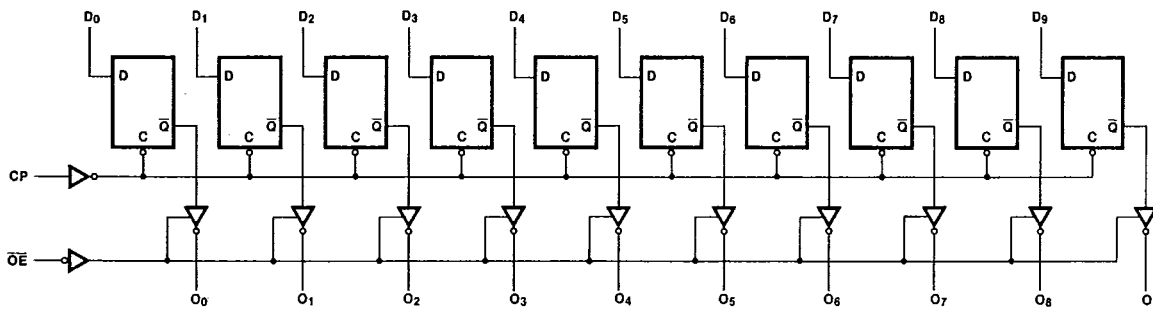
Function Table

Inputs			Internal	Outputs		Function
$\overline{OE}$	CP	D	Q	O ('821)	$\overline{O}$ ('822)	
H	$\downarrow$	L	L	Z	Z	High Z
H	$\downarrow$	H	H	Z	Z	High Z
L	$\downarrow$	L	L	L	H	Load
L	$\downarrow$	H	H	H	L	Load

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 Z = High Impedance  
 $\downarrow$  = LOW-to-HIGH Clock Transition

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Logic Diagram ('AC/ACT821)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays. The 'AC/ACT822 also has the same logic diagram with inverting outputs.

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DC Characteristics (unless otherwise specified)

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Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I <sub>CC</sub>	Maximum Quiescent Supply Current	160	80	μA	V <sub>IN</sub> = V <sub>CC</sub> or Ground, V <sub>CC</sub> = 5.5 V, T <sub>A</sub> = Worst Case
I <sub>CC</sub>	Maximum Quiescent Supply Current	8.0	8.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or Ground, V <sub>CC</sub> = 5.5 V, T <sub>A</sub> = 25°C
I <sub>CC</sub> T	Maximum Additional I <sub>CC</sub> /Input (ACT821/822)	1.6	1.5	mA	V <sub>IN</sub> = V <sub>CC</sub> - 2.1 V, V <sub>CC</sub> = 5.5 V, T <sub>A</sub> = Worst Case

## AC Characteristics

Symbol	Parameter	V <sub>CC</sub> * (V)	74AC			54AC		74AC		Units	Fig. No.
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	3.3 5.0	100 125						MHz	3-3	
t <sub>PLH</sub>	Propagation Delay CP to O <sub>n</sub>	3.3 5.0	9.5 6.5						ns	3-6	
t <sub>PHL</sub>	Propagation Delay CP to O <sub>n</sub>	3.3 5.0	9.5 6.5						ns	3-6	
t <sub>PZH</sub>	Output Enable Time $\overline{OE}$ to O <sub>n</sub>	3.3 5.0	7.5 5.5						ns	3-7	
t <sub>PZL</sub>	Output Enable Time $\overline{OE}$ to O <sub>n</sub>	3.3 5.0	8.0 6.0						ns	3-8	
t <sub>PHZ</sub>	Output Disable Time $\overline{OE}$ to O <sub>n</sub>	3.3 5.0	10.5 7.5						ns	3-7	
t <sub>PLZ</sub>	Output Disable Time $\overline{OE}$ to O <sub>n</sub>	3.3 5.0	9.0 6.5						ns	3-8	

\*Voltage Range 3.3 is 3.3 V ± 0.3 V  
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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## AC Operating Requirements

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Symbol	Parameter	Vcc* (V)	74AC		54AC		74AC		Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Typ	Guaranteed Minimum						
ts	Setup Time, HIGH or LOW Dn to CP	3.3 5.0	3.0 2.0						ns	3-9
th	Hold Time, HIGH or LOW Dn to CP	3.3 5.0	2.0 1.5						ns	3-9
tw	CP Pulse Width HIGH or LOW	3.3 5.0	3.5 2.5						ns	3-6

\*Voltage Range 3.3 is 3.3 V ± 0.3 V  
Voltage Range 5.0 is 5.0 V ± 0.5 V

## AC Characteristics

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Symbol	Parameter	Vcc* (V)	74ACT			54ACT		74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
fmax	Maximum Clock Frequency	5.0	120	110			110		MHz	3-3	
tPLH	Propagation Delay CP to On	5.0	1.0	8.0	9.5			1.0	10.5	ns	3-6
tPHL	Propagation Delay CP to On	5.0	1.0	8.0	9.5			1.0	10.5	ns	3-6
tpZH	Output Enable Time OE to On	5.0	1.0	7.0	10.5			1.0	11.5	ns	3-7
tpZL	Output Enable Time OE to On	5.0	1.0	7.5	10.5			1.0	12.0	ns	3-8
tPHZ	Output Disable Time OE to On	5.0	1.0	10.0	12.0			1.0	13.0	ns	3-7
tPLZ	Output Disable Time OE to On	5.0	1.0	9.5	10.5			1.0	11.5	ns	3-8

\*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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## AC Operating Requirements

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Symbol	Parameter	Vcc* (V)	74ACT		54ACT	74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -55°C to +125°C CL = 50 pF	TA = -40°C to +85°C CL = 50 pF			
			Typ	Guaranteed Minimum					
t <sub>s</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to CP	5.0	2.0	2.0			2.5	ns	3-9
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	5.0	-0.5	2.0			2.5	ns	3-9
t <sub>w</sub>	CP Pulse Width HIGH or LOW	5.0	3.0	4.5			5.5	ns	3-6

\*Voltage Range 5.0 Is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

## Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C <sub>IN</sub>	Input Capacitance	4.5	pF	Vcc = 5.5 V
CPD	Power Dissipation Capacitance	35.0	pF	Vcc = 5.5 V