REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET	35																		
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
93-06-17

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, N-CHANNEL, 8-BIT MICROPROCESSOR, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-38480
A	67268	

SHEET 1 OF 35

DESC FORM 193
JUL 91

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5962-E141-93

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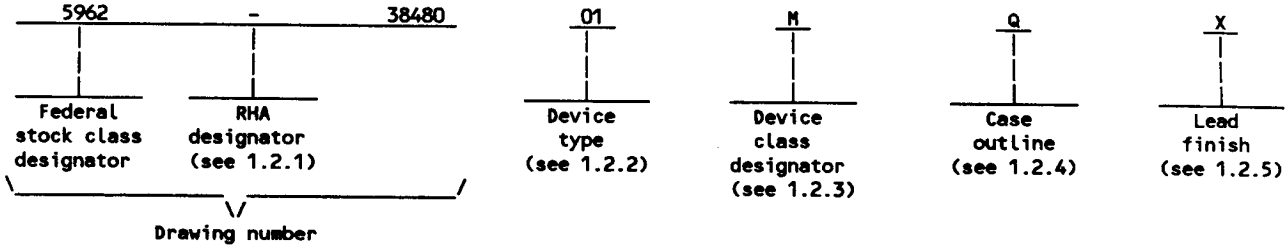
1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Clock frequency	Circuit function
01	Z08400	4.0 MHz	8-bit, fixed instruction microprocessor
02	Z08400	2.5 MHz	8-bit, fixed instruction microprocessor
03 1/	Z08400	6.0 MHz	8-bit, fixed instruction microprocessor

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Q	GDIP1-T40 or CDIP2-T40	40	Dual-in-line
X 1/	CQCC1-N44A	44	Square leadless chip carrier, option A
Y 1/	CQCC1-N44B	44	Square leadless chip carrier, option B

1/ Not available from an approved source of supply.

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1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

V_{CC} supply voltage range (V_{CC} - GND)	-0.3 V to +7.0 V
Voltage on any pin (referenced to ground)	-0.3 V to +7.0 V
Storage temperature range	-65° C to +150° C
Maximum power dissipation, (P_D):	
T_C = -55°C	1.5 W
T_C = +125°C	1.0 W
Lead temperature (soldering, 5 seconds)	270°C
Maximum junction temperature (T_J)	170°C 2/
Thermal resistance, junction to case (Θ_{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage range	4.5 V minimum to 5.5 V maximum
Minimum high-level input voltage	
Logic inputs (V_{IH})	2.2 V
Clock input (V_{IHC})	V_{CC} -0.6 V
Maximum low-level input voltage	
Logic inputs (V_{IL})	+0.8 V
Clock input (V_{ILC})	+0.45 V
Frequency of operation	
Device type 01	0.5 to 4.0 MHz
Device type 02	0.5 to 2.5 MHz
Device type 03	0.5 to 6.0 MHz
Case operating temperature range	-55°C to +125°C
Clock rise time (t_r)	
Device types 01 and 02	30 ns maximum
Device type 03	20 ns maximum
Clock fall time (t_f)	
Device types 01 and 02	30 ns maximum
Device type 03	20 ns maximum

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 3/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operating at the maximum levels may degrade performance and affect reliability.

2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening condition per method 5004 of MIL-STD-883.

3/ Values will be added when they become available.

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2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagrams. The block diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

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3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 107 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

3.12 PIN supersession information. Pin supersession information shall be as specified in the appendix.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified 1/ $4.5 \le V_{CC} \le 5.5$ V	Refer. No 2/	Group A subgroups	Device type	Limits		Unit
						Min	Max	
Clock input low voltage	V_{ILC}	V_{CC} = 4.5 V		1,2,3	ALL	-0.3	0.45	V
Clock input high voltage	V_{IHC}	V_{CC} = 4.5 V		1,2,3,	ALL	V_{CC} - 0.6	V_{CC} + 0.3	V
Input low voltage	V_{IL}	V_{CC} = 4.5 V		1,2,3	ALL	-0.3	0.8	V
Input high voltage	V_{IH}	V_{CC} = 4.5 V		1,2,3,	ALL	2.2	V_{CC}	V
Output low voltage	V_{OL}	I_{OL} = 1.8 mA V_{CC} = 4.5 V		1,2,3	ALL		0.4	V
Output high voltage	V_{OH}	I_{OH} = -250 µA V_{CC} = 4.5 V		1,2,3	ALL	2.4		V
Power supply current	I_{CC}	V_{CC} = 5.5 V		1,2,3	ALL		250	mA
Input leakage current, low	I_{IL1}	V_{IN} = 0.4 V V_{CC} = 5.5 V		1,2,3	ALL	-10	+10	µA
Input leakage current, high	I_{IH1}	V_{IN} = 2.4 V V_{CC} = 5.5 V		1,2,3	ALL	-10	+10	µA
Tristate output leakage, current, low	I_{ZL}	V_{OUT} = 0.4 V V_{CC} = 5.5 V		1,2,3	ALL	-10	+10	µA
Tristate output leakage, current, high	I_{ZH}	V_{OUT} = 2.4 V V_{CC} = 5.5 V		1,2,3	ALL	-10	+10	µA
Input leakage current, low-data bus	I_{IL2}	V_{IN} = 0.4 V V_{CC} = 5.5 V		1,2,3	ALL	-10	+10	µA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified 1/ $4.5\ V \le V_{CC} \le 5.5\ V$	Refer. No 2/	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Input leakage current, high-data bus	I_{IH2}	$V_{IN} = 2.4\ V$ $V_{CC} = 5.5\ V$		1,2,3	ALL	-10	+10	µA
Clock capacitance	C_C	f = 1 MHz, $T_C = +25°C$; from input or output pin to ground, all other pins at ground see 4.4.1c		4	ALL		35	pF
Input capacitance, all other inputs	C_I			4	ALL		5	pF
Output capacitance, all outputs and data bus	C_O			4	ALL		15	pF
Functional test		see 4.4.1b		7,8	ALL			
Maximum clock frequency	f_{MAX}	$V_{CC} = 4.5\ V$ $C_L = 50\ pF \pm 10\%$		9,10,11	01 02 03	4.0 2.5 6.0		MHz
Maximum clock frequency	f_{MAX}	$V_{CC} = 5.5\ V$ $C_L = 50\ pF \pm 10\%$		9,10,11	01 02 03	4.0 2.5 6.0		MHz
Clock cycle time	t_{cyc}	$V_{CC} = 4.5\ V$ unless otherwise specified; $C_L = 140\ pF \pm 10\%$ see figures 4 and 5	1	9,10,11	01 02 03	250 400 165	3/	ns
Clock time Rise	t_r		5	9,10,11	01,02 03		30 20	ns
Fall	t_f		4	9,10,11	01,02 03		30 20	ns
Clock pulse width high	t_{PWH1}		2	9,10,11	01 02 03	110 180 65	2,000 2,000 2,000	ns
Clock pulse width low	t_{PWL1}		3	9,10,11	01 02 03	110 180 65	2,000 2,000 2,000	ns
$\overline{MREQ}$ pulse width high	t_{PWH2}		10	9,10,11	All	4/		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified 1/ $4.5\ V \le V_{CC} \le 5.5\ V$	Refer. No 2/	Group A subgroups	Device type	Limits Min	Limits Max	Unit
$\overline{MREQ}$ Pulse width low	t_{PWL2}	V_{CC} = 4.5 V unless otherwise specified; C_L = 140 pF ±10% see figures 4 and 5	11	9,10,11	ALL	5/		ns
$\overline{WR}$ pulse width low	t_{PWL3}		31	9,10,11	ALL	6/		ns
$\overline{NMI}$ pulse width low	t_{PWL4}		37	9,10,11	01,02	80		ns
					03	70		
Data setup to clock ↑ (D0 - D7)	t_{SZH1}		15	9,10,11	01	35		ns
					02	50		
					03	30		
	t_{SZL1}				01	35		
					02	50		
					03	30		
$\overline{WAIT}$ setup to clock ↓	t_{SLH1}		17	9,10,11	01,02	70		ns
					03	60		
	t_{SHL1}				01,02	70		
					03	60		
Data setup to clock ↓ (D0 - D7)	t_{SZH2}		25	9,10,11	01	50		ns
					02	60		
					03	40		
	t_{SZL2}				01	50		
					02	60		
					03	40		
$\overline{BUSRQ}$ setup to clock ↑	t_{SLH2}		38	9,10,11	01	50		ns
					02	80		
					03	50		
	t_{SHL2}				01	50		
					02	80		
					03	50		
$\overline{RESET}$ setup to clock ↑	t_{SLH3}		46	9,10,11	01	60		ns
					02	90		
					03	60		
	t_{SHL3}				01	60		
					02	90		
					03	60		
$\overline{INT}$ setup to clock ↑	t_{SLH4}		48	9,10,11	01,02	80		ns
					03	70		
	t_{SHL4}				01,02	80		
					03	70		
Data valid after RD ↑ (D0 - D7)	t_{HLZ1}		16	9,10,11	All	0		
	t_{HHZ1}							

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified 1/ $4.5\ V \le V_{CC} \le 5.5\ V$	Refer. No 2/	Group A subgroups	Device type	Limits Min	Limits Max	Unit
$\overline{WAIT}$ valid after clock ↓	t_{HLH1}	V_{CC} = 4.5 V unless otherwise specified; C_L = 140 pF ±10% see figures 4 and 5	18	9,10,11	ALL	0		ns
	t_{HHL1}				ALL	0		ns
$\overline{BURSQ}$ valid after clock ↑	t_{HLH2}		39	9,10,11	ALL	0		ns
	t_{HHL2}				ALL	0		
$\overline{RESET}$ valid after clock ↑	t_{HLH3}		47	9,10,11	ALL	0		ns
	t_{HHL3}				ALL	0		ns
$\overline{INT}$ valid after clock ↑	t_{HLH4}		49	9,10,11	ALL	0		ns
	t_{HHL4}				ALL	0		ns
Clock ↑ to address valid delay (A_0 -A_{15})	t_{PLH1}		6	9,10,11	01		110	ns
	t_{PHL1}				02		145	
					03		90	
Address valid to MREQ ↓ delay	t_{PLH2}		7	9,10,11	ALL	7/		ns
	t_{PHL2}					7/		
Address stable before IORQ ↓	t_{PLH3}		26	9,10,11	ALL	8/		ns
	t_{PHL3}					8/		
Clock ↑ to address float delay	t_{PLZ1}		44	9,10,11	01		90	ns
	t_{PHZ1}				02		110	
					03		80	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified 1/ $4.5\ V \le V_{CC} \le 5.5\ V$	Refer. No 2/	Group A subgroups	Device type	Limits		Unit
						Min	Max	
Address stable from MREQ ↑, RD ↑, WR ↑, or IORQ ↑	t_{PLH4} / t_{PHL4}	V_{CC} = 4.5 V unless otherwise specified; C_L = 140 pF ±10% see figures 4 and 5	45	9,10,11	ALL	9/		ns
Data stable before WR ↓ (memory write)	t_{PZL1} / t_{PZH1}		29	9,10,11	ALL	10/		ns
Data stable before WR ↓ (I/O write)	t_{PZL2} / t_{PZH2}		33	9,10,11	ALL	11/		ns
Data stable from WR ↑	t_{PLZ2} / t_{PHZ2}		35	9,10,11	ALL	12/		ns
Clock ↑ to data float delay	t_{PLZ3} / t_{PHZ3}		42	9,10,11	01,02 03		90 80	ns
Clock ↓ to data valid delay	t_{PZL3} / t_{PZH3}		53	9,10,11	01 02 03		150 230 130	ns
Clock ↓ to MREQ ↓ delay	t_{PHL5}		8	9,10,11	01 02 03		95 100 70	ns
Clock ↓ to MREQ ↑ delay	t_{PLH5}		12	9,10,11	01 02 03		95 100 70	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified 1/ $4.5\ V \le V_{CC} \le 5.5\ V$	Refer. No 2/	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Clock ↑ to $\overline{MREQ}$ ↑ delay	t_{PLH6}	V_{CC} = 4.5 V unless otherwise specified; C_L = 140 pF ±10% See figures 4 and 5	9	9,10,11	01		95	ns
					02		100	
					03		70	
Clock ↑ to $\overline{IORQ}$ ↓ delay	t_{PHL7}		27	9,10,11	01		75	ns
					02		90	
					03		65	
Clock ↑ to $\overline{IORQ}$ ↑ delay	t_{PLH7}		52	9,10,11	01		85	ns
					02		100	
					03		70	
Clock ↓ to $\overline{IORQ}$ ↑ delay	t_{PLH8}		28	9,10,11	01		85	ns
					02		110	
					03		70	
Clock ↓ to $\overline{IORQ}$ ↓ delay	t_{PHL8}		51	9,10,11	01		85	ns
					02		110	
					03		70	
Clock ↓ to $\overline{RD}$ ↓ delay	t_{PHL9}		13	9,10,11	01		120	ns
					02		130	
					03		80	
Clock ↓ to $\overline{RD}$ ↑ delay	t_{PLH9}		23	9,10,11	01		95	ns
					02		110	
					03		70	
Clock ↑ to $\overline{RD}$ ↑ delay	t_{PLH10}		14	9,10,11	01		95	ns
					02		100	
					03		70	
Clock ↑ to $\overline{RD}$ ↓ delay	t_{PHL10}		24	9,10,11	01		95	ns
					02		100	
					03		70	
Clock ↓ to $\overline{WR}$ ↓ delay	t_{PHL11}		30	9,10,11	01,02		90	ns
					03		70	
Clock ↓ to $\overline{WR}$ ↑ delay	t_{PLH11}		32	9,10,11	01		90	ns
					02		100	
					03		70	
Clock ↑ to $\overline{WR}$ ↓ delay (I/O to write)	t_{PHL12}		34	9,10,11	01		75	ns
					02		80	
					03		70	
Clock ↑ to $\overline{MI}$ ↓ delay	t_{PHL13}		19	9,10,11	01		110	ns
					02		130	
					03		80	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified 1/ $4.5\ V \le V_{CC} \le 5.5\ V$	Refer. No 2/	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Clock ↑ to $\overline{MI}$ ↑ delay	t_{PLH13}	V_{CC} = 4.5 V unless otherwise specified; C_L = 140 pF ±10% See figures 4 and 5	20	9,10,11	01		115	ns
					02		130	
					03		80	
$\overline{MI}$ ↓ before $\overline{IORQ}$ ↓	t_{PHL14}		50	9,10,11	All	13/		ns
Clock ↑ to $\overline{RFSH}$ ↓ delay	t_{PHL15}		21	9,10,11	01		130	ns
					02		180	
					03		110	
Clock ↑ to $\overline{RFSH}$ ↑ delay	t_{PLH15}		22	9,10,11	01		120	ns
					02		150	
					03		100	
Clock ↓ to $\overline{HALT}$ valid delay	t_{PLH16}		36	9,10,11	01,02		300	ns
					03		260	
	t_{PHL16}				01,02		300	
					03		260	
Clock ↑ to $\overline{BUSAK}$ ↓ delay	t_{PHL17}		40	9,10,11	01		100	ns
					02		120	
					03		90	
Clock ↓ to $\overline{BUSAK}$ ↑ delay	t_{PLH18}		41	9,10,11	01		100	ns
					02		110	
					03		90	
Clock ↑ to $\overline{MREQ}$, $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, float delay	t_{PHZ4}		43	9,10,11	01		80	ns
					02		110	
					03		70	

See footnotes at end of table.

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Constant table

14/	Device			
Constant	01	02	03	Unit
a	65	75	50	ns
b	70	80	55	
c	50	40	50	
d	170	210	140	
e	140	180	140	
f	70	80	55	
g	30	40	30	
h	40	50	40	
j	30	40	30	
k	65	80	50	

1/ All test to be performed using worst-case test conditions unless otherwise specified.

2/ The reference number refers to the position where the parameter being measured appears on figure 4.

3/ $t_{cyc} = t_{PWH1} + t_{PWL1} + t_r + t_f$

4/ $t_{PWH2} = t_{PWH1} + t_f$ - h (see constant table)

5/ $t_{PWL2} = t_{cyc}$ - g (see constant table)

6/ $t_{PWL3} = t_{cyc}$ - j (see constant table)

7/ t_{PLH2} or $t_{PHL2} = t_{PWH1} + t_f$ - a (see constant table)

8/ t_{PLH3} or $t_{PHL3} = t_{cyc}$ - b (see constant table)

9/ t_{PLH4} or $t_{PHL4} = t_{PWL1} + t_r$ - c (see constant table)

10/ t_{PZL1} or $t_{PZH1} = t_{cyc}$ - d (see constant table)

11/ t_{PZL2} or $t_{PZH2} = t_{PWL1} + t_r$ - e (see constant tale)

12/ t_{PLZ2} or $t_{PHZ2} = t_{PWL1} + t_r$ - f (see constant table)

13/ $t_{PHL13} = 2\ (t_{cyc}) + t_{PWH1} + t_r$ - k (see constant table)

14/ The ac parameters represented by notes 4/ through 13/ are CLK dependent, the equations are used to calculate limits for any given set of CLK parameters (clock high, clock low, clock cycle time) within the frequency of operation.

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Device types 01, 02, and 03

Case Q

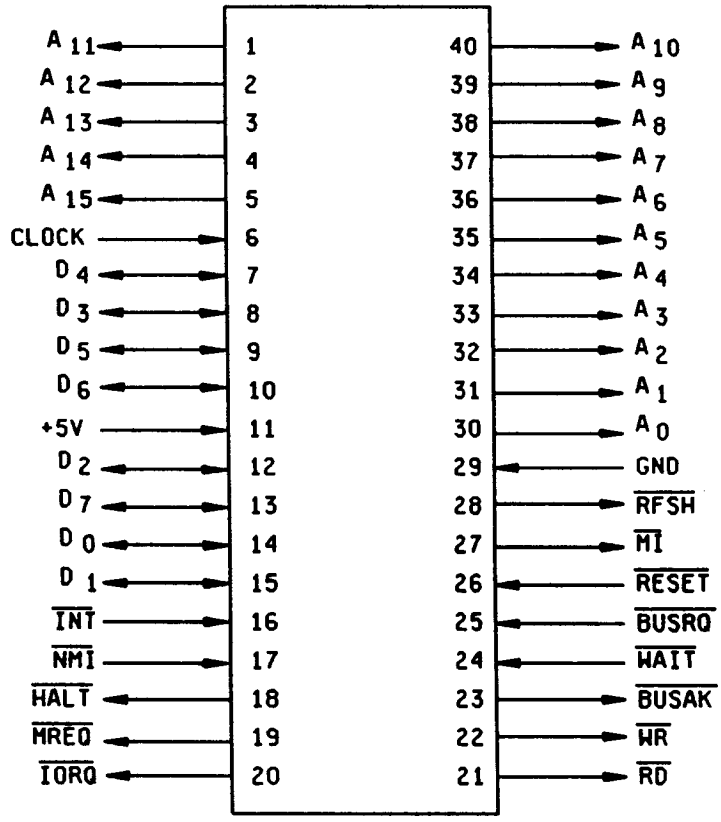

FIGURE 1. Terminal connections (pin assignment).

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Device types 01, 02 and 03
Cases X and Y

Device type	01, 02 and 03
Case outline	X and Y
Terminal number	Terminal symbol
1	A11
2	A12
3	A13
4	A14
5	A15
6	N/C
7	CLK
8	D4
9	D3
10	D5
11	D6
12	N/C
13	VCC
14	D2
15	D7
16	D0
17	D1
18	$\overline{INT}$
19	$\overline{NMI}$
20	$\overline{HALT}$
21	$\overline{MREQ}$
22	$\overline{IORQ}$

Device type	01, 02 and 03
Case outline	X and Y
Terminal number	Terminal symbol
23	$\overline{RD}$
24	N/C
25	$\overline{N/C}$
26	$\overline{WR}$
27	$\overline{BUSAK}$
28	$\overline{WAIT}$
29	$\overline{BUSRQ}$
30	$\overline{RESET}$
31	$\overline{MI}$
32	$\overline{RFSH}$
33	GND
34	A0
35	A1
36	A2
37	A3
38	A4
39	A5
40	A6
41	A7
42	A8
43	A9
44	A10

FIGURE 2. Terminal connections. - Continued.

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Device types 01, 02, and 03

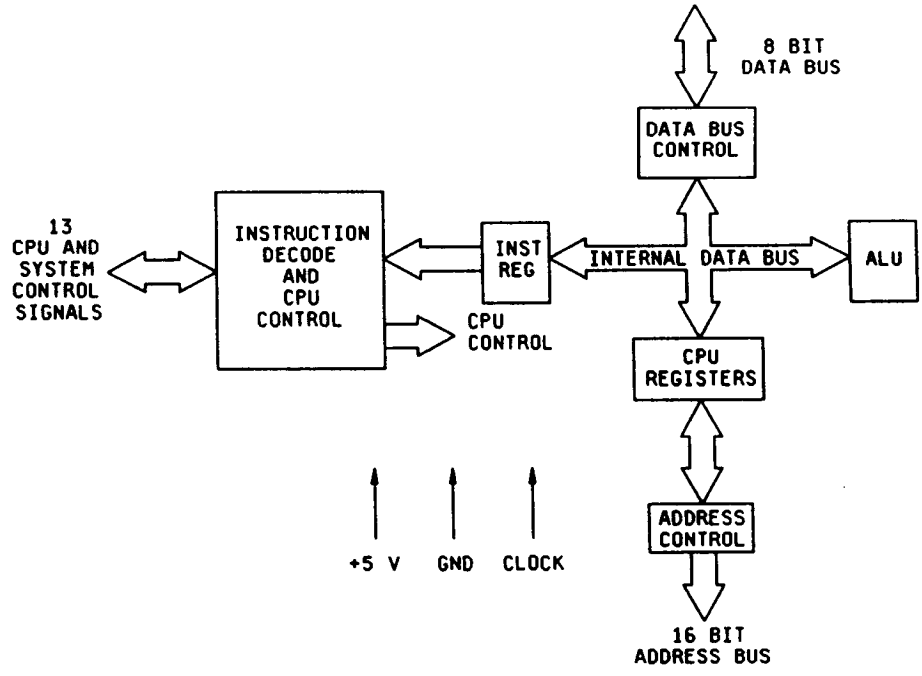

FIGURE 2. Block diagram.

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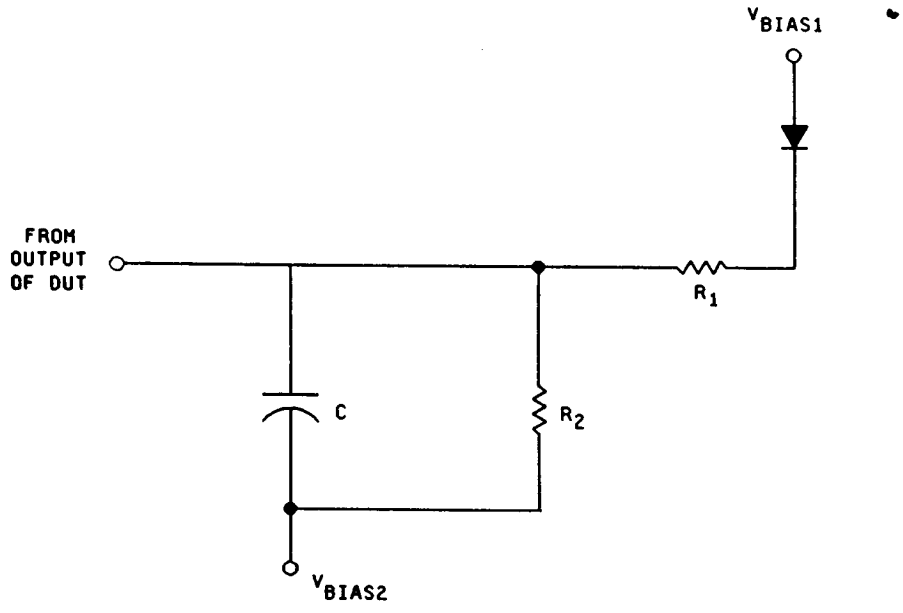

NOTES:
1. C = 140 pF ±20% for pins 1-5, 7-10, 12-15, 18-23, 27, 28, 30-40.
2. R_1 = 550Ω ±5%, R_2 = 9.6 kΩ ±5%.
3. All diodes are 1N3064 or equivalent.
4. For AC testing:
   V_{Bias1} = 2.1 V ±5%, V_{Bias2} = 0 V.

   For Tristate tests:

   a. Logic "1" to tristate (address, data and control out pin)
      V_{Bias1} = 1.0 V ±5%, V_{Bias2} = -10 V ±5%.

   b. Logic "0" to tristate (address and data pins only)
      V_{Bias1} = 4.5 V ±5%, V_{Bias2} = 0 V.

FIGURE 3. Output load circuit for functional and ac testing, all device types.

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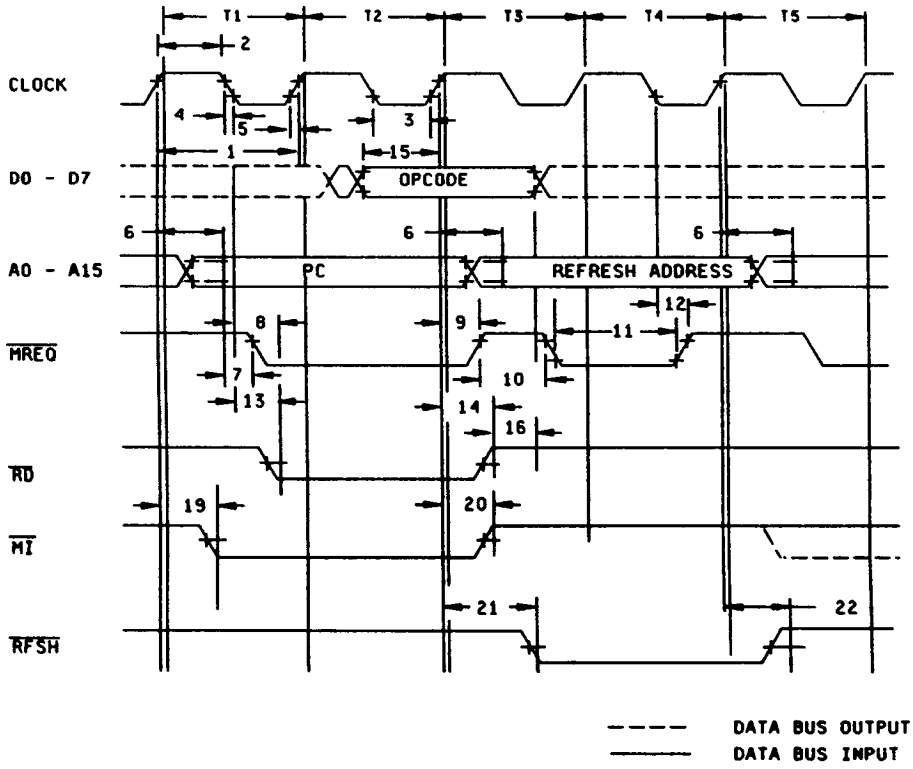

Instruction opcode fetch ($\overline{MI}$ cycle)

FIGURE 4. Timing diagram.

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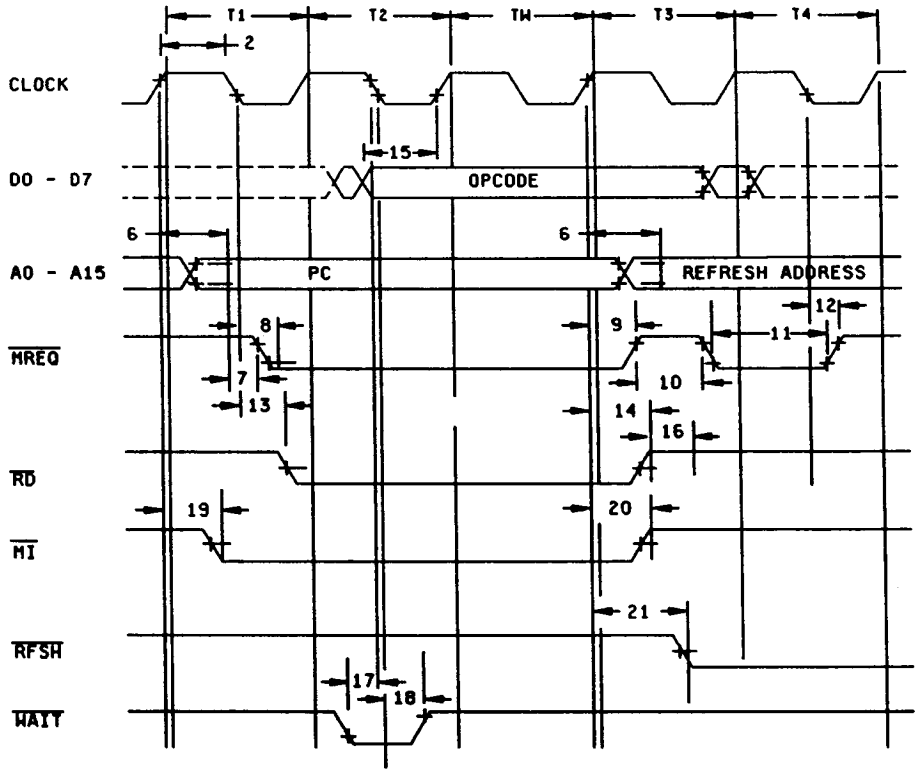

Instruction opcode fetch w/wait (s)

FIGURE 4. Timing diagram - Continued.

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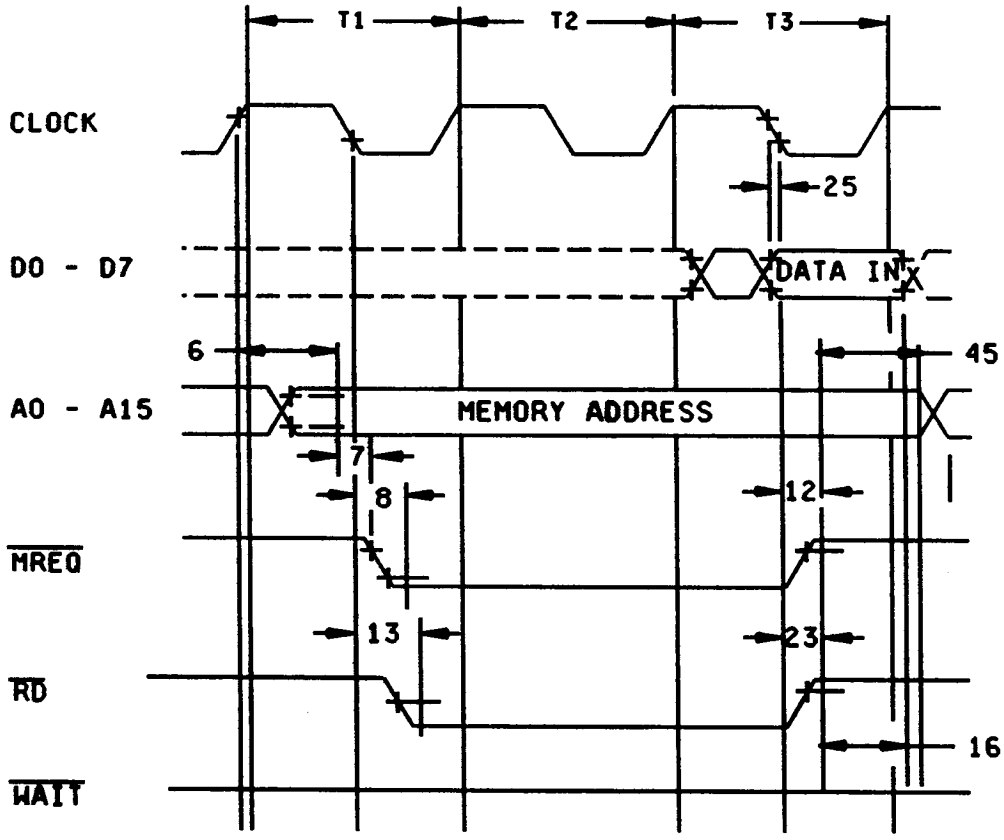

Memory read cycle

FIGURE 4. Timing diagram - Continued.

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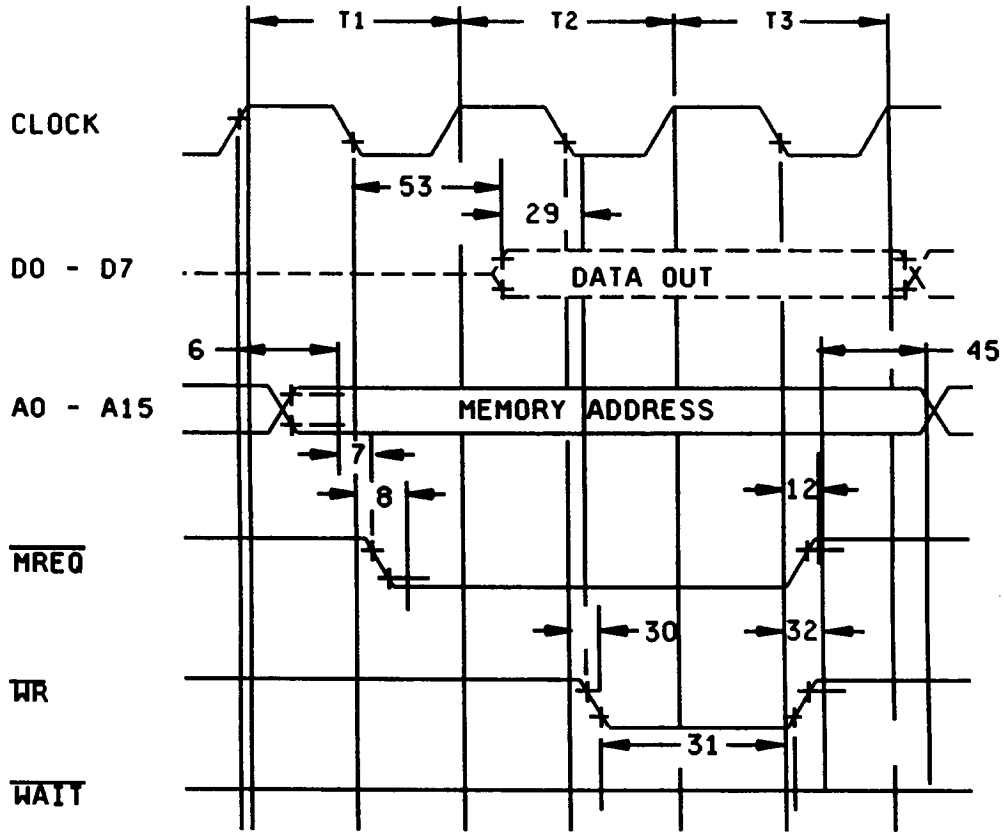

Memory write cycle

FIGURE 4. Timing diagram - Continued.

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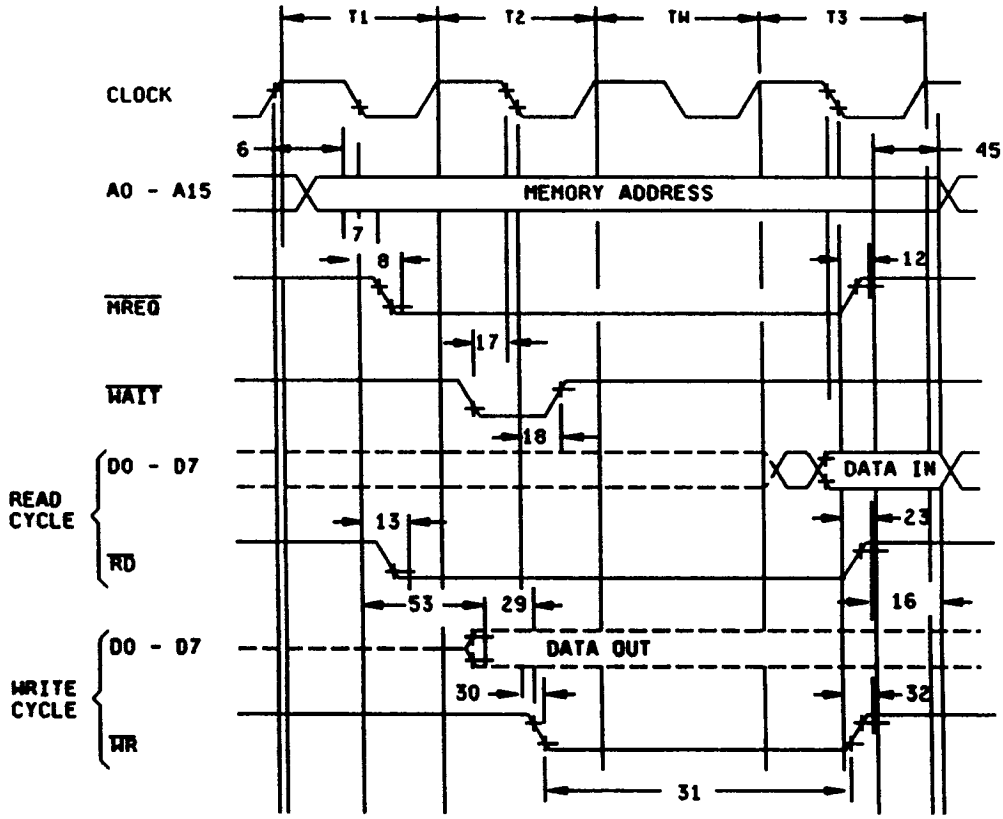

Memory read/write cycle w/wait (s)

FIGURE 4. Timing diagram - Continued.

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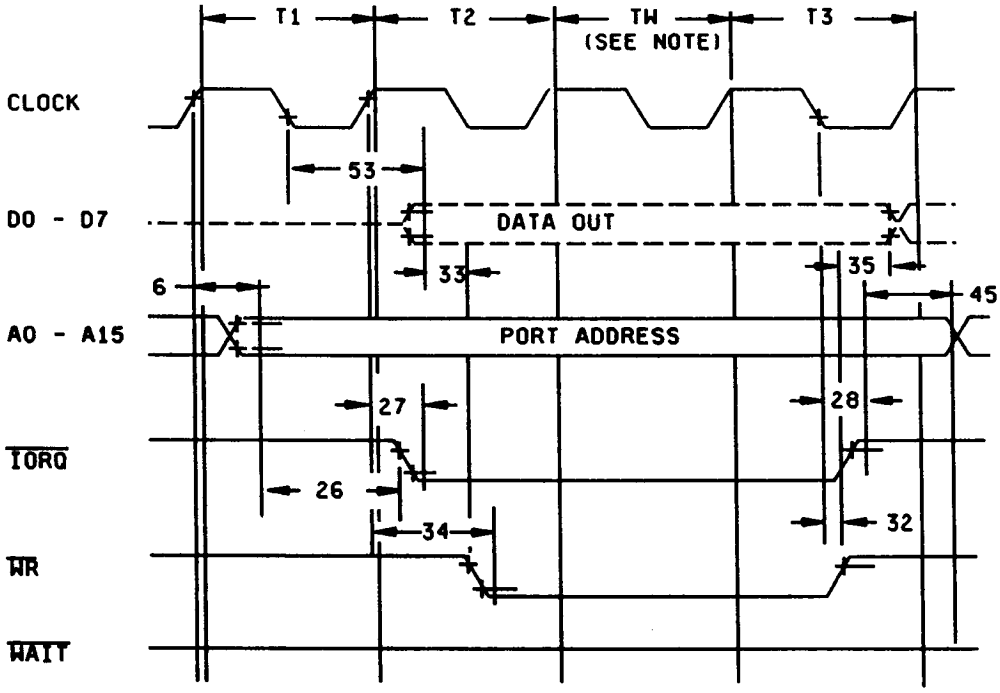

NOTE: Automatically inserted wait state by CPU

TW* - automatically inserted wait state by CPU

I/O write cycle

FIGURE 4. Timing diagram - Continued.

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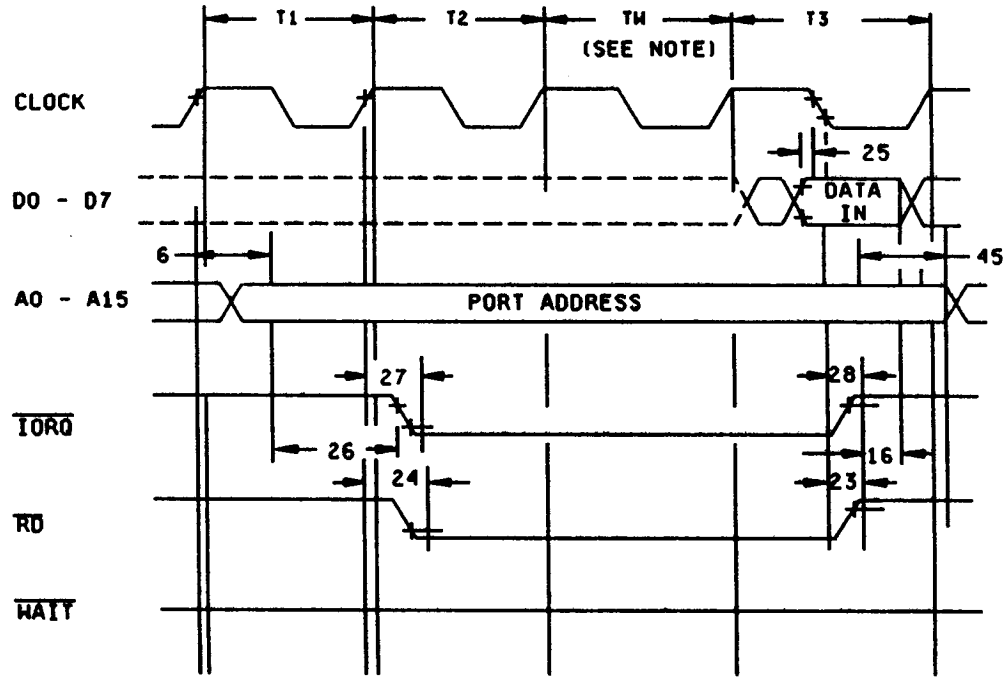

NOTE: TW automatically inserted wait state by CPU

I/O read cycle

FIGURE 4. Timing diagram - Continued.

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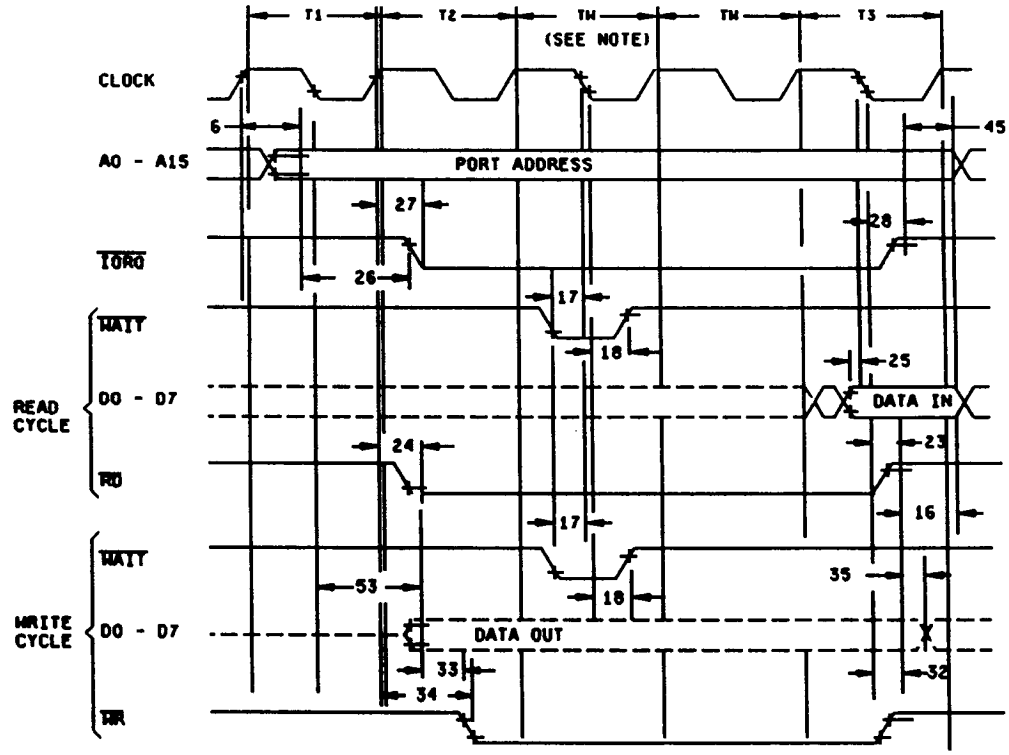

NOTE: TW automatically inserted wait state by CPU.

I/O read/write cycle w/wait (s)

FIGURE 4. Timing diagram - Continued.

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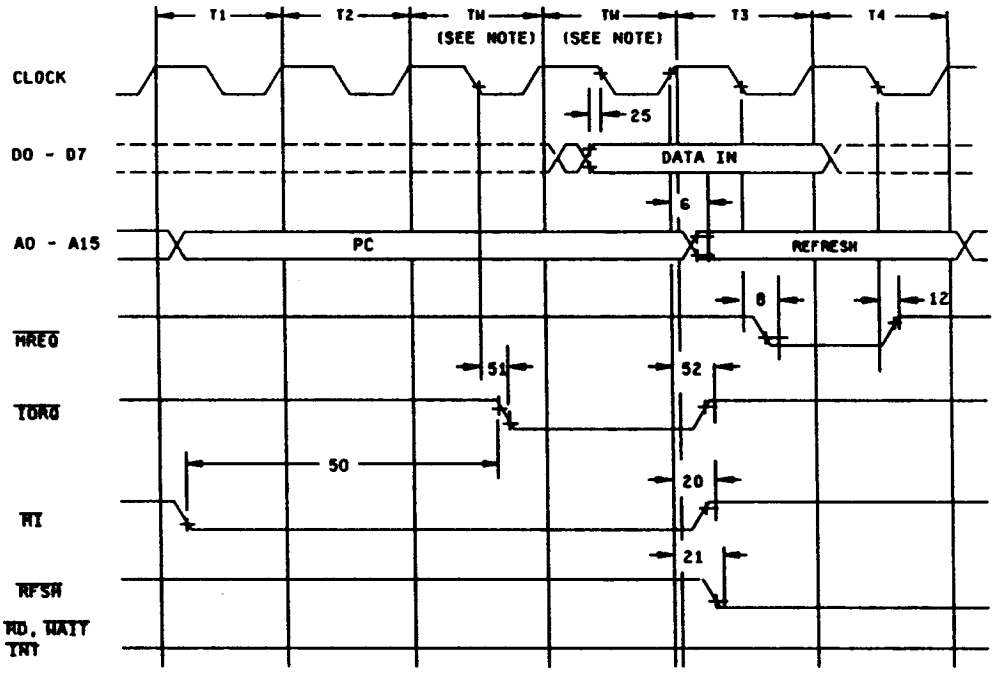

NOTE: TW automatically inserted wait state by CPU.

Basic timing cycles with wait states expand in multiples of T_{c3}.

Interrupt acknowledge cycle

FIGURE 4. Timing diagram - Continued.

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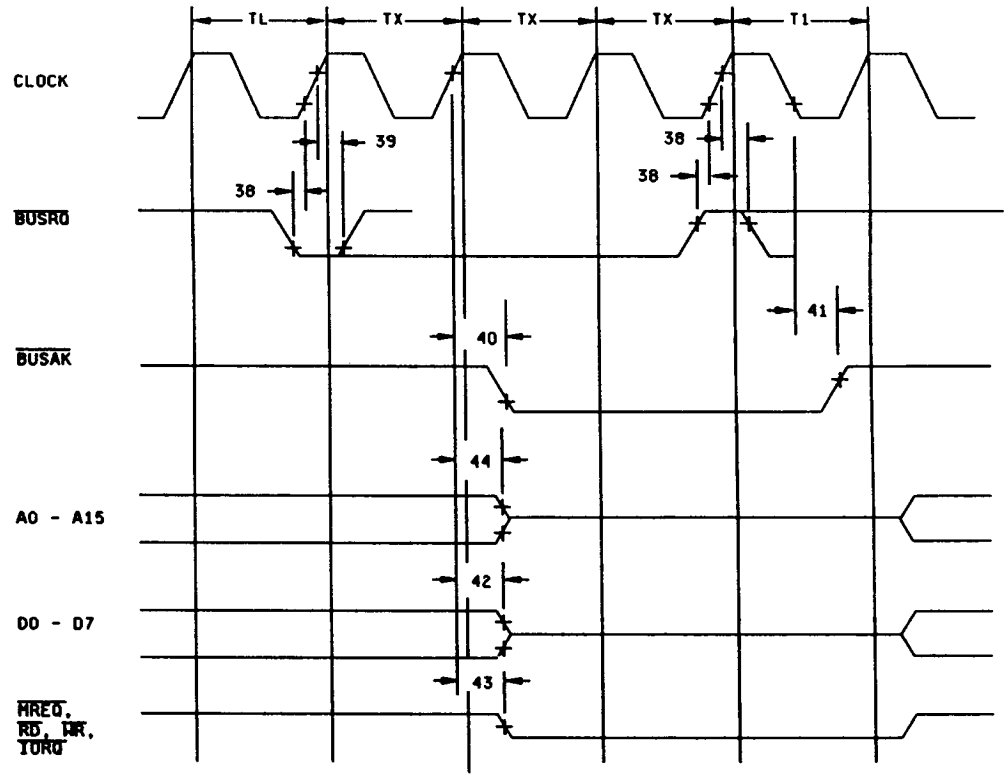

NOTE: TL = Last state of any M cycle
TX = An arbitrary clock cycle used by requesting device.

Output timing

BUS request/acknowledge cycle

FIGURE 4. Timing diagram - Continued.

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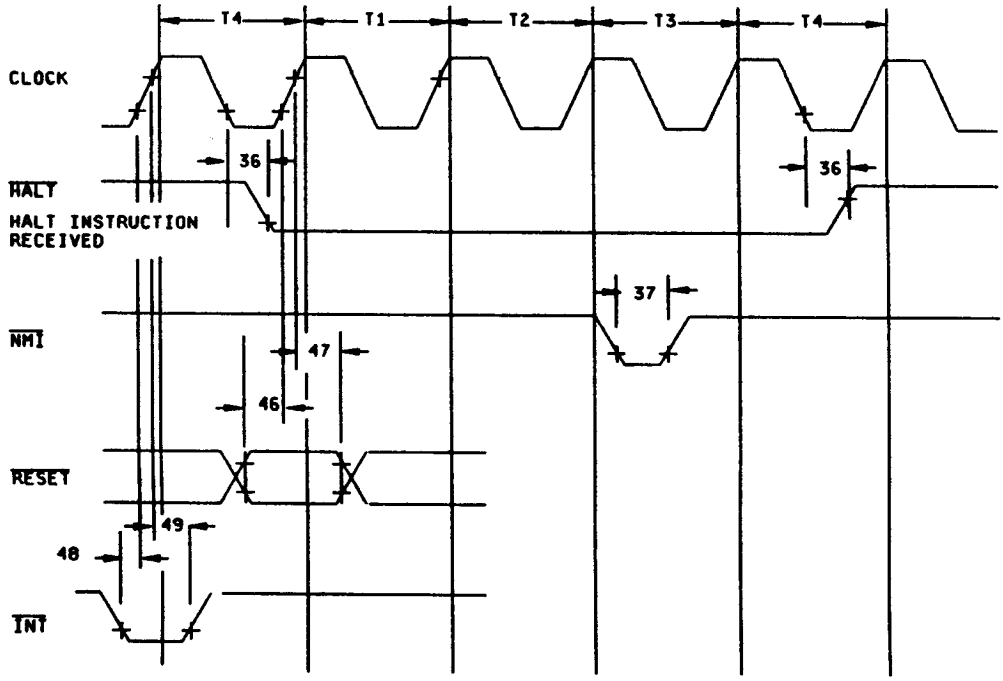

NOTE: Signals are not necessarily related.

Output timing

FIGURE 4. Timing diagram - Continued.

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4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroups 4 (C_C, C_I and $C_{I/O}$) measurements shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of five devices with zero rejects shall be required.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (per method 5005, table I)			Subgroups (per MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9
Final electrical parameters (see 4.2)	1,2,3, 7,8,9 10,11 1/	1,2,3, 7,8, 10,11 1/	1,2,3, 7,8, 10,11 2/	1,2,3, 7,8, 10,11 1/	1,2,3, 7,8, 10,11 2/
Group A test requirements (see 4.4)	1,2,3,4, 7,8, 9,10,11	1,2,3,4, 7,8, 10,11	1,2,3,4, 7,8, 9,10,11	1,2,3,4, 7,8, 9,10,11	1,2,3,4, 7,8, 9,10,11
Group B end-point electrical parameters (see 4.4)	---	---	1,7,9	---	
Group C end-point electrical parameters (see 4.4)	1,7,9	1,7,9	---	1,7,9	1,7,9
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table II herein. For device class S steady-state life tests, the test circuit shall be submitted to the qualifying activity.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A,B,C or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class B, the test circuit shall be submitted to the qualifying activity. For device classes M and B, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

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4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA environment and level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-8526.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

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6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510 and MIL-STD-1331 and in Table III.

Table III. Pin description.

A0 - A15 (Address Bus)	Tristate output, active high. A0 - A15 constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes) data exchanges for I/O device data exchanges. I/O addressing uses the 8 lower address bits to allow the user to directly select up to 256 input or 256 output ports. A0 is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address.
D0 - D7 (Data Bus)	Tristate input/output, active high. D0 - D7 constitute an 8-bit bidirectional constitute an 8-bit bidirectional data bus. The data bus used for data exchanges with memory and I/O devices.
$\overline{M1}$ (Machine Cycle One)	Output, active low. $\overline{M1}$ indicates that the current machine cycle is the OP code fetch cycle of an instruction execution. Note that during execution of 2-byte op-code, $\overline{M1}$ is generated as each op code byte is fetched. These two byte op-codes always begin with DBH, DDH, EDH, or FDH. $\overline{M1}$ also occurs with IORQ to indicates an interrupt acknowledge cycle.
$\overline{MREQ}$ (Memory Request)	Tristate output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.
$\overline{IORQ}$ (Input/Output Request)	Tristate output, active low. The $\overline{IORQ}$ signal indicates that the lower half of the address bus holds valid I/O address for an I/O read or write operation. An IORQ signal is also generated with an M1 signal when an interrupt response vector can be placed on the data bus. Interrupt acknowledge operations occur during M1 time while I/O operations never occur during M1 time.
$\overline{RD}$ (Memory Read)	Tristate output, active low. $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The address I/O device or memory should use this signal to gate data onto the CPU data bus.
$\overline{WR}$ (Memory Write)	Tristate output, active low. $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored in the address memory or I/O device.
$\overline{RFSH}$ (Refresh)	Output, active low. $\overline{RFSH}$ indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current MREQ signal should be used to do a refresh read to all dynamic memories.
$\overline{HALT}$ (HALT State)	Output, active low. $\overline{HALT}$ indicates that the CPU has executed a HALT software instruction and is awaiting either a nonmaskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOPs to maintain memory refresh activity.
$\overline{WAIT}$	Input, active low. $\overline{WAIT}$ indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. This signal allows memory or I/O devices of any speed to be synchronized to the CPU.

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Table III. Pin description - Continued.

$\overline{\text{INT}}$ (Interrupt Request)	Input, active low. The interrupt request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software-controlled interrupt enable flip-flop (IFF) is enabled and if the BUSRQ signal is not active. When the CPU accepts the interrupt, an acknowledge signal (IORQ during M1 time) is sent out at the beginning of the next instruction cycle.
$\overline{\text{NMI}}$ (Non-maskable Interrupt)	Input, negative edge triggered. The non-maskable interrupt request line has a higher priority than INT and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. NMI automatically forces the CPU to restart to location 0066H. The program counter us automatically saved in the external stack so that the users cab return to the program that was interrupted. Note that continuous WAIT cycles can prevent the current instruction from ending, and that a BUSRQ will override a NMI.
$\overline{\text{RESET}}$	Input, active low. RESET forces the program counter to zero and initializes the CPU initialization includes: 1. Disable the interrupt enable flip-flop. 2. Set Register I = 00H. 3. Set Register R = 00H. 4. Set Interrupt Mode 0. During reset time, the address bus and data bus go to a high impedance state and all control output signals go to the inactive state. RESET must be active for a minimum of three clock cycles.
$\overline{\text{BUSRQ}}$ (Bus Request)	Input, active low. The bus request signal is used to request the CPU address bus, and tristate output control signals to go to a high-impedance state so that other devices can control these buses. When BUSRQ is activated, the CPU will set these buses to a high impedance state as soon as the current CPU machine cycle is terminated.
$\overline{\text{BUSAK}}$ (Bus Acknowledge)	Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus, and tristate control bus signals have been set to their high impedance state and the external device can now control these signals.
CLOCK	Input. Single phase +5 V clock.

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6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

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APPENDIX

SUPERSESSION

10. Scope

10.1 Scope. This appendix contains the PIN supersession information to support the one part-one part number system. SMD 5962-38480 supersedes Military Specification MIL-M-38510/480. For new designs, after the date of this document the new PIN shall be used in lieu of the old PIN. For existing designs prior to the date of this document the new PIN can be used in lieu of the old PIN. This is a mandatory part pf the specification, The information contained herein is intended for compliance, The PIN supersession data shall be as follows:

Old PIN	NEW PIN
M38510/48001BQX	5962-3848001MQX
M38510/48001BXX	5962-3848001MXX
M38510/48001BYX	5962-3848001MYX
M38510/48002BQX	5962-3848002MQX
M38510/48002BXX	5962-3848002MXX
M38510/48002BYX	5962-3848002MYX
M38510/48003BQX	5962-3848003MQX
M38510/48003BXX	5962-3848003MXX
M38510/48003BYX	5962-3848003MYX

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

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