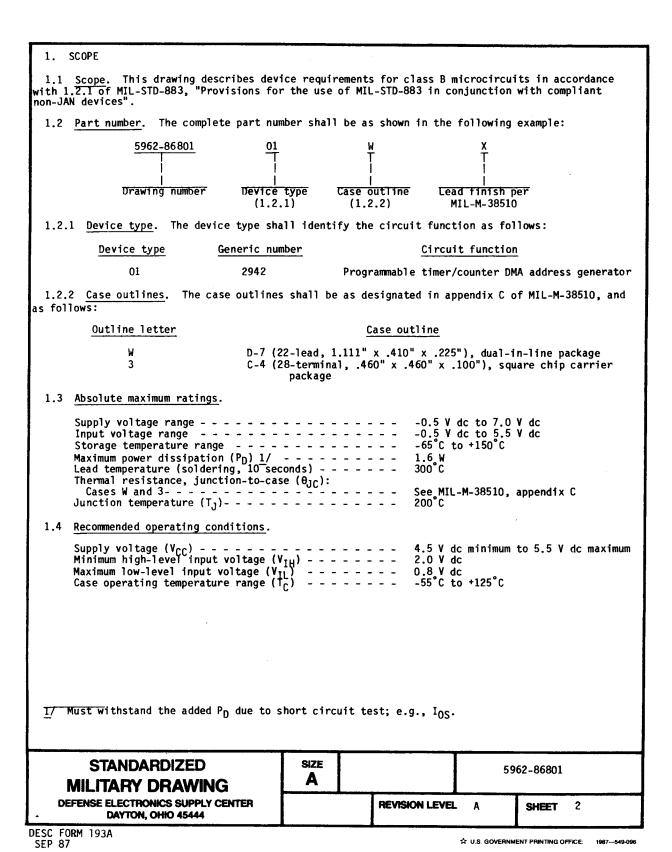
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REV SHEET REV SHEET REV STA	ATUS EETS VA NDA MILIT	RC	REV SHEET		A 1 PRE	A 2 PARE	A 3 ED BY	A 4	A 5	A	7	 	9	10 11CR	DEFE	12	13 ELE DAY	14 CTRO CTON	DNIC ONIC OHI	S SU IO 45	ROGR	RAMM/	ABLE		
REV SHEET REV SHEET OF SHI PMIC N	ATUS EETS VA NDA MILIT DRAV	REFAIL	REV SHEET		A 1 PRE	A 2 PARE	A 3 ED BY	A 4	A 5	A 6	7	 	9	10 MICR	DEFE	12 ENSE RCUI OUNT HIC	TS, ER SIL	DIG DMA ICON	DNIC , OHI	S SU IO 45	ROGR	RAMM/	ABLE		
REV SHEET REV SHEET REV STA	ATUS EETS VA MILIT DRAV RAWING E BY ALL	RC AF	REV SHEET DIZED RY IG	E	A 1 PRE	A 2 PARE CKECKEC ROVE	A 3 S D BY	A 4	A 5	A 6	7	 	9	110 MICR FIME MONO	DEFE	RCUI OUNT HIC	TS, ER I	DIG DMA ICON	DNIC , OHI	S SU IO 45	ROGR GEN	RAMM/ NERA	ABLE TOR,		
REV SHEET REV SHEET OF SHI PMIC N STA	ATUS EETS VA MILIT DRAV RAWING E BY ALL D AGENC	RC AF	REV SHEET DIZED RY IG	E	A 1 PRE CHE	A 2 PARE CKECKEC ROVE	A 3 3 S BY APRI	A 4	A 5	A 6	7	 	9	110 MICR FIME	DEFE	RCUI OUNT HIC	TS, ER I	DIG DMA ICON	DNIC , OHI	S SU IO 45	ROGR GEN	RAMM/ NERA	ABLE TOR,		301

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5962-E822

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2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the Issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510

- Microcircuits, General Specification for

STANDARD

MILITARY

MIL-STD-883

- Test Methods and Procedures for Microelectronics

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

- 3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.
- 3.2 Design, construction, and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-M-38510 and herein.
 - 3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.
 - 3.2.2 Block diagram. The block diagram shall be as specified on figure 2.
 - 3.2.3 Function table. The function table shall be as specified on figure 3.
 - 3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.
- 3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.
- 3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein
- 3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444 SIZE A FREVISION LEVEL A SHEET 3

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TA	BLE I. E	lectr	ical perfo	rmanc	e characteris	tics.			
Test	Symbol		Cond -55°C < T 4.5 V <	itions CC <u><</u>	5 125°C 5.5 V	Group A subgroups	Limits Min Max 		Unit
Output high voltage	v _{OH}	V _{CC} =	4.5 V, V	[N = \	I _{IH} or V _{IL} ,	1, 2, 3	2.4	1 1	γ
Output low voltage	V _{OL1}	VIN	= 4.5 V, = V _{IH} or V	/IL	WCO, ACO I _{OL} = 8.0 mA	1, 2, 3		0.5	٧
	V _{OL2}] 			D _{O-7} , DONE I _{OL} = 16 mA	1, 2, 3		0.5	٧
Input high voltage	V _{IH}	1/	1/			1, 2, 3	2.0		٧
Input low voltage	VIL	1/			1, 2, 3		0.8	٧	
Input clamp voltage	v _{IC}	V _{CC} = 4.5 V, I _{IN} = -18 mA			1, 2, 3		-1.5	٧	
Input low current	IILI	VCC VIN	= 5.5 Y, = 0.5 Y		D ₀₋₇	1, 2, 3		-0.15	mA
	IIL2] *** 		[*] 	All others	1, 2, 3		-0.8	mA
Input high current	I _{IH1}	V _{CC}	= 5.5 V, = 2.7 V		D ₀₋₇	1, 2, 3		150	μА
	I _{IH2}] •" 			All others	1, 2, 3		40	μА
Output leakage current on DONE	ICEX	VCC	cc = 5.5 V, V ₀ = 5.5 V			1, 2, 3		250	μА
Input high current	I IH3	VCC	= 5.5 V,	VIN =	5.5 V	1, 2, 3		1.0	mA
Output short-circuit current	Ios	Vcc	= 6.0 V,	V ₀ = ().5 V <u>2</u> /	1, 2, 3	-30	-85	mA
Output OFF current	I _{OZH}	OE =	2.4 V, = 5.5 V,		V _{OUT} = 2.4 V	1, 2, 3		150	μА
	IOZL	D ₀₋₇ 	•	[*] 	V _{OUT} = 0.5 V	1, 2, 3		-150	μА
See footnotes at end of ta	ble.			•					
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	TABLE I. E	lectrical	performance characteristics -	Continued	•		
Test		 Symbol 	Conditions -55°C < T _C < +125°C 4.5 V < V _{CC} < 5.5 V	 Group A subgroups 		mits Max 	Unit
Power supply c	urrent	Icc1	V _{CC} = 5.5 V	1, 2, 3		285	mA
		I _{CC2}	V _{CC} = 5.5 V, T _C = +125°C] 2 		205	mA
Functional tes	ts		See 4.3.1(c)	7,8			
Setup times	D ₀₋₇	t _{s1}	 Setup and hold times are relative to clock LOW-to-HIGH	9, 10, 11	27		ns
	I ₀₋₃ , TE	t _{s2}	l transition, see figure 4 	 9, 10, 11	 49 	 	l ns
	ACI, WCI	lt _s 3		 9, 10, 11 	34	 	ns
Hold times	D ₀₋₇	t _{h1}	1		7.0] 	l ns
	ACT, WCT	t _{h2}		9, 10, 11	5.0		l ns
Propagation delay times	ACT to ACO	t _{PD1}	See figure 4	9, 10, 11		21	ns
·	WCI to WCO	t _{PD2}		9, 10, 11		 21 	l ns
	WCI to DONE 3/	t _{PD3}	 	9, 10, 11		 54 	ns
	I I ₀₋₃ to D ₀₋₇	t _{PD4}		9, 10, 11		 41 	ns
	CP to ACO or WCO	lt _{PD5}	 	9, 10, 11	 	 64 	ns
	CP to DONE 4/	t _{PD6}		9, 10, 11		88	ns
	CP to D ₀₋₇	t _{PD7}		9, 10, 11	 	 68 	ns
	TE to D ₀₋₇	t _{PD8}		9, 10, 11		 41 	ns
See footnotes	at end of table.						
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Test	Symbol	Conditions	Group A		imits_	_ Unit
	 	Conditions $ \begin{array}{ccc} & \text{Conditions} \\ & -55^{\circ}\text{C} & \leq \text{T}_{\text{C}} & \leq +125^{\circ}\text{C} \\ 1 & 4.5 \text{ V} & \leq \text{V}_{\text{CC}} & \leq 5.5 \text{ V} \\ \end{array} $	subgroups 	Min	Max	
Output enable time, from OE to D _{O-7}	t _{en}	 See figure 4 	9, 10, 11		30	ns
Output disable time, from OE to D _{O-7}	tdis		9, 10, 11		30	ns
Minimum clock LOW time	tpWL	 	9, 10, 11	23		ns
Minimum clock HIGH time	tpWH] -	9, 10, 11	35		ns
Maximum clock frequency	f _{MAX}	<u> </u> 	9, 10, 11	17		MHz

- 1/ These input levels provide no guaranteed noise immunity and should only be static tested in a noise-free environment (not functionally tested).
- $\frac{2}{}$ Not more than one output should be tested at a time. Duration of short circuit test should not exceed one second.
- $\underline{3}/\overline{\text{WCI}}$ to DONE occurs only in control modes 0 and 1.
- 4/ CP to DONE occurs only in control modes 0, 1, and 2.

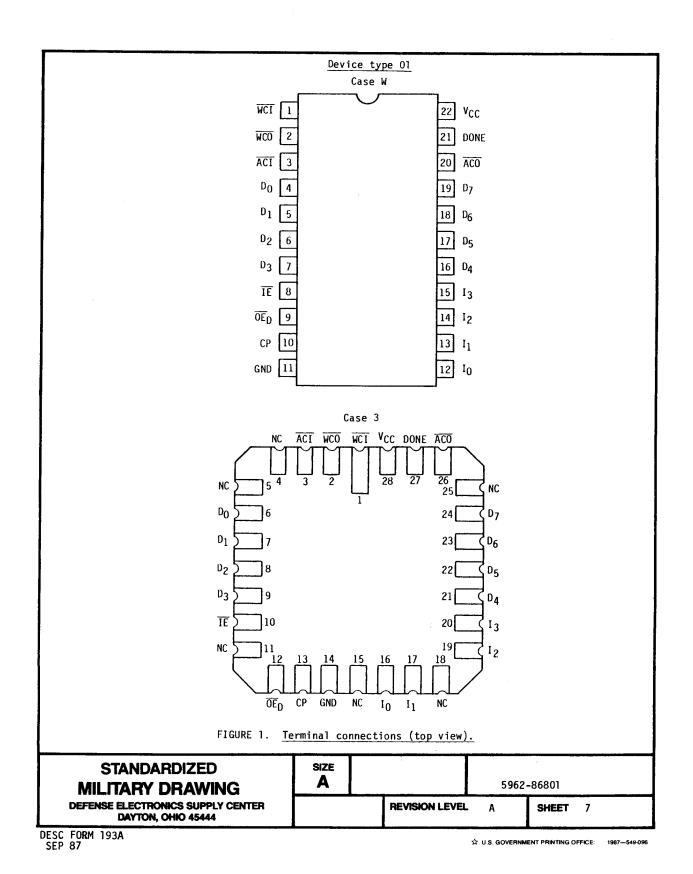
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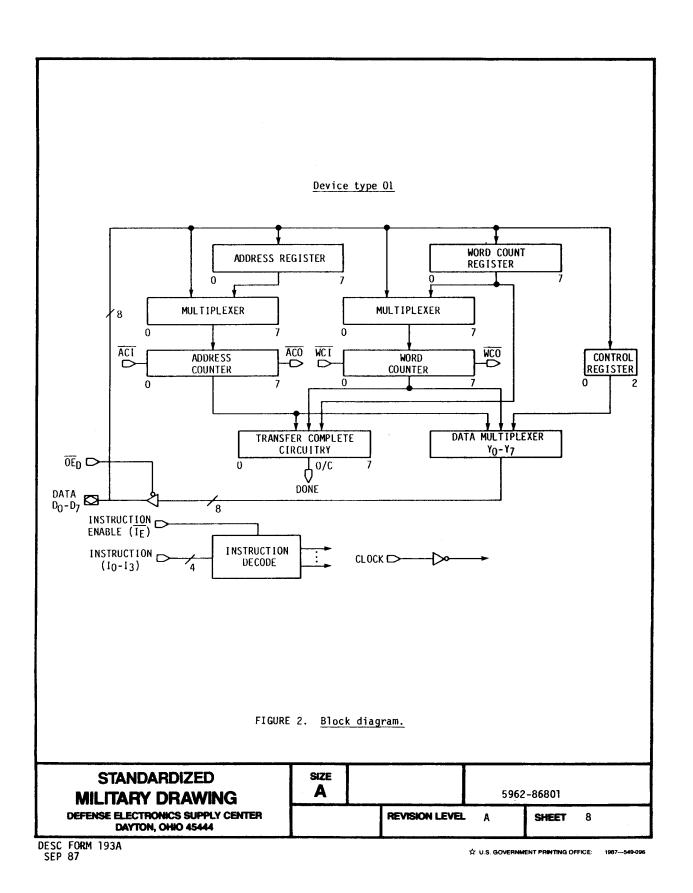
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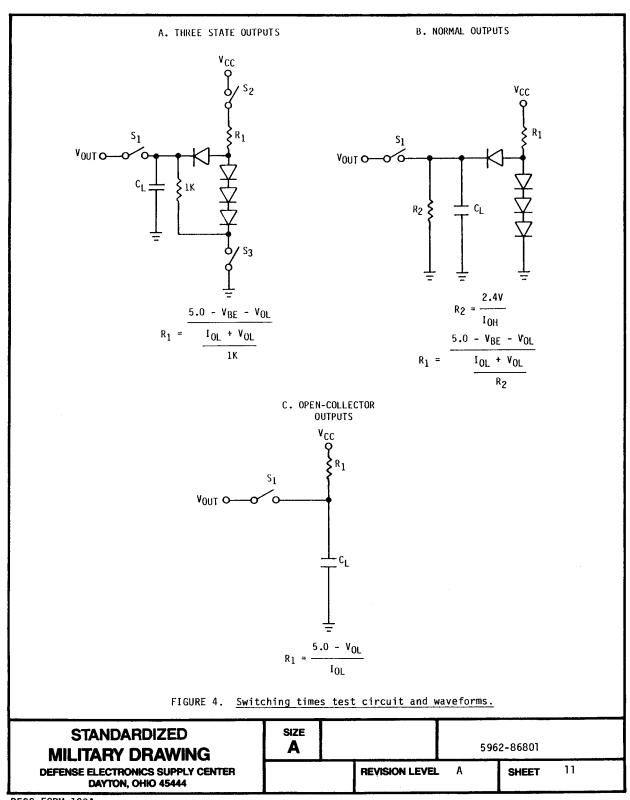


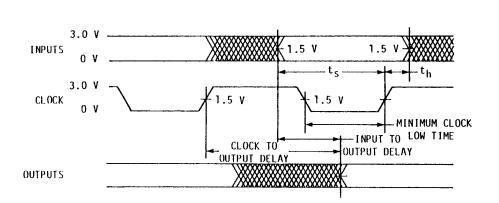
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ΙĒ	 I ₀₋₃ (Hex)	 Function 	Mne- monic	Control mode		 Word counter (WC) 	 Address register (AR) 		 Control register (CR) 	Data multiplexer output (D)	
L	0 	 WRITE CONTROL REGISTER	WRCR	0,1,2,3	l HOLD 	HOLD	I HOLD	HOLD	 D ₀₋₂ > CR 	FORCED HIGH	
L	1	READ CONTROL REGISTER	RDCR	0,1,2,3	l HOLD	 HOLD 	HOLD	HOLD 	HOLD !	CONTROL REGISTER	
L	2	READ WORD COUNTER	RDWC	0,1,2,3	 HOLD 	HOLD	 HOLD 	HOLD	HOLD	WORD COUNTER	
L	3	READ ADDRESS COUNTER	RDAC	0,1,2,3	HOLD	HOLD	HOLD	HOLD	HOLD	ADDRESS COUNTER	
L	4	 - REINITIALIZE COUNTERS	REIN	0,2,3	HOLD	 WR → WC	l HOLD I	IAR > AC	HOLD I	ADDRESS COUNTER	
]]] 	1	HOLD	 ZERO > WC 	 HOLD 	lAR → AC` I	HOLD I	ADDRESS COUNTER	
L	 5 	LOAD COUNT	LDAD	0,1,2,3	HOLD	I HOLD	D > AR 	D > AC	HOLD	WORD COUNTER	
L	6	LOAD WORD COUNT	LDWC	0,2,3	D → WR	l D → WC	HOLD	HOLD	HOLD HOLD	FORCED HIGH	
	 		 	1	D → WR	 ZERO > WC 	HOLD	HOLD	HOLD	FORCED HIGH	
L	 	ENABLE Counters	ENCT	0,1,3	HOLD	 ENABLE 	HOLD	ENABLE	HOLD	ADDRESS COUNTER	
	1 1 1	 	 	2 	HOLD	HOLD	HOLD	ENABLE	HOLD HOLD 	ADDRESS COUNTER	
н	0-7	INSTRUCTION DISABLE		0,1,3	HOLD	ENABLE	HOLD	ENABLE	HOLD HOLD	ADDRESS COUNTER	
] 		 	2	HOLD	HOLD	HOLD	ENABLE	HOLD	ADDRESS COUNTER	
				FIGURE 3.		on table.					
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	FENSE EL	ECTRONICS SUPPI AYTON, OHIO 45444	Y CENTI	ER -		REVI	SION LEVE	<u> </u>			

TE	 I ₀₋₃ (Hex)	 Function 	Mne- monic	Control mode 	Word register (WR)	Word Word counter (WC)	 Address register (AR)	 Address counter (AC)	 Control register (CR)	Data multiplexe output (D)
L	8	WRITE CONTROL! REGISTER, T/C	WCRT	0,1,2,3 	HOLD	ENABLE	 HOLD 	ENABLE	 D ₀₋₂ > CR 	CONTROL REGISTER
L	9	REINITIALIZE ADDRESS COUNTER	REAC	0,1,2,3	HOLD	 ENABLE 	i HOLD	AR > AC	HOLD	ADDRESS COUNTER
L	A	READ WORD COUNTER, T/C	RWCT	0,1,2,3	HOLD	 ENABLE 	HOLD	ENABLE	HOLD	WORD COUNTER
L	Г В 	READ ADDRESS COUNTER, T/C	RACT	0,1,2,3	HOLD	ENABLE	HOLD	 ENABLE 	HOLD I	ADDRESS COUNTER
L	C	 REINITIALIZE ADDRESS AND	RAWC	0,2,3	 HOLD 	WR → WC	 HOLD 	AR > AC	HOLD	ADDRESS COUNTER
		WORD COUNTERS 		1	HOLD	 ZERO → WC 	 HOLD 	AR > AC	 HOLD 	ADDRESS COUNTER
L	D 	LOAD ADDRESS, T/C	LDAT	0,1,2,3	HOLD	ENABLE	D > AR	D > AC	HOLD I	WORD COUNTER
L	 E	LOAD WORD COUNT, T/C	LWCT	0,2,3	D → WR	i D → WC	HOLD	ENABLE	HOLD	FORCED HIG
	 	 		 1 	D → WR	 ZERO → WC 	l HOLD i	ENABLE	HOLD	FORCED HIG
L	 F	 REINITIALIZE WORD	REWC	0,2,3	 HOLD 	 WR ≯ WC 	 HOLD 	ENABLE	 HOLD 	WORD COUNTER
	 	COUNTER 		1	 HOLD 	 ZERO → WC 	HOLD	ENABLE	HOLD	WORD COUNTER
Н	 8-F	INSTRUCTION DISABLE, T/C		0,1,3	 HOLD 	ENABLE	HOLD	ENABLE	HOLD	WORD COUNTER
	1 			2	HOLD	HOLD	HOLD	ENABLE	HOLD	WORD COUNTER
			FIGU	RE 3. <u>F</u> u	inction t	able - Cor	itinued.		·	
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Test output loads

Pin name	Test circuit	R1 (ohms)	R2 (ohms)
D ₀₋₇	٨	220	1.0K
ACO	В	470	2.4K
DONE	С	270	-
WCO	В	470	2.4K

NOTES:

- 1. $C_L = 50$ pFincludes scope probe, wiring and stray capacitance without device in test fixture.
- S₁, S₂, S₃ are closed during function tests and all AC tests except output enable tests.
 S₁ and S₃ are closed while S₂ is open for ten test.
 C_L = 5.0pf for output disable tests.

FIGURE 4. Switching times test circuit and waveforms - Continued.

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- 3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.
- 3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.5 herein).
- 3.8 <u>Verification and review.</u> DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.
 - 4. QUALITY ASSURANCE PROVISIONS
- 4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).
- 4.2 <u>Screening</u>. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:
 - a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).
 - (2) $T_A = +125^{\circ}C$, minimum.
 - b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.
- 4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.
 - 4.3.1 Group A inspection.
 - a. Tests shall be as specified in table II herein.
 - b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
 - c. Subgroup 7 and 8 tests sufficient to verify the function table.
 - 4.3.2 Groups C and D inspections.
 - a. End-point electrical parameters shall be as specified in table II herein.
 - b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).
 - (2) $T_A = +125$ °C, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	
Final electrical test parameters (method 5004) 	1*, 2, 3, 7, 8, 9, 10**, 11**
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3, 7, 8

PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

- 6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.
- 6.2 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.
- 6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER

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^{**} Subgroups 10 and 11, if not tested, shall be guaranteed to the limits specified in table I.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

	Vendor CAGE number	Vendor similar part number <u>1</u> /
5962-8680101WX	34335	AM2942/BWA
5962-86801013X	34335	AM2942/B3A

1/ <u>Caution</u>. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

34335

Vendor name and address

Advanced Micro Devices, Incorporated 901 Thompson Place Sunnyvale, CA 94088

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