REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																									
SHEET																									
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SHEET	22	23																							
REV STATUS OF SHEETS	REV																								
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21			

PMIC N/A

STANDARDIZED MILITARY DRAWING

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AMSC N/A

PREPARED BY

CHECKED BY

APPROVED BY

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21 JUNE 1988

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, CMOS 8K X 8
UV EPROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-87515

SHEET 1 OF 23

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E225

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-87515	01	J	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	See 6.4	8K x 8 UV EPROM	45 ns
02	See 6.4	8K x 8 UV EPROM	55 ns
03	See 6.4	8K x 8 UV EPROM	70 ns
04	See 6.4	8K x 8 UV EPROM	90 ns
05	See 6.4	8K x 8 UV EPROM	45 ns
06	See 6.4	8K x 8 UV EPROM	55 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
J	D-3 (24 lead, 1.290" x .610" x .225"), dual-in-line package 1/
K	F-6 (24 lead, .640" x .420" x .090"), flat package 1/
L	D-9 (24 lead, 1.280" x .310" x .200"), dual-in-line package 1/
3	C-4 (28 terminal, .460" x .460" x .100"), square chip carrier package 1/

1.3 Absolute maximum ratings.

Storage temperature	-65°C to +150°C
Voltages on any pin with respect to ground	-0.5 V dc to +7.0 V dc
V_{PP} with respect to ground	-0.5 V dc to +14.0 V dc
Maximum power dissipation (P_D) 2/	1 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J) 3/	+150°C

1.4 Recommended operating conditions.

Case operating temperature (T_C)	-55°C to +125°C
Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc

1/ Lid shall be transparent to permit ultraviolet light erasure.
2/ Must withstand the added P_D due to short circuit test, e.g., I_{OS}.
3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification For.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth tables shall be as specified on figure 2.

3.2.2.1 Unprogrammed or erased devices. The truth table for unprogrammed devices shall be as specified on figure 2.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C < T_C < +125°C$ $V_{SS} = 0$ V 4.5 V $\leq V_{CC} \leq 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input leakage current	I_{LI}	V_{IN} = 5.5 V and GND	1,2,3	All		±10	µA
Output leakage current	I_{LO}	V_{OUT} = 5.5 V and GND	1,2,3	All		±10	µA
Operating supply current (active) 1/	I_{CC1}	$\overline{CS} = V_{IL}$, V_{CC} = 5.5 V DO to D7 = 0 mA f = max	1,2,3	All		120	mA
Standby current, TTL inputs	I_{CC2}	$\overline{CS}$ = 2.0 V, V_{CC} = 5.5 V	1,2,3	All		40	mA
Standby current, CMOS inputs	I_{CC3}	V_{CC} = 5.5 V, $\overline{CS} = V_{CC}$ -0.3 V	1,2,3	All		40	mA
Input low voltage	V_{IL}	V_{CC} = 4.5 V and 5.5 V	1,2,3	All		0.8	V
Input high voltage	V_{IH}	V_{CC} = 4.5 V and 5.5 V	1,2,3	All	2.0		V
Output voltage low	V_{OL}	I_{OL} = 16 mA, V_{IH} = 2.0 V V_{CC} = 4.5 V, V_{IL} = .8 V	1,2,3	All		0.45	V
Output voltage high	V_{OH}	I_{OH} = -4 mA, V_{IH} = 2.0 V V_{CC} = 4.5 V, V_{IL} = .8 V	1,2,3	All	2.4		V
Output short circuit current 2/	I_{OS}	V_O = GND	1,2,3	All		-100	mA
Input capacitance	C_{IN}	f = 1.0 MHz, T_C = +25°C, See 4.3.1e, V_{CC} = 5.5 V, V_{IN} = 0 V	4	All		6	pF
Output capacitance	C_{OUT}	f = 1.0 MHz, T_C = +25°C, See 4.3.1e, V_{CC} = 5.5 V, V_{OUT} = 0 V	4	All		12	pF
Address to output delay	t_{ACC} 3/ 4/	$\overline{CS} = V_{IL}$	9,10,11	01,05 02,06 03 04		45 55 70 90	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V 4.5 V $\le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
$\overline{CS}$ to output delay	t_{CS} 3/ 4/		9, 10, 11	01,02		35	ns
				05		45	
				03,04, 06		55	
$\overline{CS}$ high to output float	t_{DF} 3/ 4/	$\overline{CS} = V_{IL}$	9, 10, 11	01,02		35	ns
				05		45	
				03,04, 06		55	
Address to output hold	t_{OH} 3/ 4/	$\overline{CS} = V_{IL}$	9, 10, 11	All	0		ns

1/ TTL inputs: $V_{IL} \le 0.8$ V, $V_{IH} \ge 2.0$ V.
2/ Not more than one output should be shorted at a time, and short circuit test (I_{OS}) should not exceed 30 seconds
3/ See figure 4.
4/ Output shall be loaded in accordance with figure 3.

3.5 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.5.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.5.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.

3.5.3 Verification of erasure of programmed EPROMS. When specified, devices shall be verified as either programmed to specified program or erased. As a minimum, verification shall consist of performing a funtional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method A.

(1) At +25°C, program greater than 95 percent of the bit locations, including the slowest programming cell. The remaining bits shall provide a worse case speed pattern.
(2) Bake, unbiased, for 72 hours at +140°C or for 32 hours at +150°C or for 8 hours at +200°C.
(3) At +25°C, perform a margin test using V_m = +5.8 V to loose timing (i.e., t_{ACC} = 1 µs).
(4) Perform dynamic burn-in in accordance with 4.2a.
(5) At +25°C, perform a margin test using V_m = +5.8 V.
(6) Perform electrical test in accordance with 4.2b.
(7) Erase in accordance with 3.5.1. Devices may be submitted to quality conformance inspection.
(8) Verify erasure in accordance with 3.5.3.

Margin test method B.

(1) Program at +25°C greater than 95 percent of the bit locations, including the slowest programming cell. The remaining cells shall provide a worst case speed pattern.
(2) Bake, unbiased, for 72 hours at +140°C or for 32 hours at +150°C or for 8 hours at +200°C.
(3) Perform margin test using V_m = +5.55 V and V_m = +4.40 V at +25°C using loose timing (i.e., t_{ACC} = 1 µs).
(4) Erase (see 3.5.1).
(5) Program at +25°C with a 50 percent pattern (checkerboard bar).
(6) Perform margin test using V_m = +5.75 V and V_m = +4.40 V at +25°C with loose timing.
(7) Perform dynamic burn-in for 48 hours at +150°C (see 4.2a).
(8) Perform margin test using V_m = +5.55 V and V_m = +4.40 V at +25°C using loose timing.
(9) Erase (see 3.5.1).
(10) Program at +25°C with a 50 percent pattern (checkerboard).
(11) Perform margin test using V_m = +5.75 V and V_m = +4.40 V at +25°C with loose timing.
(12) Perform dynamic burn-in for 48 hours at +150°C (see 4.2a).
(13) Perform margin test using V_m = +5.55 V and V_m = +4.40 V at +25°C using loose timing.
(14) Perform electrical tests (see 4.2b).
(15) Erase (see 3.5.1), except devices submitted for groups A, B, C, and D testing.
(16) Verify erasure (see 3.5.3).

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified except devices being submitted to group B, C, and D testing.

d. As a minimum, subgroups 7 and 8 shall consist of verifying the EPROM pattern specified.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance.

4.3.2 Groups B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883 and as follows:

a. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015 for initial testing and after any design or process changes which may affect input-output protection circuitry. The option to categorize devices as ESD sensitive without performing the test is not allowed. Device types categorized as ESD sensitive shall be further tested using method 3015 modified as follows:

Only those device types that pass ESDS testing at 1000 volts or greater shall be considered as conforming to the requirements of this drawing.

4.3.3 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

c. All devices submitted for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified.

4.4 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 angstroms (Å). The intergrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 25 Ws/cm^2. The erasure time with this dosage is approximately 35 minutes using a ultraviolet lamp with a 12,000 $\mu W/cm^2$ power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum intergrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12,000 $\mu W/cm^2$). Exposure of EPROMS to high intensity UV light for long periods may cause permanent damage.

4.5 Progamming procedure. The progamming characteristics in table III and the programming algorithm of figure 6 shall be used to program the device.

4.5.1 Programming method A. Initially and after each erasure all bits are in the "1" state. Programming is performed by raising V_{CC} to 5.6 V, disabling the outputs, addressing the byte to be programmed, presenting the data to be programmed onto the data pins, and applying a 13.5 V pulse to the $\overline{CS}/V_{PP}$ pin for 1 ms. The byte is then verified by removing the input data and reading the programmed byte as in the read operation. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device.

4.5.2 Programming method B. Two 12.5 V $\overline{CS}/V_{PP}$ pulse widths are used to program; initial and overprogram. Input addresses are set to address the desired byte. V_{CC} is raised to 6.0 V. The first $\overline{CS}/V_{PP}$ pulse is 1 ms. The programmed byte is then verified. If the byte programmed successfully, then an overprogram $\overline{CS}/V_{PP}$ pulse is applied for 3 ms. If the byte fails to program after the first 1 ms pulse, then up to 25 successive 1 ms pulses are applied with a verification after each pulse. When the byte passes verification, the overprogram pulse width is three times the number of 1 ms pulses required earlier (75 ms maximum). If the part fails to verify after 25 1 ms pulses have been applied, it is considered as failed. After the first byte is programmed, the input addresses are set to the next address repeating the alogorithm until all required addresses are programmed. Then V_{CC} is lowered to 5.0 V. All bytes subsequently are read to compare with the original data to determine if the device passes or fails.

Notes: V_{CC} must be applied simultaneously or before $\overline{CS}/V_{PP}$ and removed simultaneously or after $\overline{CS}/V_{PP}$.
When programming the 27HC641/2 a 0.1 µF capacitor is required across $\overline{CS}/V_{PP}$ and ground to supress spurious voltage transients which can damage the device.

4.5.3 Programming method C.

a. The waveforms of figure 5 and programming characteristics of table III shall apply.

b. Initially and after each erasure all bits are in the low "L" state. Information is introduced selectively programming a high "H" into the desired bit locations. A programmed "H" can be changed to an "L" by ultraviolet light erasure (see 4.4).

c. The programming mode is entered by raising pin A_{11} to V_{PP}. In this mode, pin A_{10} becomes a latch signal, allowing the upper 5 address bits to be latched and held in an onboard register, while the lower 8 address bits are presented on the same pins for selecting one of 256 memory bytes. The addressed location is programmed and verified with the application of a $\overline{PGM}$ and $\overline{VFY}$ pulse applied to pins A_9 and A_8 respectively. Entering and exiting the programming mode should be done with care.

d. Addressing during programming and blankcheck is accomplished by multiplexing the upper 5 address bits with the lower 8. The address designations for the lower 8 addressing bits is AX0 through AX7 and the upper 5 address bits are designated AY8 through AY12.

Addressing while in these modes is accomplished by placing the upper 5 bits of address on pins A_4, A_3, A_2, A_1, and A_0 with the LSB on pin A_0. These address bits are loaded into an onboard register by clocking pin A_{10}, the latch signal, from V_{ILP} to V_{IHP} and back to V_{ILP}. The lower 8 address bits are then placed on pins A_0 through A_7, with the LSB on pin A_0. The upper 5 bits remain in the onboard latch until a new value is loaded or power is removed from the device. All 256 bytes addressed by the lower 8 bits may be accessed by sequencing the lower 8 addresses without changing the upper 5 bits or relatching the value in the onboard register.

e. Blankcheck is accomplished by performing a verify cycle, sequencing through all memory address locations, where all the data read will be "0"s.

f. Programming is accomplished with an intelligent algorithm. The sequence of operations is to enter the programming mode by placing V_{PP} on pin A_9. This should be done after a minimum delay from power up, and be removed prior to power down by the same delay.

g. Address the location to be programmed and place the data to be programmed on the data pins. Clock the $\overline{PGM}$ signal from V_{IHP} to V_{ILP} and back to V_{IHP} with a pulse width of 200 µs.

h. Remove the data from the data pins, then verify the location by taking the $\overline{V_{FY}}$ signal from V_{IHP} to V_{ILP}, comparing the output with the desired data and then returning $\overline{V_{FY}}$ to V_{IHP}.

i. If the contents are correct, a second overprogram pulse of four times the original 200 µs is delivered with the data to be programmed again on the data pins.

j. If the data is not correct, a second 200 µs pulse is applied to $\overline{PGM}$ with the data on the data pins. The compare and overprogram operation is repeated with an overprogram pulse width four times the sum of the initial program pulses. This operation continues until the location is programmed or 10 initial program pulses are attempted.

k. If on the tenth attempt, the location fails to verify, an overprogram pulse of 8 ms is applied, and the content of the location is once more verified. If the location still fails to verify, the device is rejected.

l. Once a location verifies successfully, the address is advanced to the next location, and the process is repeated until all locations are programmed.

m. After all locations are programmed, they should be verified at V_{CCP} = 5.0 V.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8,9,10,11
Group A test requirements (method 5005)	1,2,3,4**,7***,8***,9,10,11
Group B end-point electrical parameters (method 5005)	1****
Groups C and D end-point electrical parameters (method 5005)	2,3,7,8

* PDA applies to subgroup 1 and 7.
** See 4.3.1e.
*** See 4.3.1d.
**** Applies to electrostatic discharge sensitivity test. See 4.3.2.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

TABLE III. Programming characteristics for method A. 1/

Parameter	Symbol	Conditions T_C = +25°C ±5°C, V_{CC} = 5.5 V ±0.5 V, V_{PP} = 13.5 V ±0.5 V	Limits		Unit
			Min	Max	
Input load current	I_{LI}	V_{IN} = V_{CC} or GND		±10	µA
V_{PP} supply current during programming pulse	I_{PP}	2/ 3/		30	mA
V_{CC} supply current	I_{CC}			60	mA
Output low voltage during verify	V_{OL}	I_{OL} = 16 mA		0.45	V
Output high voltage during verify	V_{OH}	I_{OH} = -4 mA	2.4		V
Input low voltage	V_{IL}		-0.1	0.8	V
Input high voltage	V_{IH}		2.0	V_{CC}+0.3 V	V
Address setup time	t_{AS}		2		µs
Chip disable setup time	t_{DF}			30	ns
Data setup time	t_{DS}		2		µs
Program pulse width	t_{PW}		1	10	ms
Data hold time	t_{DH}		2		µs
Chip select delay	t_{CS}			30	ns
V_{PP} rise and fall time	t_{RF}		1		ns

See footnotes at end of table.

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TABLE III. Programming characteristics for method B - Continued. 1/

Parameter	Symbol	Conditions T_C = 25°C ±5°C, V_{CC} = 6.0 V ±0.25 V, V_{PP} = 12.5 V ±0.5 V	Limits		Unit
			Min	Max	
Input load current	I_{LI}	V_{IN} = V_{CC} or GND		±10	µA
V_{PP} supply current during programming pulse	I_{PP}	2/ 3/		30	mA
V_{CC} supply current	I_{CC}	2/		80	mA
Output low voltage during verify	V_{OL}	I_{OL} = 16 mA		0.45	V
Output high voltage during verify	V_{OH}	I_{OH} = -4 mA	2.4		V
Input low voltage	V_{IL}		-0.1	0.8	V
Input high voltage	V_{IH}		2.0	V_{CC}+0.3 V	V
Address setup time	t_{AS}	4/	2		µs
Address hold time	t_{AH}	4/	2		µs
Chip disable setup time	t_{DFP}	4/ 5/	0	130	ns
Data setup time	t_{DS}	4/	2		µs
V_{CC} setup time	t_{VCS}	4/	2		µs
Program pulse width	t_{PW}	4/ 6/	0.95	1.05	ms
Overprogram pulse width	t_{OPW}	4/ 7/	2.85	78.75	ms
Data hold time	t_{DH}	4/	2		µs
$\overline{CS}/V_{PP}$ setup time	t_{CSS}	4/	2		us
Chip select delay	t_{CS}	4/		70	ns

See footnotes at end of table.

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TABLE III. Programming characteristics for method C - Continued. 1/

Parameter	Symbol	Conditions T_C = +25°C ±5°C	Limits		Unit
			Min	Max	
Programming voltage	V_{PP}	8/	12.0	13.0	V
Supply voltage	V_{CCP}		4.75	5.25	V
Input high voltage	V_{IHP}		3.0		V
Input low voltage	V_{ILP}			0.4	V
Output high voltage	V_{OH}	9/	2.4		V
Output low voltage	V_{OL}	9/		0.40	V
Programming supply current	I_{PP}			50.0	mA
Programming pulse width	t_{PP}		0.2	10	ms
Address setup time	t_{AS}		1.0		µs
Data setup time	t_{DS}		1.0		µs
Address hold time	t_{AH}		1.0		µs
Data hold time	t_{DH}		1.0		µs
V_{PP} rise and fall time	t_R, t_F	10/	1.0		µs
Delay to verify	t_{VD}		1.0		µs
Verify pulse width	t_{VP}		2.0		µs
Verify data valid	t_{DV}		1.0		µs
Verify HIGH to high-Z	t_{DZ}			1.0	µs

See footnotes at end of table.

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TABLE III. Programming characteristics for method C - Continued. 1/

Parameter	Symbol	Conditions T_C = +25°C ±5°C	Limits		Unit
			Min	Max	
Address setup time to latch	t_{ALS}		1.0		µs
Adress hold time from latch	t_{ALH}		1.0		µs
Latch pulse width	t_{LP}		1.0		µs
Delay to function	t_{DP}		1.0		µs
Hold from function	t_{HP}		1.0		µs
Power up/down	t_P		20.0		ms

1/ See figure 5 for the programming waveform.
2/ TTL inputs $V_{IL} \leq 0.8$ V, $V_{IH} > 2.0$ V.
3/ AC power component adds 3 mA/MHz.
4/ Input rise and fall times (10 percent to 90 percent): 5 ns
Input pulse levels: 0.0 V to 3.0 V
Input timing reference level: 1.5 V
Output timing reference level: 1.5 V
5/ Tested initially and after any design or process change which may affect this parameter.
6/ Initial program pulse width tolerance is 1 ms ±5 percent.
7/ The length of the overprogram pulse may vary from 2.85 ms to 78.75 ms as a function of the iteration counter value X.
8/ V_{CCP} must be applied prior to V_{PP}.
9/ During verify operation.
10/ Measured 10 percent and 90 percent points.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

	Terminal symbol	
Device	01-06	
Case	J, K, L	3
Terminal number		
1	A_7	NC
2	A_6	A_7
3	A_5	A_6
4	A_4	A_5
5	A_3	A_4
6	A_2	A_3
7	A_1	A_2
8	A_0	A_1
9	O_0	A_0
10	O_1	NC
11	O_2	O_0
12	GND	O_1
13	O_3	O_2
14	O_4	GND
15	O_5	NC
16	O_6	O_3
17	O_7	O_4
18	A_{12}	O_5
19	A_{11}	O_6
20	$\overline{CS}$	O_7
21	A_{10}	NC
22	A_9	A_{12}
23	A_8	A_{11}
24	V_{CC}	$\overline{CS}$
25	-	A_{10}
26	-	A_9
27	-	A_8
28	-	V_{CC}
29	-	

FIGURE 1. Terminal connections.

Mode	V_{CC}	$\overline{CS}/V_{PP}$	O_0-O_7
Read	5 V ±10%	V_{IL}	FF H
Output disable	5 V ±10%	V_{IH}	High Z
Program 1/	V_{CC}	V_{PP}	Data in
Verify 1/	V_{CC}	V_{IL}	Programmed byte

/1 See table III.

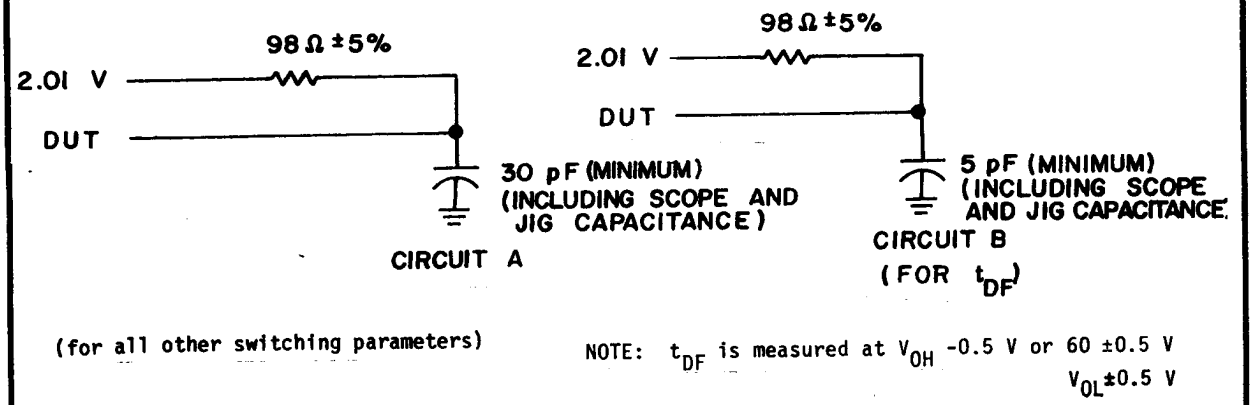
Truth table for unprogrammed devices.
Programming method A and B,
devices 01-04

Type	Mode	Outputs	A_{12}	A_{11}	$\overline{CS}$	A_{10}	A_9	A_8	V_{CC}	Power
All	Read	D_{OUT}	A_{12}	A_{11}	V_{IL}	A_{10}	A_9	A_8	V_{CC}	I_{CC}
All	Not selected	High-Z	A_{12}	A_{11}	V_{IH}	A_{10}	A_9	A_8	V_{CC}	I_{SB}
All	Program	D_{IN}	V_{ILP}**	V_{PP}**	V_{ILP}	Latch	V_{ILP}	V_{IHP}**	V_{CCP}**	I_{CC}
All	Program inhibit	High-Z	V_{ILP}	V_{PP}	V_{ILP}	Latch	V_{IHP}	V_{IHP}	V_{CC}	I_{CC}
All	Program verify	D_{OUT}	V_{ILP}	V_{PP}	V_{ILP}	Latch	V_{IHP}	V_{ILP}	V_{CC}	I_{CC}
All	Blank check	D_{OUT}	V_{ILP}	V_{PP}	V_{ILP}	Latch	V_{IHP}	V_{ILP}	V_{CC}	I_{CC}

** V_{CCP} = 5.0 V ±0.25 V; V_{PP} = 13.5 V ±0.5 V; V_{ILP} = 0.4 V max.; V_{IHP} = 3.0 V min.

Truth table for unprogrammed devices.
Programming method C,
devices 05 and 06

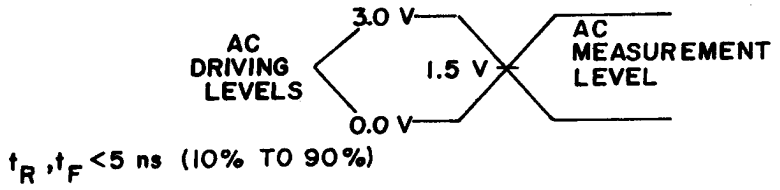
Figure 2. Truth tables.



(for all other switching parameters)

NOTE: t_{DF} is measured at V_{OH} -0.5 V or 60 ±0.5 V
V_{OL} ±0.5 V

FIGURE 3. Output load circuits or equivalent circuit.



AC TIMING INPUT LEVELS

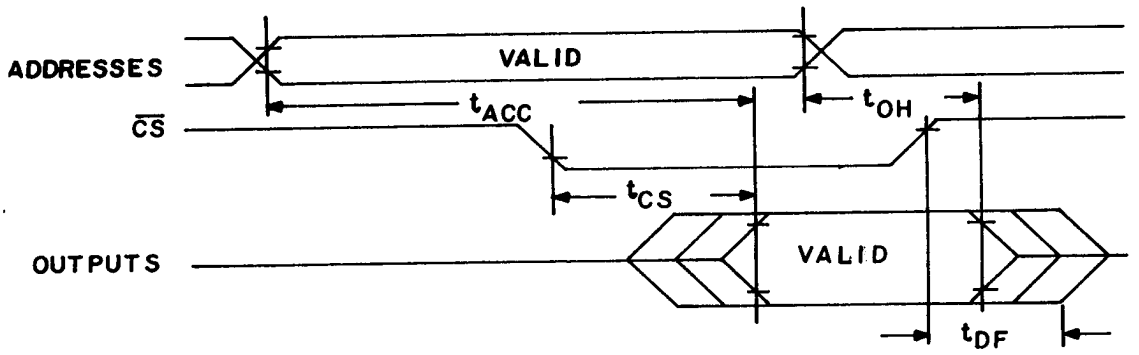
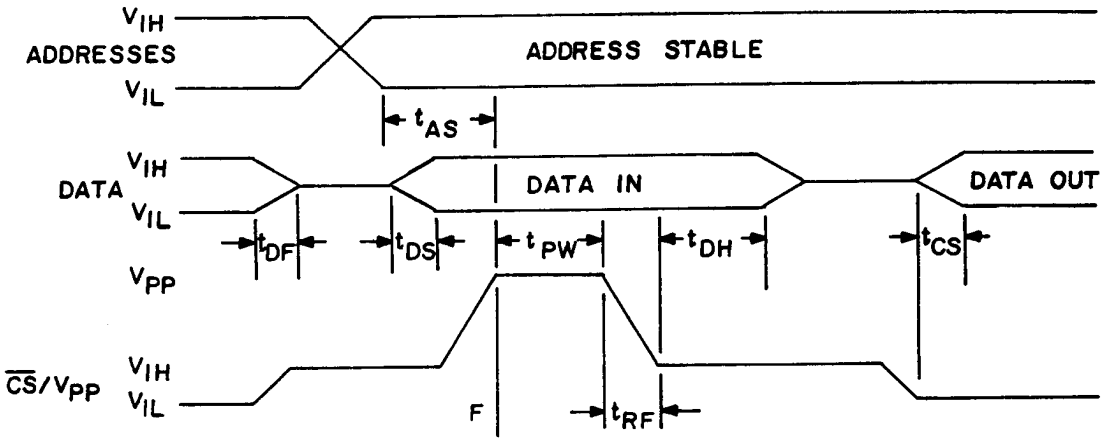
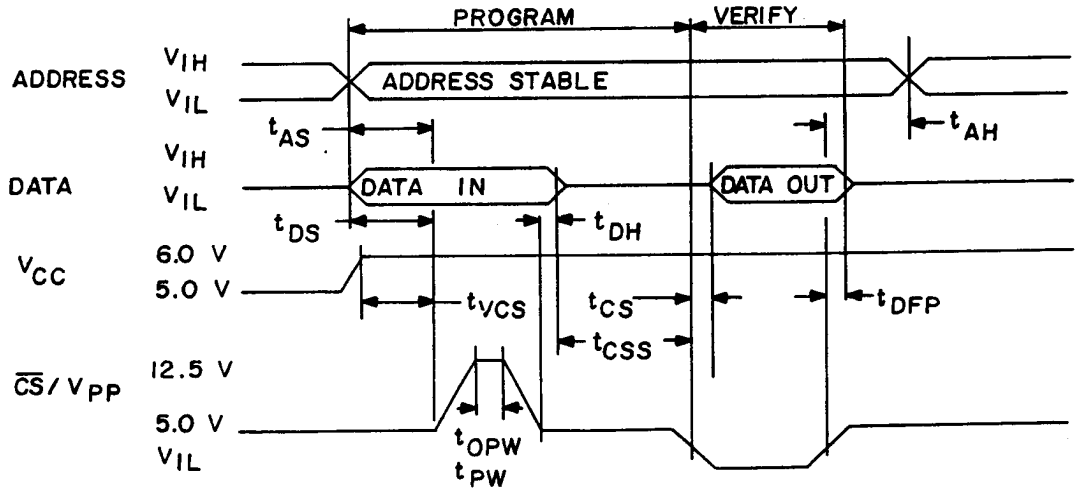


FIGURE 4. AC read timing diagram.

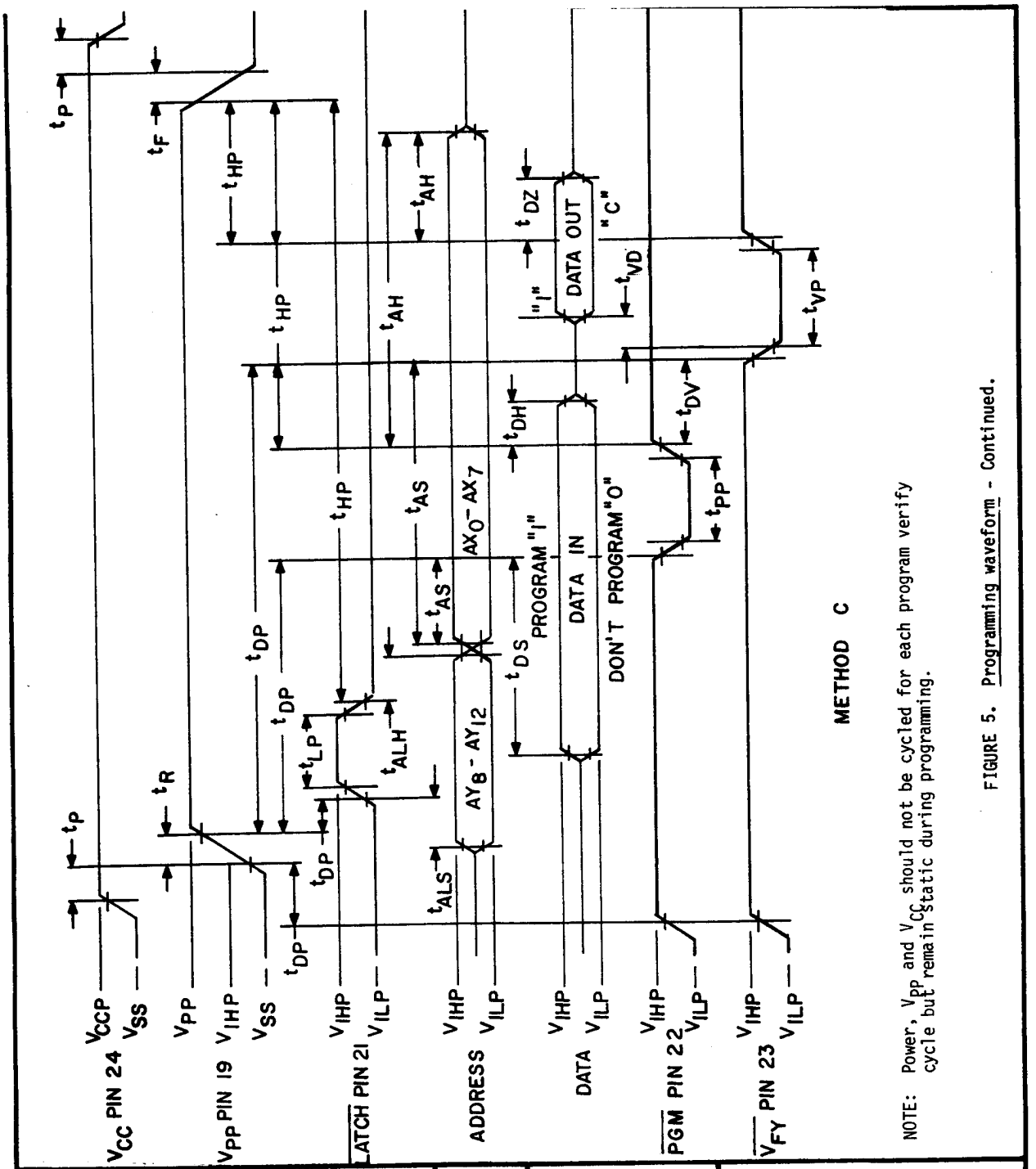


METHOD A



METHOD B

FIGURE 5. Programming waveform.



NOTE: Power, V_{PP} and V_{CC} should not be cycled for each program verify cycle but remain static during programming.

FIGURE 5. Programming waveform - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87515
		REVISION LEVEL	SHEET 18

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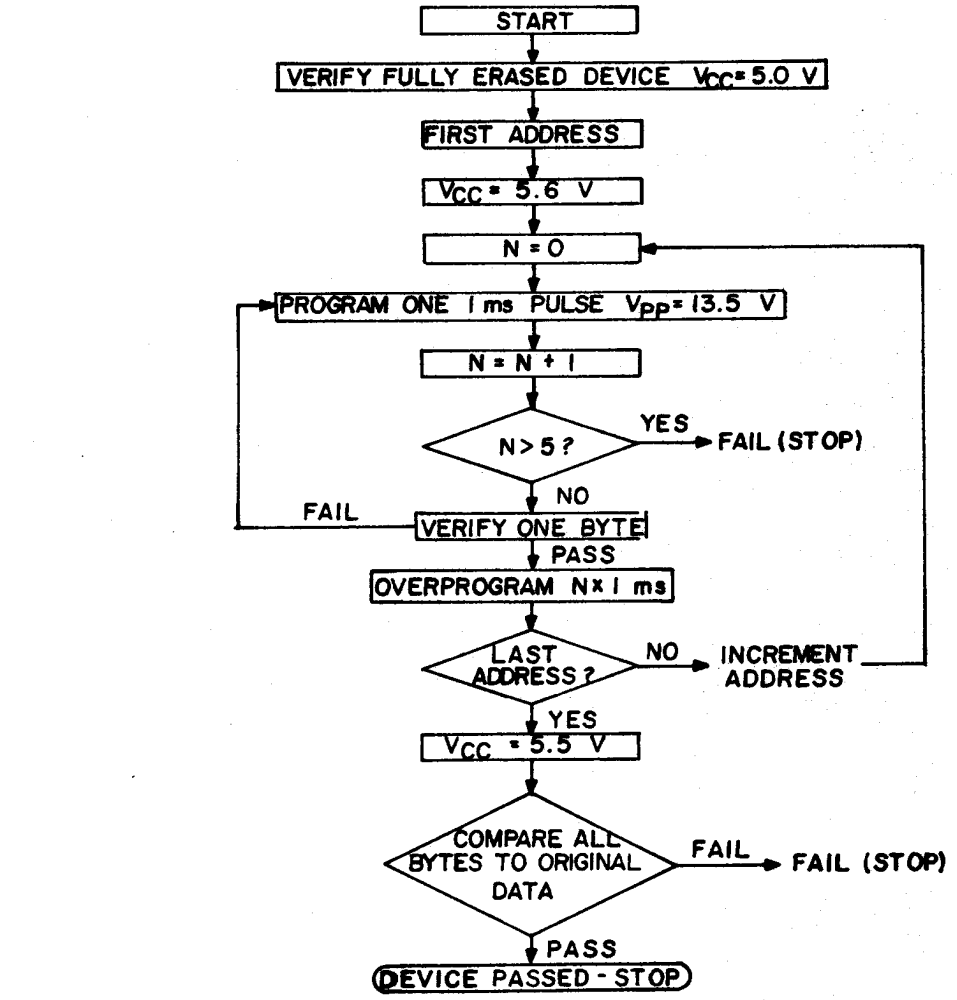

FIGURE 6. Programming algorithm method A.

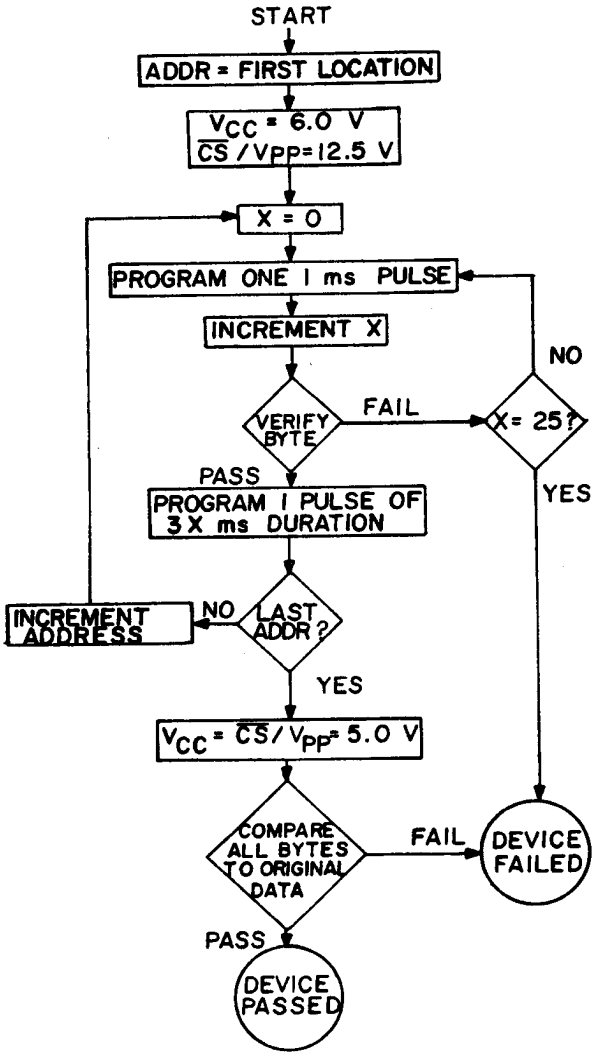

FIGURE 6. Programming algorithm method B - Continued.

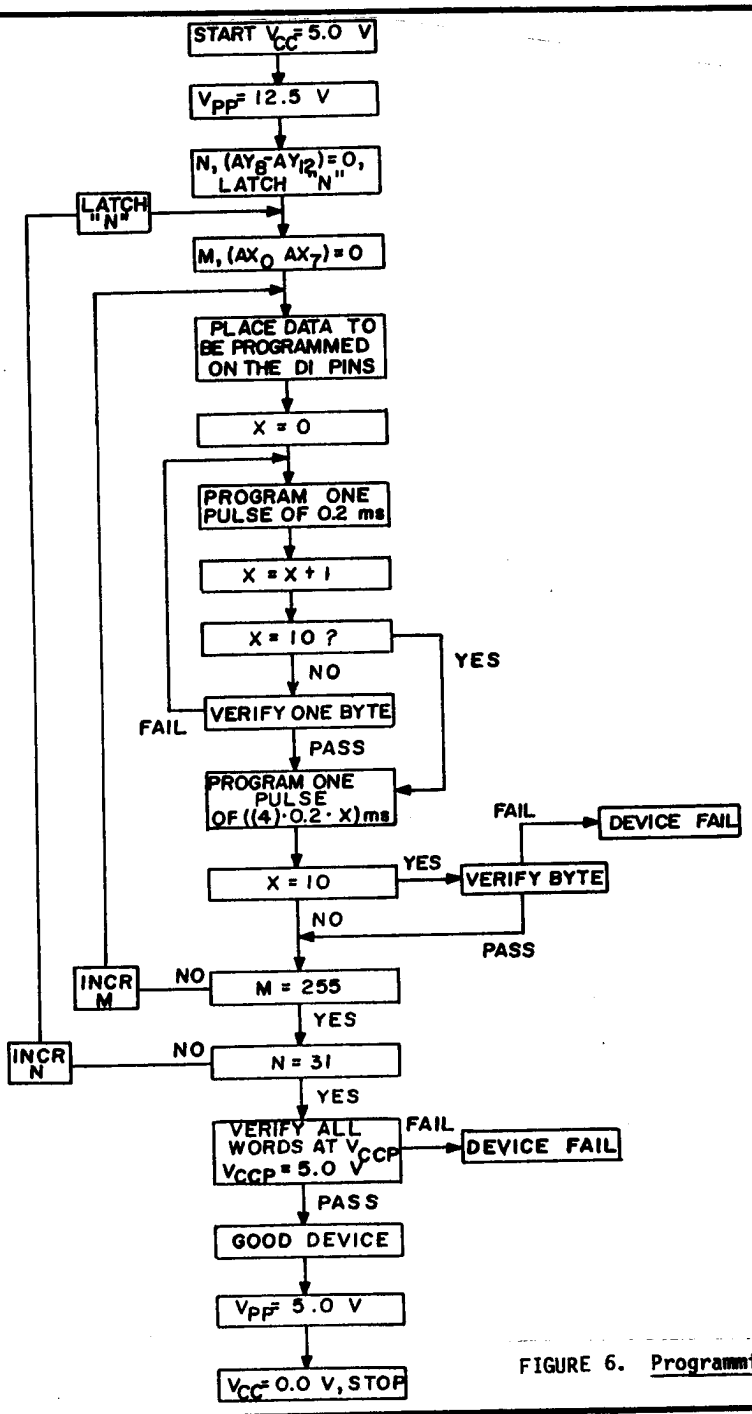

FIGURE 6. Programming algorithm method C - Continued.

6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8751501JX	66579	WS57C49B-45DMB	
	1FN41	AT27HC641-45DM/883	
5962-8751501LX	66579	WS57C49B-45TMB	
	1FN41	AT27HC642-45DM/883	
5962-87515013X	66579	WS57C49B-45CMB	
	1FN41	AT27HC641-45LM/883	
5962-8751501KX	66579	WS57C49B-45FMB	
5962-8751502JX	66579	WS57C49B-55DMB	
	1FN41	AT27HC641-55DM/883	
5962-8751502LX	66579	WS57C49B-55TMB	
	1FN41	AT27HC642-55DM/883	
5962-87515023X	66579	WS57C49B-55CMB	
	1FN41	AT27HC641-55LM/883	
5962-8751502KX	66579	WS57C49B-55FMB	
5962-8751503JX	1FN41	AT27HC641-70DM/883	
	66579	WS57C49B-70DMB	
5962-8751503LX	1FN41	AT27HC642-70DM/883	
	66579	WS57C49B-70TMB	
5962-87515033X	1FN41	AT27HC641-70LM/883	
	66579	WS57C49B-70CMB	
5962-8751503KX	66579	WS57C49B-70FMB	
5962-8751504JX	1FN41	AT27HC641-90DM/883	
	66579	WS57C49B-90DMB	
5962-8751504LX	1FN41	AT27HC642-90DM/883	
	66579	WS57C49B-90TMB	
5962-87515043X	1FN41	AT27HC641-90LM/883	
	66579	WS57C49B-90CMB	
5962-8751504KX	66579	WS57C49B-90FMB	

See footnote at end of table.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8751505LX	65786	CY7C261-45WMB	
5962-87515053X	65786	CY7C261-45QMB	
5962-8751505KX	65786	CY7C261-45TMB	
5962-8751506LX	65786	CY7C261-55WMB	
5962-87515063X	65786	CY7C261-55QMB	
5962-8751506KX	65786	CY7C261-55TMB	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address	Margin test method	Programming method
66579	WaferScale Intergration Inc. 47280 Kato Road Fremont, CA 94538	A	A
1FN41	ATMEL Corporation 2095 Ringwood Ave San Jose, CA 95131	A	B
65786	Cypress Semiconductor Corporation 3901 North First Street San Jose, CA 95134	B	C