REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27						
REV STATUS OF SHEETS				REV															
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
92-05-22

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, HMOS, REMOTE UNIVERSAL PERIPHERAL INTERFACE, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-89971
A	67268	

SHEET 1 OF 27

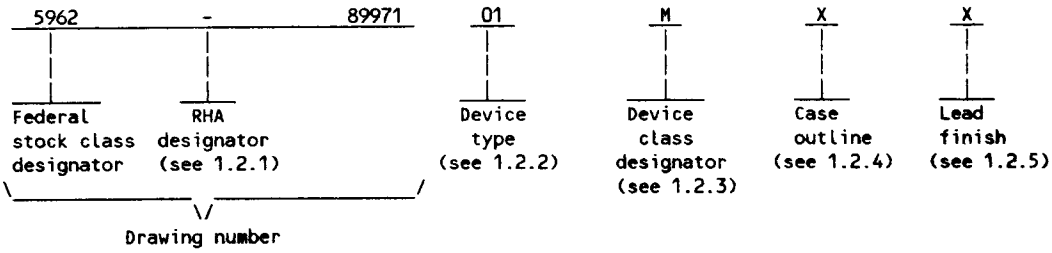
DESC FORM 193
JUL 91

5962-E367

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Frequency
01	8744H-10	Remote universal peripheral interface	10 MHz

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). For device classes M, B, and S, case outline(s) shall meet the requirements in appendix C of MIL-M-38510 and as listed below. For device classes Q and V, case outline(s) shall meet the requirements of MIL-I-38535, appendix C of MIL-M-38510, and as listed below.

Outline letter	Case outline
Q	D-5 (40-lead, 2.096" x .620" x .225") dual-in line package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Storage temperature	-65°C to +150°C
V_{CC} supply voltage with respect to ground (V_{SS})(except $\overline{EA}$)	-0.5 V to +7.0 V
Lead temperature(soldering 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-M-38510, appendix C
Junction temperature(T_J)	+150°C
Maximum power dissipation(P_D)	2.0 W
Maximum voltage V_{PP} to V_{SS}	+21.5 V

1.4 Recommended operating conditions.

Case operating temperature (T_C)	-55°C to +125°C
Supply voltage, V_{CC}	5.0 V ±10%
Minimum high level input voltage (V_{IH}):	
Logic input	2.2 V
Clock input	2.5 V
Maximum low level input voltage (V_{IL})	0.7 V
Frequency	10 MHz

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 2/

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Values will be added when they become available.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-ECC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

3.12 Processing EPROM's. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.12.1 Erasure of EPROM's. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.5.

3.12.2 Programmability of EPROM's. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.6 and table III.

3.12.3 Verification of erasure of programmability of EPROM's. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 10\%$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Output low voltage ports 1, 2, 3	V_{OL}	$V_{CC} = 4.5\ V$, $V_{IN} = V_{IH}$ min, V_{IL} max, $I_{OL} = 1.6\ mA$ 2/	1, 2, 3		0.45	V
Output low voltage ports 0, ALE, PSEN	V_{OL1}	$V_{CC} = 4.5\ V$, $V_{IN} = V_{IH}$ min, V_{IL} max, $I_{OL} = 2.4\ mA$ 2/	1, 2, 3		0.45	V
Output high voltage ports 1, 2, 3	V_{OH}	$V_{CC} = 4.5\ V$, $V_{IN} = V_{IH}$ min, V_{IL} max, $I_{OH} = -80\ \mu A$	1, 2, 3	2.4		V
Output high voltage port 0, ALE, PSEN	V_{OH1}	$V_{CC} = 4.5\ V$, $V_{IN} = V_{IH}$ min, V_{IL} max, $I_{OH} = -400\ \mu A$	1, 2, 3	2.4		V
Logical 0 input current ports 1, 2, 3	I_{IL}	$V_{IN} = 0.45\ V$ 3/	1, 2, 3		-500	µA
Input high current to RST/VPD for reset	I_{IH1}	$V_{IN} = V_{CC} - 1.5\ V$	1, 2, 3		500	µA
Input leakage current to port 0	I_{IL1}	$0.45\ V < V_{IN} < V_{CC}$	1, 2, 3		±125	µA
Logical 0 input current to EA/V_{PP}	I_{IL1}	$V_{IN} = 0.45\ V$	1, 2, 3		-15	mA
Power supply current	I_{CC}	$V_{CC} = 5.5\ V$, $V_{IN} = 5.5\ V$	1, 2, 3		300	mA
Logical 0 input current XTAL2	I_{IL2}	XTAL1 = V_{SS}, $V_{IL} = 0.45\ V$	1, 2, 3		-3.5	mA
Logical input current to EA/V_{PP}	I_{IH}		1, 2, 3		500	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0$ V ±10% unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Capacitance of I/O buffer	C_{IO}	Test frequency = 1 MHz 4/	4		10	pF
Functional test		See 4.4.1b	7, 8			
ALE pulse width	t_{LHLL}	See figure 3 5/	9, 10, 11	$2t_{CLCL}-40$		ns
Address setup to ALE	t_{AVLL}	See figure 3 5/	9, 10, 11	$t_{CLCL}-40$		ns
Address hold after ALE	t_{LLAX}	See figure 3 5/	9, 10, 11	$t_{CLCL}-35$		ns
ALE to valid Instr In	t_{LLIV}	See figure 3 5/	9, 10, 11		$4t_{CLCL}-150$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	See figure 3 5/	9, 10, 11	$t_{CLCL}-25$		ns
$\overline{PSEN}$ pulse width	t_{PLPH}	See figure 3 5/	9, 10, 11	$3t_{CLCL}-60$		ns
$\overline{PSEN}$ to valid Instr In	t_{PLIV}	See figure 3 5/	9, 10, 11		$3t_{CLCL}-150$	ns
Input Instr hold after $\overline{PSEN}$	t_{PXIX}	See figure 3 5/	9, 10, 11	0		ns
Input Instr float after $\overline{PSEN}$	t_{PXIZ}	See figure 3 3/ 5/	9, 10, 11		$t_{CLCL}-20$	ns
Address valid after $\overline{PSEN}$	t_{PXAV}	See figure 3 3/ 5/	9, 10, 11	$t_{CLCL}-8$		ns
Address to valid Instr In	t_{AVIV}	See figure 3 5/	9, 10, 11		$5t_{CLCL}-150$	ns
Address float to $\overline{PSEN}$	t_{AZPL}	See figure 3 5/	9, 10, 11	-25		ns
$\overline{RD}$ pulse width	t_{RLRH}	See figure 3 5/	9, 10, 11	$6t_{CLCL}-100$		ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 10\%$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
$\overline{WR}$ pulse width	t_{WLWH}	See figure 3 5/	9, 10, 11	$6t_{CLCL}-100$		ns
Address hold after ALE	t_{LLAX}	See figure 3 2/ 5/	9, 10, 11	$t_{CLCL}-35$		ns
$\overline{RD}$ to valid Data In	t_{RLDV}	See figure 3 5/	9, 10, 11		$5t_{CLCL}-165$	ns
Data hold after $\overline{RD}$	t_{RHDX}	See figure 3 5/	9, 10, 11	0		ns
Data float after $\overline{RD}$	t_{RHDZ}	See figure 3 2/ 5/	9, 10, 11		$2t_{CLCL}-70$	ns
ALE to valid Data In	t_{LLDV}	See figure 3 5/	9, 10, 11		$8t_{CLCL}-150$	ns
Address to valid Data In	t_{AVDV}	See figure 3 5/	9, 10, 11		$9t_{CLCL}-165$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	See figure 3 5/	9, 10, 11	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
Address to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	See figure 3 5/	9, 10, 11	$4t_{CLCL}-130$		ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	See figure 3 5/	9, 10, 11	$t_{CLCL}-50$	$t_{CLCL}+50$	ns
Data valid to $\overline{WR}$ transition	t_{DVWX}	See figure 3 5/	9, 10, 11	$t_{CLCL}-70$		ns
Data setup before $\overline{WR}$	t_{QVWH}	See figure 3 5/	9, 10, 11	$7t_{CLCL}-150$		ns
Data hold after $\overline{WR}$	t_{WHQX}	See figure 3 5/	9, 10, 11	$t_{CLCL}-50$		ns
Address float after $\overline{RD}$	t_{RLAZ}	See figure 3 2/ 5/	9, 10, 11		25	ns
Data clock	t_{DCY}	See figure 3 5/	9, 10, 11	500		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0$ V ±10% unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Data clock low	t_{DCL}	See figure 3 5/	9, 10, 11	180		ns
Data clock high	t_{DCH}	See figure 3 5/	9, 10, 11	100		ns
Transmit data delay	t_{TD}	See figure 3 5/	9, 10, 11		180	ns
Data setup time	t_{DSS}	See figure 3 5/	9, 10, 11	40		ns
Data hold time	t_{DHS}	See figure 3 5/	9, 10, 11	40		ns
Oscillator period	t_{CLCL}	See figure 3 5/	9, 10, 11	100	167	ns
High time	t_{CHCX}	See figure 3 5/	9, 10, 11	20		ns
Low time	t_{CLCX}	See figure 3 5/	9, 10, 11	20		ns
Rise time	t_{CLCH}	See figure 3 5/	9, 10, 11		20	ns
Fall time	t_{CHCL}	See figure 3 2/ 5/	9, 10, 11		20	ns

1/ All testing to be performed using worst case conditions, unless otherwise specified.

2/ V_{OL} is degraded when the device rapidly discharges external capacitance. This ac noise is most pronounced during emission of address data. When using external memory, locate the latch or buffer as close to the device as possible.

3/ Except P1.6 (pin 7), P3.0 (pin 10) and P3.1 (pin 11) which are equal to -700 µA max.

4/ See 4.4.1c.

5/ Output Load capacitance, C_L, for port 0, ALE, $\overline{PSEN}$ outputs is 100 pF. Load capacitance for all other outputs is 80 pF. $1/t_{CLCL}$ = 6 MHz to 10 MHz.

Device type	01		Device type	01	
Case outline	Q		Case outline	Q	
Terminal number	Terminal symbol	Terminal port	Terminal number	Terminal symbol	Terminal port
01	---	P 1.0	21	A8	P 2.0
02	---	P 1.1	22	A9	P 2.1
03	---	P 1.2	23	A10	P 2.2
04	---	P 1.3	24	A11	P 2.3
05	---	P 1.4	25	A12	P 2.4
06	---	P 1.5	26	A13	P 2.5
07	$\overline{RTS}$	P 1.6	27	A14	P 2.6
08	$\overline{CTS}$	P 1.7	28	A15	P 2.7
09	RST	---	29	---	$\overline{PSEN}$
10	I/$\overline{O}$/RXD	P 3.0	30	$\overline{PROG}$	ALE
11	DATA/TDX	P 3.1	31	VPP	$\overline{EA}$
12	INT0	P 3.2	32	AD7	P 0.7
13	INT1	P 3.3	33	AD6	P 0.6
14	T0	P 3.4	34	AD5	P 0.5
15	SCLK/T1	P 3.5	35	AD4	P 0.4
16	$\overline{WR}$	P 3.6	36	AD3	P 0.3
17	$\overline{RD}$	P 3.7	37	AD2	P 0.2
18	---	XTAL2	38	AD1	P 0.1
19	---	XTAL1	39	AD0	P 0.0
20	---	V_{SS}	40	---	V_{CC}

FIGURE 1. Terminal connections.

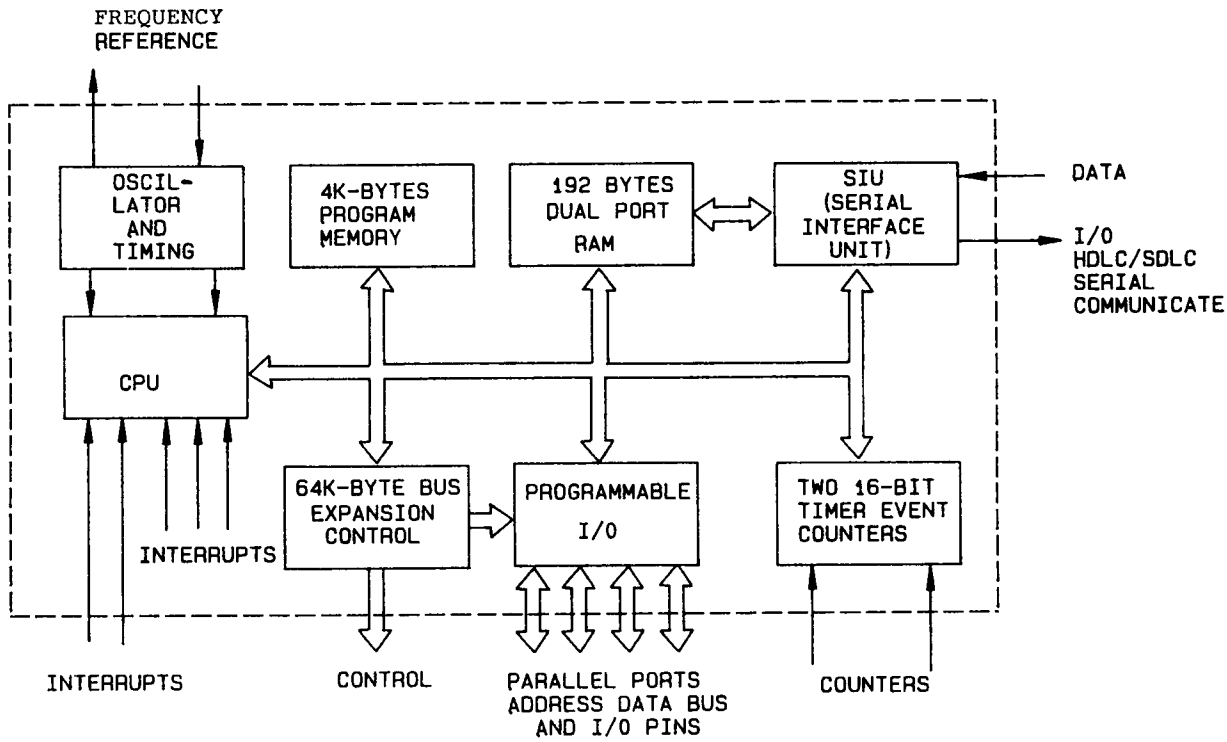
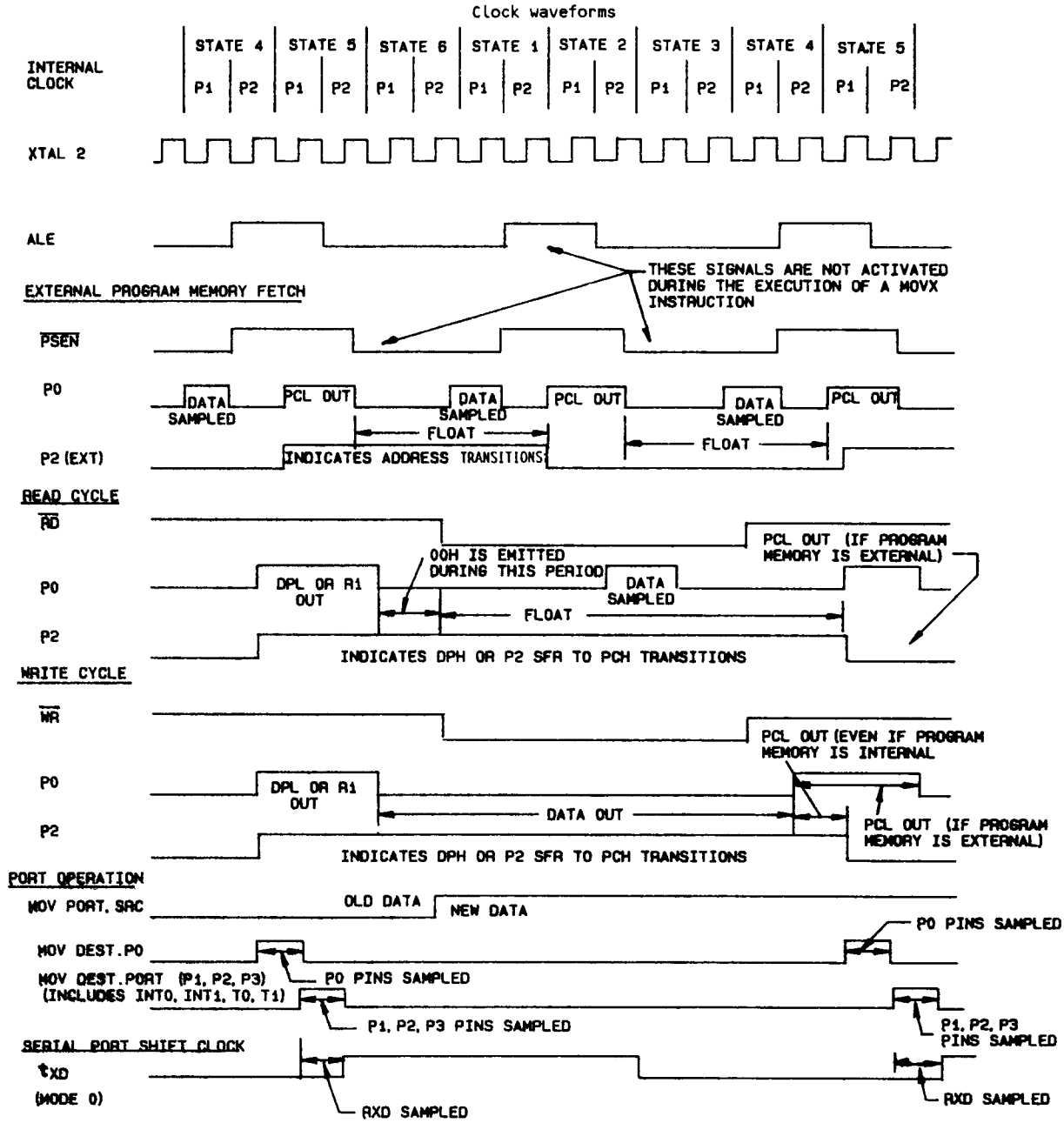


FIGURE 2. Block diagram.

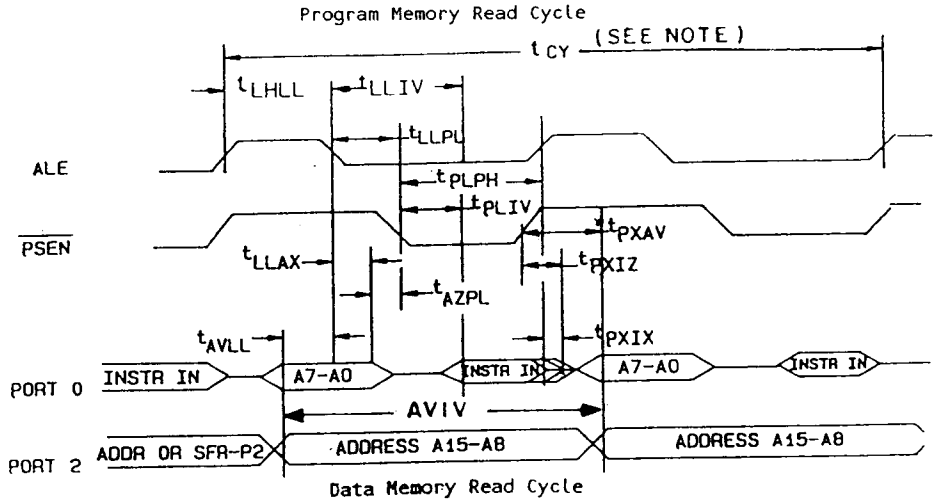


This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 50 ns to 150 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component to component. Typically though, (T_A = 25°C, fully loaded) RD and WR propagation delays are approximately 50 ns. The other signals are typically 85 ns. Propagation delays are incorporated in the ac specifications.

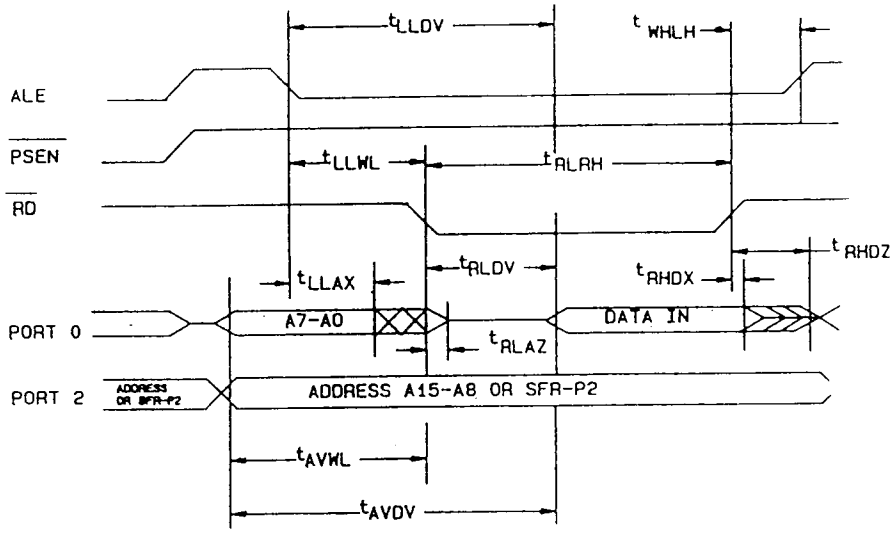
FIGURE 3. Switching test circuit and waveforms.

MEMORY ACCESS

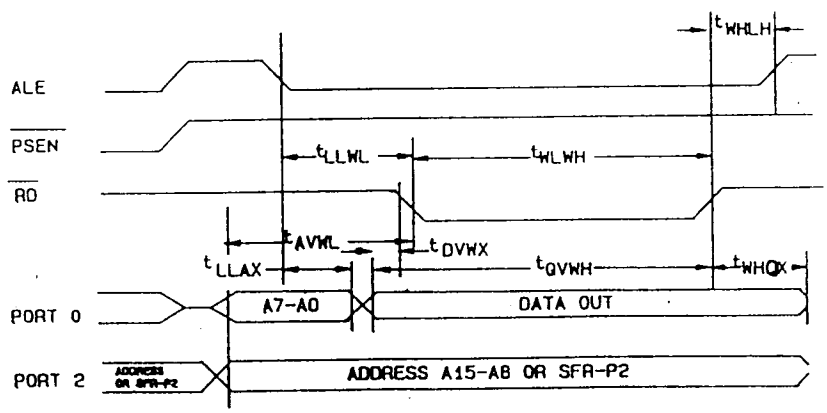
Program Memory Read Cycle



Data Memory Read Cycle



Data Memory Write Cycle

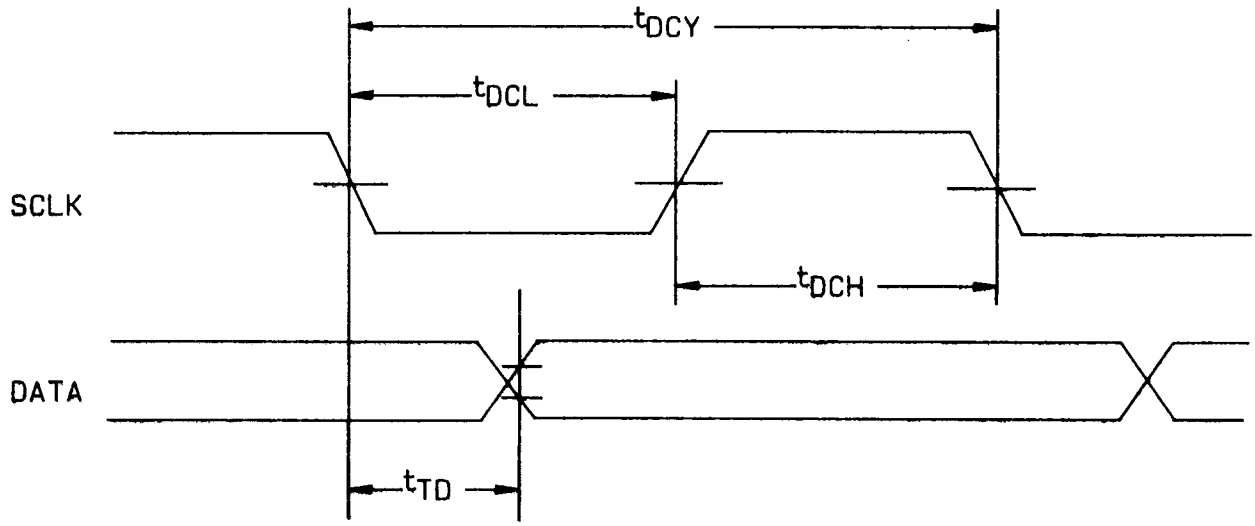


NOTE: t_{CY} = 4 Clock cycles.

FIGURE 3. Switching test circuit and waveforms - Continued.

SERIAL I/O WAVEFORMS

Synchronous Data Transmission



Synchronous Data Reception

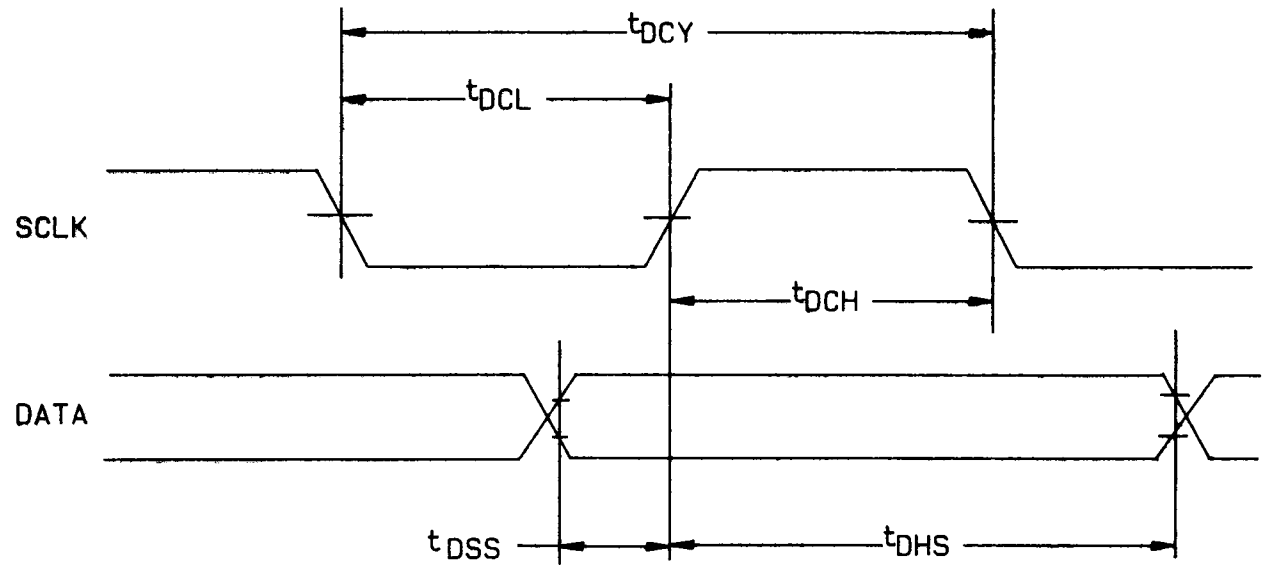
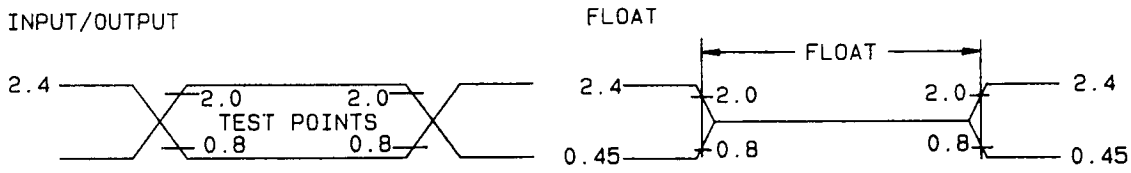


FIGURE 3. Switching test circuit and waveforms - Continued.

AC Testing Input, Output, Float Waveforms



External Clock Drive XTAL2

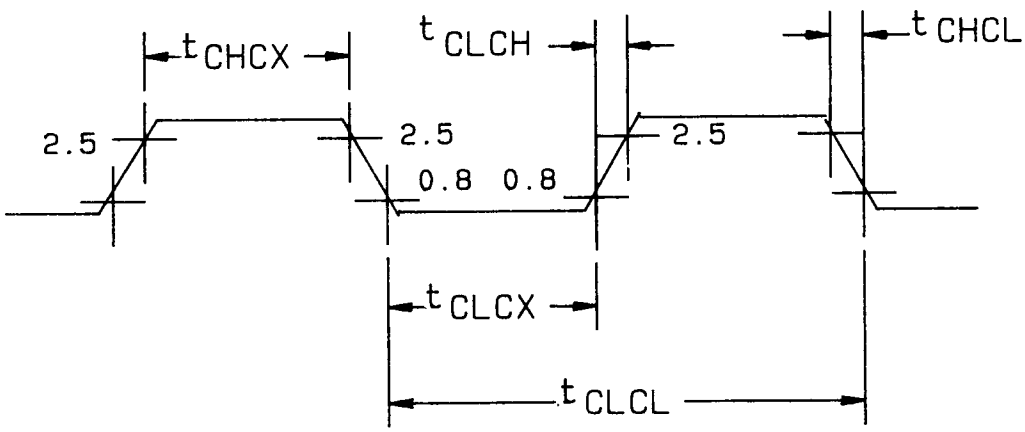
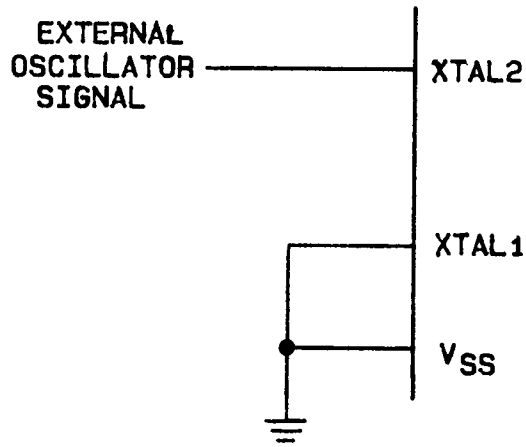


FIGURE 3. Switching test circuit and waveforms - Continued.

External Drive Configuration



Output Load Circuit

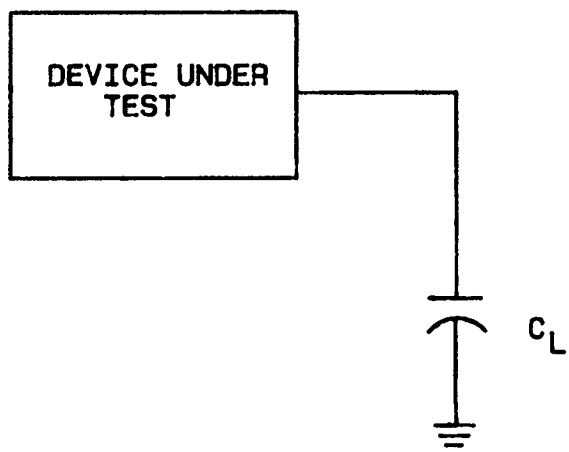


FIGURE 3. Switching test circuit and waveforms - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of following steps:

Margin test method A.

(1) Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.12.2). The remaining cells shall provide a worst case speed pattern.

(2) Bake, unbiased, for 72 hours at +140°C to screen for data retention lifetime.

(3) Perform a margin test using V_M = +5.9 V at +25°C using loose timing (i.e., t_{ACC} > 1 μs).

(4) Perform dynamic burn-in (see 4.2.1a).

(5) Margin at V_M = 5.9 V.

(6) Perform electrical tests (see 4.2).

(7) Erase (see 3.12.1), except devices submitted for groups A, B, C, and D testing.

(8) Verify erasure (see 3.12.3).

Margin test method B.

(1) Program at 25°C, 100 percent of the bits.

(2) Bake, unbiased, for 24 hours at 250°C.

(3) Perform margin test at V_M = 5.9 V.

(4) Erase (see 3.12.1).

(5) Perform interim electrical tests in accordance with table IIA.

(6) Program 100 percent of the bits and verify (see 3.12.2).

(7) Perform burn-in (see 4.2.1a).

(8) One-hundred percent test at 25°C (group A, subgroups 1 and 7). V_M = 5.9 V with loose timing, apply PDA.

(9) Perform remaining final electrical subgroups and group A testing.

(10) Erase. Devices may be submitted for groups B, C, and D at this time.

(11) Verify erasure (see 3.12.3). Steps 1 through 4 are performed at wafer level.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (per method 5005, table I)			Subgroups (per MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)			1, 7, 9		1, 7, 9
Final electrical parameters (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/	1, 2, 3, 7, 8, 9, 10, 11 2/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group B end-point electrical parameters (see 4.4)			2, 8a, 10		
Group C end-point electrical parameters (see 4.4)	2, 8a, 10	2, 8a, 10		2, 8a, 10	2, 8a, 10
Group D end-point electrical parameters (see 4.4)	2, 8a, 10	2, 8a, 10	2, 8a, 10	2, 8a, 10	2, 8a, 10
Group E end-point electrical parameters (see 4.4)	2, 8a, 10	2, 8a, 10	2, 8a, 10	2, 8a, 10	2, 8a, 10

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall consist of verifying the EPROM pattern specified and instruction set. The instruction set forms a part of the vendor's test tape and shall be maintained and available from the approved source of supply. For device classes B and S, subgroups 7 and 8 tests shall include verification of the device functionality (including verification of EPROM pattern specified and instruction set). For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4(C_{IO} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of five devices with zero rejects shall be required.

TABLE IIB. Additional screening for device class V.

Test	MIL-STD-883, test method	Lot requirement
Particle impact noise detection	2020	100%
Internal visual	2010, condition A or approved alternate	100%
Nondestructive bond pull	2023 or approved alternate	100%
Reverse bias burn-in	1015	100%
Burn-in	1015, total of 240 hours at +125°C	100%
Radiographic	2012	100%

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3.1 Additional criteria for device classes M, B, and S. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition C or D. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

d. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The steady-state life test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for device classes B and S for levels M, D, R, and H or for device class M for levels M and D shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table IIA herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table IIA herein.

d. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

f. For device classes M, B, and S, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Erasing procedure. The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-s/cm^2 rating for 20 to 30 minutes, at a distance of about 1 inch, should be sufficient.

4.6 Programming procedures. The programming characteristics in table III and the following procedures shall be used for programming the device:

a. Connect the device in the electrical configuration (see figure 4) for programming. The waveforms of figure 4 and programming characteristics of table III shall apply.

b. Initially and after each erasure, all bits are in the high "H" state. To be programmed, the device must be running with a 4 to 6 MHz oscillator. The address of an EPROM location to be programmed is applied to port 1 and pins P2.0-P2.3 of port 2, while the data byte is applied to port 0. Pins P2.4-P2.6 and PSEN should be held low, and P2.7 and RST high. (These are all TTL levels except RST, which requires 2.5 V for high). EA/V_{PP} is held normally high, and is pulsed to +21 V. While EA/V_{PP} is at 21 V, The ALE/PROG pin, which is normally being held high, is pulsed low for 50 ms. The EA/V_{PP} is returned to high.

TABLE III. Programming and verification characteristics.

Symbol	Parameter 1/	Min	Max	Units
V_{PP}	Programming supply voltage	20.5	21.5	V
I_{PP}	Programming current		30	mA
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz
t_{AVGL}	Address setup to $\overline{PROG}$	$48t_{CLCL}$		ns
t_{GHAX}	Address hold after $\overline{PROG}$	$48t_{CLCL}$		ns
t_{DVGL}	Data setup to $\overline{PROG}$	$48t_{CLCL}$		ns
t_{GHDX}	Data hold after $\overline{PROG}$	$48t_{CLCL}$		ns
t_{EHSH}	$\overline{ENABLE}$ high to V_{PP}	$48t_{CLCL}$		ns
t_{SHGL}	V_{PP} setup to $\overline{PROG}$	10		µs
t_{GHSL}	V_{PP} hold after $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ width	45	55	ms
t_{AVQV}	Address to data valid		$48t_{CLCL}$	ns
t_{ELQV}	$\overline{ENABLE}$ to data valid		$48t_{CLCL}$	ns
t_{EHQZ}	Data float after $\overline{ENABLE}$	0	$48t_{CLCL}$	ns

1/ The following conditions apply during programming and verification:

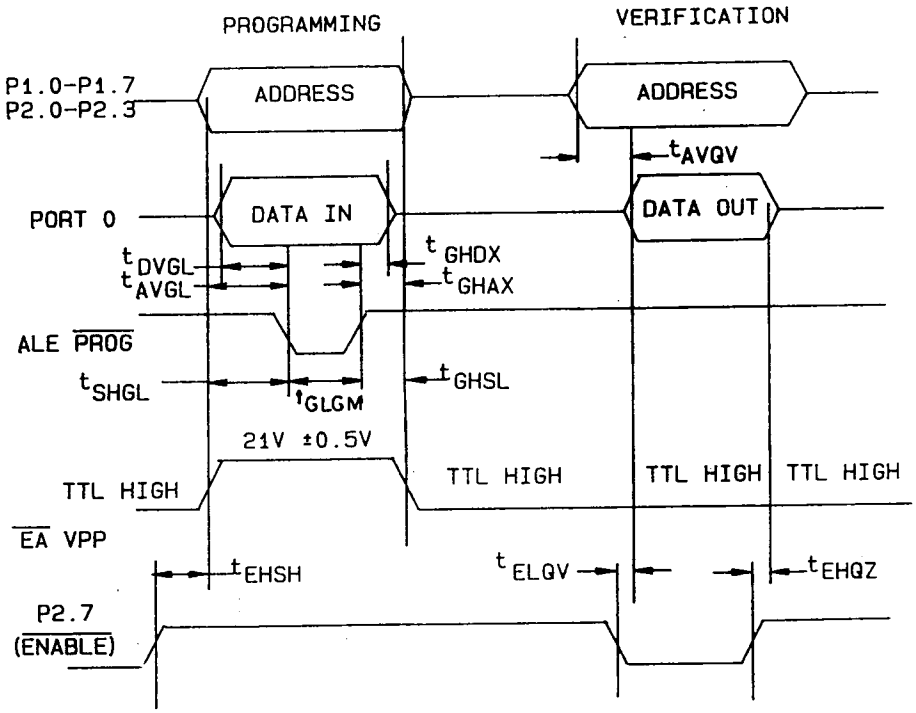
a. $V_{SS} = 0$ V

b. $+4.5\ V \le V_{CC} \le +5.5\ V$

c. $21°C \le T_C \le 27°C$

d. See figure 4

EPROM Programming
Security Bit Programming and Verification Waveforms



Security Bit Programming Configuration

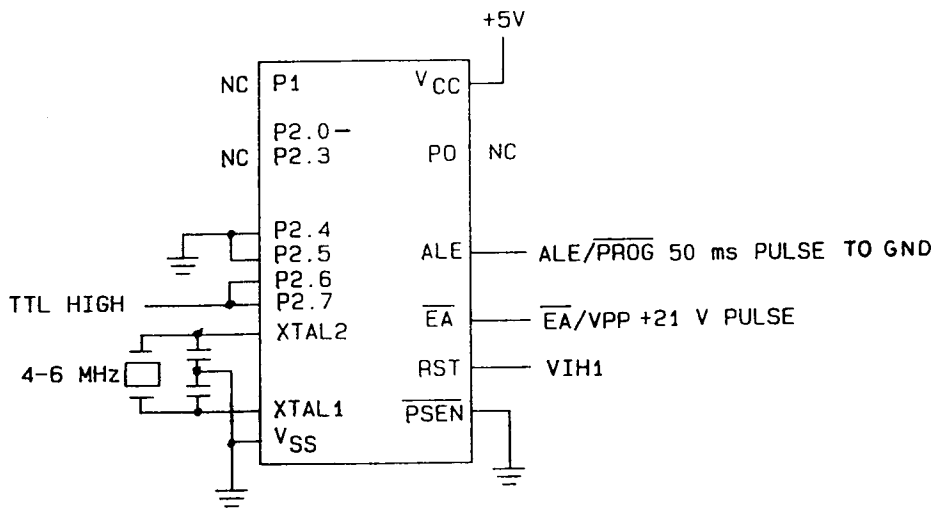
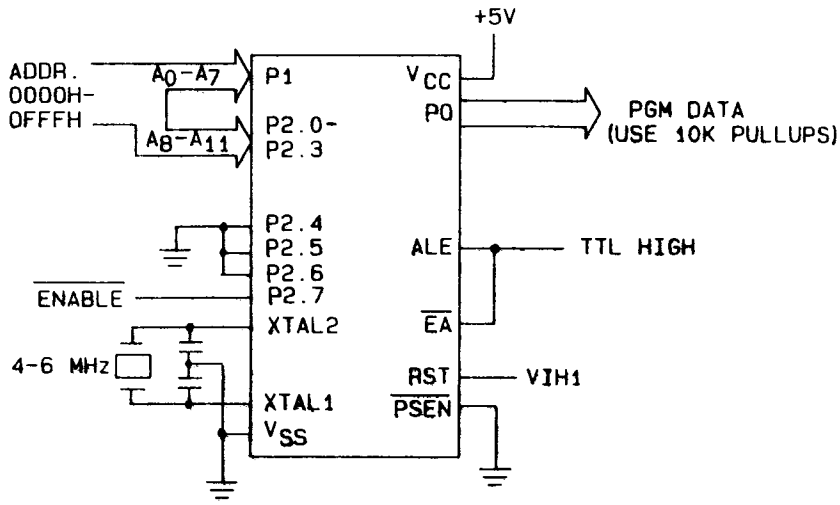


FIGURE 4. EPROM programming configuration and waveforms.

Programming Verification Configuration



Programming Configuration

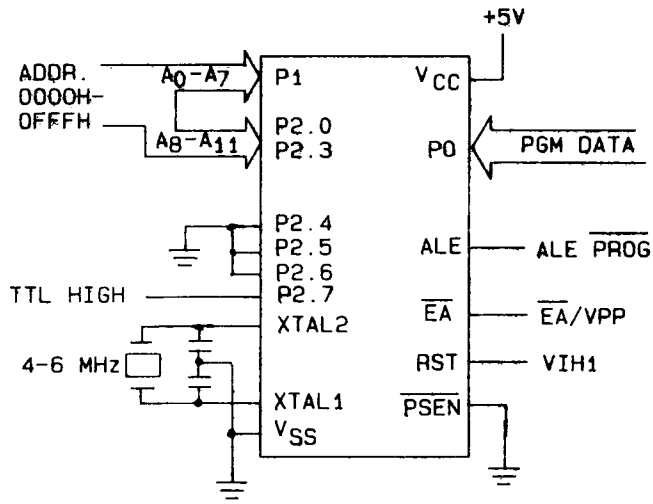


FIGURE 4. EPROM programming configuration and waveforms - Continued.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-6022.

6.4 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8526.

6.5 Symbols, definitions, and functional descriptions.

Symbol	Type	Name and Description
AD0-AD7	I/O	Port 0 (P0.0-P0.7): Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplex low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source six LS TTL loads.
	I/O	Port 1 (P1.0-P1.7): Port 1 is an 8-bit quasi-bidirectional I/O. It is used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads.
$\overline{\text{RTS}}$ (P1.6)	O	Request-to-Send output: A low indicates that the device is ready to transmit.
$\overline{\text{CTS}}$ (P1.7)	I	Clear-to-Send input: A low indicates that a receiving station is ready to receive.

Symbol	Type	Name and Description
A8-A15	I/O	Port 2 (P2.0-P2.7): Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 sink/source four LS TTL loads.
	I/O	Port 3 (P3.0-P3.7): Port 3 is an 8-bit quasibidirectional I/O port. It also contains the interrupt, timer, serial port, and RD and WR pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS TTL loads.
I/$\overline{O}$ RxD (P3.0)	I	In point-to-point or multipoint configurations, this pin controls the direction of pin P3.1. Serves as Receive Data input in loop and diagnostic modes.
DATA TxD (P3.1)	O	In point-to-point or multipoint configurations, this pin functions as data input/output. In loop mode, it serves as transmit pin. A "0" written to this pin enables diagnostic mode.
$\overline{INT0}$ (P3.2)	I	Interrupt 0 input or gate control input for counter 0.
$\overline{INT1}$ (P3.3)	I	Interrupt 1 input or gate control input for counter 0.
T0 (P3.4)	I	Input to counter 0.
SCLK T1 (P3.5)	I	In addition to I/O, this pin provides input to counter 1 or serves as SCLK (serial clock) input.
$\overline{WR}$ (P3.6)	O	WRITE: The write control signal latches the data byte from port 0 into the external data memory.
$\overline{RD}$ (P3.7)	O	READ: The read control signal enables external data memory to port 0.
RST	I	A high on this pin for two machine cycles while the oscillator is running resets the device. A small external pull-down resistor ($\approx$ 8.2 kΩ) from RST to V_{SS} permits power-on reset when capacitor ($\approx$ 10 μF) is also connected from this pin to V_{CC}.
ALE/$\overline{PROG}$	O	Provides Address Latch Enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access. It also receives the program pulse input for programming the device.

Symbol	Type	Name and Description
$\overline{PSEN}$	O	The program Store Enable output is a control signal that enables the external Program Memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.
$\overline{EA}/V_{PP}$	I	When held at a TTL high level, the device executes instructions from the internal ROM when the PC is less than 4096. When held at a TTL low level, the device fetches all instructions from external Program Memory. The pin also receives the 21 V EPROM programming supply voltage on the device.
XTAL1	I	Input to the oscillator's high gain amplifier. Required when a crystal is used. Connected to V_{SS} when external source is used on XTAL2.
XTAL2	O	Output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-89971ZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-89971ZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-89971ZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-89971ZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-ECC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.