PRELIMINARY

AmC001AFLKA

1 Megabyte Flash Memory PC Card

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 250 ns maximum access time
- **CMOS low power consumption**
  - 25 mA typical active current (X8)
  - 400 μA typical standby current
- **PCMCIA/JEIDA 68-pin standard**
  - Selectable byte or word-wide configuration
- **Write protect switch**
  - Prevents accidental data loss
- **High re-programmable endurance**
  - Minimum 100,000 erase/write cycles
- **Zero data retention power**
  - Batteries not required for data storage
- **Separate attribute memory**
  - 512 byte EEPROM
- **Automated write and erase operations (increases system write performance)**
  - 128K byte memory segment
  - Typically <1 second per single memory segment erase
  - Random address writes to previously erased bytes (10 μs typical per byte)
- **Total system integration solution**
  - Support from independent software and hardware vendors
- **Insertion and removal force**
  - State of art connector allows for minimum card insertion and removal effort
- **Write and erase voltage, 12.0 V ± 5%**
- **Read voltage, 5 V ± 5%**
- **Manufactured by DuPont Connector Systems**

GENERAL DESCRIPTION

AMD's Flash Memory PC Card provides the highest system level performance for data and file storage solutions to the portable PC market segment. Data files and application programs can be stored on the AmC001AFLKA. This allows OEM manufacturers of portable system to eliminate the weight, extreme power consumption and reliability issues associated with electro-mechanical disk-based systems. The AmC001AFLKA also allows today's bulky and heavy battery packs to be reduced in weight and size. Typically only two "AA" alkaline batteries are required for total system operation. AMD's Flash Memory PC Cards provide the most efficient method to transfer useful work between different hardware platforms. The enabling technology of the AmC001AFLKA enhances the productivity of mobile workers.

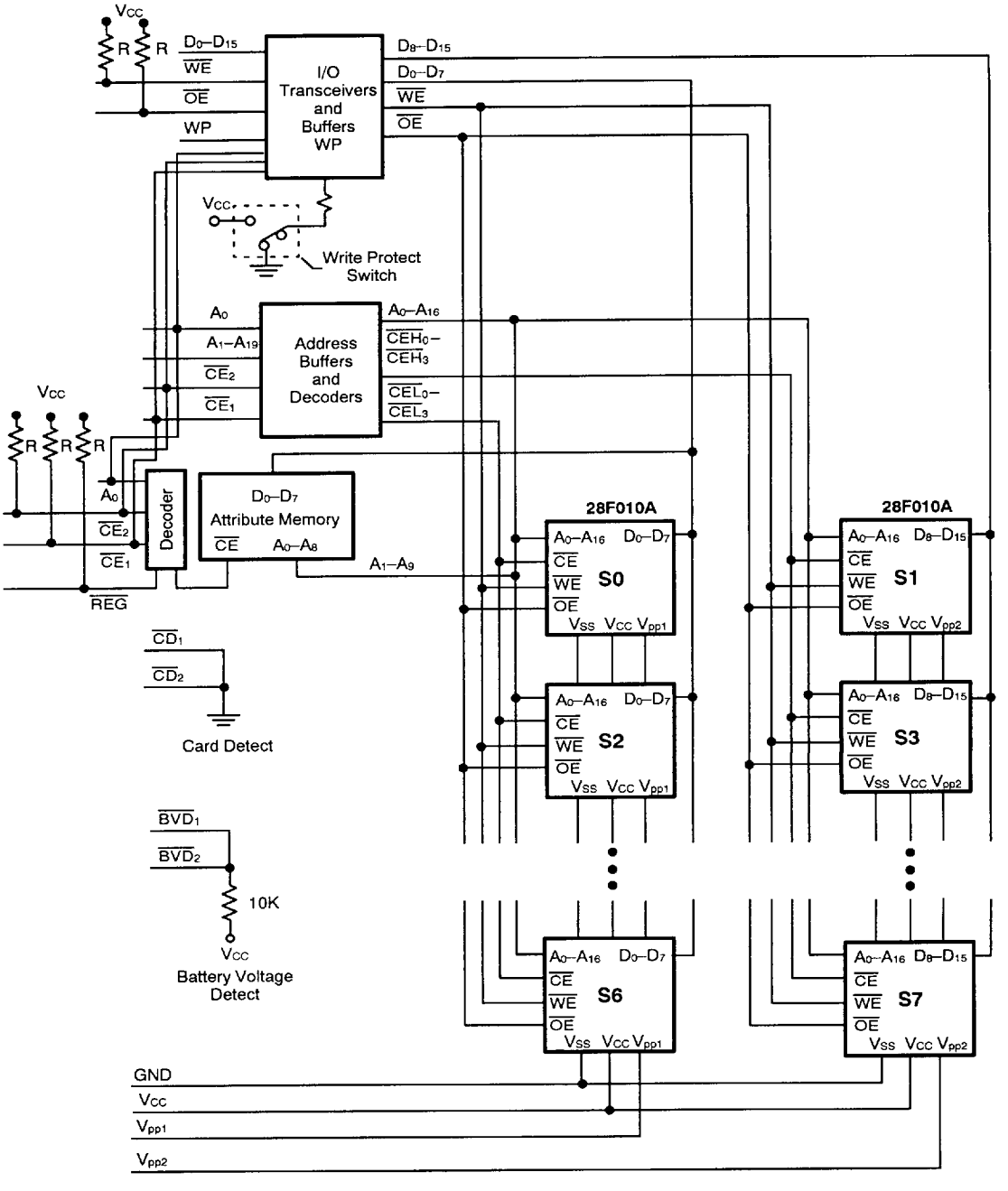
Widespread acceptance of the AmC001AFLKA is assured due to its compatibility with the 68-pin PCMCIA/JEIDA international standard. AMD's Flash Memory Cards can be read in either a byte-wide or word-wide mode which allows for flexible integration into various system platforms. Compatibility is assured at the hardware interface and software interchange specification. The Card Information Structure (CIS) or Metaformat, can be written by the OEM at the Memory Card's attribute memory address space beginning at address 00000H by using a format utility. The CIS appears at the beginning of the Card's attribute memory space and defines the low-level organization of data on the PC Card. The AmC001AFLKA contains a separate 512 byte EEPROM memory for the card's attribute memory space. This allows all of the Flash Memory to be used for the common memory space.

Third party software solutions such as Microsoft's Flash File System (FFS), enable AMD's Flash Memory PC Card to replicate the function of traditional disk-based memory systems.

Manufactured by DuPont Connector Systems

Publication# 17120 Rev. A Amendment/0
Issue Date: September 1992

BLOCK DIAGRAM



PC CARD PIN ASSIGNMENTS

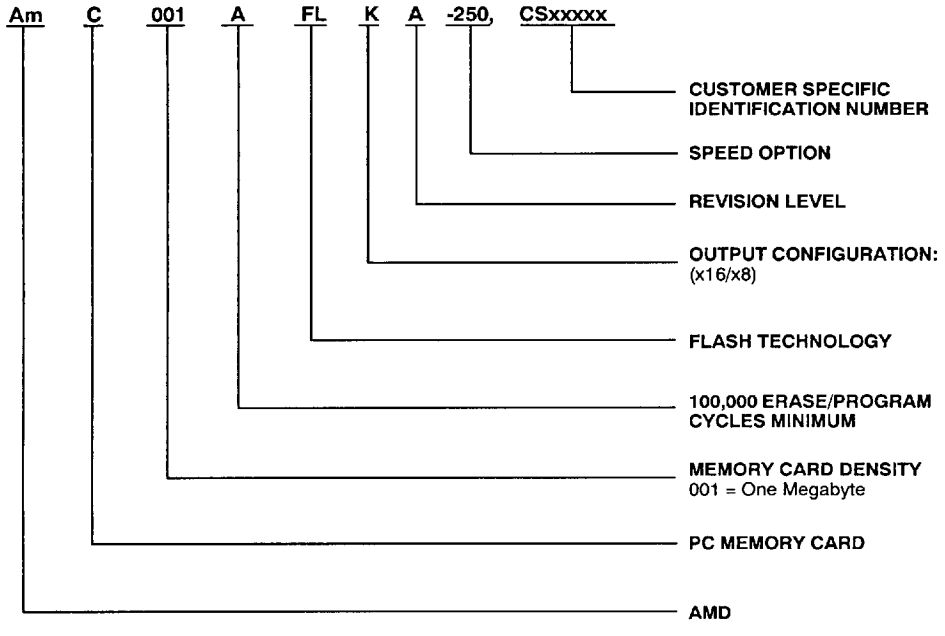
Pin#	Signal	I/O	Function	Pin#	Signal	I/O	Function
1	GND		Ground	35	GND		Ground
2	D_3	I/O	Data Bit 3	36	$\overline{CD_1}$	O	Card Detect (Note 1)
3	D_4	I/O	Data Bit 4	37	D_{11}	I/O	Data Bit 11
4	D_5	I/O	Data Bit 5	38	D_{12}	I/O	Data Bit 12
5	D_6	I/O	Data Bit 6	39	D_{13}	I/O	Data Bit 13
6	D_7	I/O	Data Bit 7	40	D_{14}	I/O	Data Bit 14
7	$\overline{CE_1}$	I	Card Enable (Note 1)	41	D_{15}	I/O	Data Bit 15
8	A_{10}	I	Address Bit 10	42	$\overline{CE_2}$	I	Card Enable 2 (Note 1)
9	$\overline{OE}$	I	Output Enable	43	NC		No Connect
10	A_{11}	I	Address Bit 11	44	RFU		Reserved
11	A_9	I	Address Bit 9	45	RFU		Reserved
12	A_8	I	Address Bit 8	46	A_{17}	I	Address Bit 17
13	A_{13}	I	Address Bit 13	47	A_{18}	I	Address Bit 18
14	A_{14}	I	Address Bit 14	48	A_{19}	I	Address Bit 19
15	$\overline{WE}$	I	Write Enable	49	NC		No Connect
16	NC		No Connect	50	NC		No Connect
17	V_{CC}		Power Supply	51	V_{CC}		Power Supply
18	V_{pp1}		Pgm Sply Vltg 1	52	V_{pp2}		Pgm Sply Vltg 2
19	A_{16}	I	Address Bit 16	53	NC		No Connect
20	A_{15}	I	Address Bit 15	54	NC		No Connect
21	A_{12}	I	Address Bit 12	55	NC		No Connect
22	A_7	I	Address Bit 7	56	NC		No Connect
23	A_6	I	Address Bit 6	57	NC		No Connect
24	A_5	I	Address Bit 5	58	NC		No Connect
25	A_4	I	Address Bit 4	59	NC		No Connect
26	A_3	I	Address Bit 3	60	NC		No Connect
27	A_2	I	Address Bit 2	61	$\overline{REG}$	I	Register Select
28	A_1	I	Address Bit 1	62	$\overline{BVD_2}$	O	Battery Vltg Detect 2 (Note 2)
29	A_0	I	Address Bit 0	63	$\overline{BVD_1}$	O	Battery Vltg Detect 1 (Note 2)
30	D_0	I/O	Data Bit 0	64	D_8	I/O	Data Bit 8
31	D_1	I/O	Data Bit 1	65	D_9	I/O	Data Bit 9
32	D_2	I/O	Data Bit 2	66	D_{10}	I/O	Data Bit 10
33	WP	O	Write Protect (Note 1)	67	$\overline{CD_2}$	O	Card Detect
34	GND		Ground	68	GND		Ground

Notes:

I = Input to card, O = Output from card
I/O = Bi-directional
NC = No connect
In systems which switch Vcc individually to cards, no signal should be directly connected between cards other than ground.
1. Signal must not be connected between cards
2. $\overline{BVD}$ = Internally pulled-up

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



PIN DESCRIPTION

Symbol	Type	Name and Function
$A_0 - A_{19}$	INPUT	**ADDRESS INPUTS** are internally latched during write cycles.
$D_0 - D_{15}$	INPUT/ OUTPUT	**DATA INPUT/OUTPUT:** Data inputs are internally latched on write cycles. Data outputs during read cycles. Data pins are active high. When the memory card is de-selected or the outputs are disabled the outputs float to tri-state.
$\overline{CE}_1$, $\overline{CE}_2$	INPUT	**CARD ENABLE** is active low. The memory card is de-selected and power consumption is reduced to stand-by levels when $\overline{CE}$ is high. $\overline{CE}$ activates the internal memory card circuitry that controls the high and low byte control logic of the card, input buffers segment decoders, and associated memory devices.
$\overline{OE}$	INPUT	**OUTPUT ENABLE** is active low and enables the data buffers through the card outputs during read cycles.
$\overline{WE}$	INPUT	**WRITE ENABLE** is active low and controls the write function of the command register to the memory array. The target address is latched on the falling edge of the $\overline{WE}$ pulse and the appropriate data is latched on the rising edge of the pulse.
V_{PP1},V_{PP2}		**ERASE/WRITE POWER SUPPLY** for erase and programming. V_{pp} enables the command register which controls all functions required to alter the memory array contents. **Note:** The Memory Card functions in a read-only memory when $V_{PP} < V_{cc} + 2$ V.
V_{CC}		**PC CARD POWER SUPPLY** for device operation (5.0 V ± 5%)
GND		**GROUND**
CD_1, CD_2	OUTPUT	**CARD DETECT.** When card detect 1 and 2 = ground the system detects the card.
WP	OUTPUT	**WRITE PROTECT** is active high and disables all card write operations.
NC		**NO CONNECT** - corresponding pin is not connected internally to the die.
BVD_1, BVD_2	OUTPUT	**BATTERY VOLTAGE DETECT.** Internally pulled-up.

MEMORY CARD OPERATIONS

The AmC001AFLKA Flash Memory Card is organized as an array of individual devices. Each device is 128K bytes in size. Although the address space is continuous each physical device defines a logical address segment size. Erase operations are performed in increments of this segment size. Multiple segments may be erased concurrently when additional V_{pp} current is supplied to the device. Once a memory segment is erased any address location may be programmed. Flash technology allows any logical "1" data bit to be programmed to a logical "0". The only way to reset bits to a logical "1" is to erase the entire memory segment of 128K bytes. High voltage is required on V_{pp1} and V_{pp2} to perform program and erase operations.

The common memory space data contents are altered in a similar manner as writing to individual Flash Memory devices. On-card address and data buffers activate the appropriate Flash device in the memory array. Each device internally latches address and data during write cycles. Refer to Table 2A.

Attribute memory is a separately accessed card memory space. The register memory space is active when the $\overline{REG}$ pin is driven low. The Card Information Structure describes the capabilities and specification of a card. The CIS is stored in the attribute memory space beginning at address 00000H. The AmC001AFLKA contains a separate 512 byte EEPROM memory for the Card Information Structure. Alternatively, the CIS can be stored at the beginning of the common memory address space. D_0–D_7 are active during attribute memory accesses. D_8–D_{15} should be ignored. Odd order bytes present invalid data. Refer to Table 2B.

Word-Wide Operations

The AmC001AFLKA provides the flexibility to operate on data in a byte-wide or word-wide format. In word-wide operations the Low-bytes are controlled with V_{pp1} and $\overline{CE}_1$ when A0 = 0. The High-bytes are controlled with V_{pp2} and $\overline{CE}_2$, A0 = don't care.

Erase operations are the only operations that work on entire memory segments. All other operations such as word-wide programming are not affected by the physical memory segments.

Byte-Wide Operations

Byte-wide data is available on D_0–D_7 for read and write operations ($\overline{CE}_1$ = low, $\overline{CE}_2$ = high). Even and odd bytes are stored in separate memory segments (i.e. S_0 and S_1) and are accessed when A0 is low and high respectively. The even byte is the low order byte and the odd byte is the high order byte of a 16-bit word.

Erase operations in the byte-wide mode must account for data multiplexing on D_0–D_7 by changing the state of A0. Each memory segment pair must be addressed separately for erase operations.

Card Detection

Each $\overline{CD}$ (output) pin should be read by the host system to determine if the memory card is adequately seated in the socket. $\overline{CD}_1$ and $\overline{CD}_2$ are internally tied to ground. If both bits are not detected, the system should indicate that the card must be re-inserted.

Write Protection

The AMD Flash memory card has three types of write protection. The PCMCIA/JEIDA socket itself provides the first type of write protection. Power supply and control pins have specific pin lengths in order to protect the card with proper power supply sequencing in the case of hot insertion and removal.

A mechanical write protect switch provides a second type of write protection. When this switch is activated, $\overline{WE}$ is internally forced high. The Flash memory command register is disabled from accepting any write commands.

The third type of write protection is achieved with V_{pp1} and V_{pp2} at logic low levels to reset the Flash devices to read-only mode. Memory contents can not be changed in this state. The command register of individual Flash memory segments is only active when V_{pp1} and/or V_{pp2} are at high voltage (V_{ppH}).

Each Flash memory device that comprises a Flash memory segment will reset the command register to the read-only mode when V_{cc} is below VLKO. VLKO is the voltage below which write operations to individual command registers are disabled.

MEMORY CARD BUS OPERATIONS

Read Enable

Two Card Enable ($\overline{CE}$) pins are available on the memory card. Both $\overline{CE}$ pins must be active low for word-wide read accesses. Only one $\overline{CE}$ is required for byte-wide accesses. The $\overline{CE}$ pins control the selection and gates power to the high and low memory segments. The Output Enable ($\overline{OE}$) controls gating accessed data from the memory segment outputs.

Output Disable

Data outputs from the card are disabled when $\overline{OE}$ is at a logic-high level. Under this condition, outputs are in the high-impedance state.

Standby Operations

Byte-wide read accesses only require half of the read/write output buffer (x16) to be active. In addition, only one memory segment is active with in either the high order or low order bank. Activation of the appropriate half of the output buffer is controlled by the combination of both $\overline{CE}$ pins. The $\overline{CE}$ pins also control power to the high and low-order banks of memory. Outputs of the memory bank not selected are placed in the high impedance state. The individual memory segment is activated by the address decoders. The other memory segments operate in standby. An active memory segment continues to draw power until completion of a write, erase, or verify operation if the card is de-selected in the process of one of these operations.

Auto Select Operation

A host system or external card reader/writer can determine the on-card manufacturer and device I.D. codes. Codes are available after writing the 90H command to the command register of a memory segment. Reading from address location 00000H in any segment provides the manufacturer I.D. while address location 00002H provides the device I.D.

Write Operations

Write and erase operations are valid only when V_{pp1} and V_{pp2} are at high voltage. This activates the state machine of an addressed memory segment. The command register is a latch which saves address, commands, and data information used by the state machine and memory array.

When Write Enable ($\overline{WE}$) and appropriate $\overline{CE}$(s) are a logic-level low, the command register is enabled for write operations. The falling edge of $\overline{WE}$ latches address information and the rising edge latches data/command information.

Memory Segment Command Definitions

When the V_{pp} pin(s) are at low voltage the command register of each Flash memory segment defaults to 00H, the Read only mode.

With high voltage on the V_{pp} pin(s), the Flash memory segments are active for either read, write, or erase operations.

Write or erase operations are performed by writing appropriate data patterns to the command register of accessed Flash memory segments.

The byte-wide and word-wide commands are defined in Tables 3 and 4 respectively.

Table 2A. Common Memory Bus Operations

Pins/ Operation	$\overline{REG}$	$\overline{CE_2}$	$\overline{CE_1}$	$\overline{OE}$	$\overline{WE}$	(1, 6) V_{PP2}	(1, 6) V_{PP1}	A0	D_8–D_{15}	D_0–D_7
READ-ONLY										
Read (x8) (Note 7)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IL}	High Z	Data Out-Even
Read (x8) (Note 8)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IH}	High Z	Data Out-Odd
Read (x8) (Note 9)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Data Out-Odd	High Z
Read (x16) (Note 10)	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Data Out Odd	Data Out-Even
Output Disable	V_{IH}	X	X	V_{IH}	V_{IH}	V_{PPL}	V_{PPL}	X	High Z	High Z
Standby	X	V_{IH}	V_{IH}	X	X	V_{PPL}	V_{PPL}	X	High Z	High Z
READ/WRITE										
Read (x8) (Notes 2, 7)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data Out-Even
Read (x8) (Notes 2, 8)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Data Out-Odd
Read (x8) (Notes 2, 9)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	X	Data Out-Odd	High Z
Read (x16) (Notes 2, 10)	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPH}	X	Data Out-Odd	Data Out-Even
Write (x8) (Notes 4, 7)	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data In-Even
Write (x8) (Notes 4, 8)	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Data In-Odd
Write (x8) (Notes 4, 9)	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	X	Data In	High Z
Write (x16) (Notes 5, 10)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	Data In Odd	Data In-Even
Output Disable	V_{IH}	X	X	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	High Z	High Z
Standby (Note 3)	X	V_{IH}	V_{IH}	X	X	V_{PPH}	V_{PPH}	X	High Z	High Z

Legend:

X = Don't Care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2$ V, See DC Characteristics for voltage levels of V_{PPH}, 0 V < An, V_{CC} + 2 V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or < V_{CC} +2 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3.
3. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
4. Refer to Table 3 for valid D_{IN} during a byte write operation.
5. Refer to Table 4 for valid D_{IN} during a word write operation.
6. $V_{PPX} = V_{PPH}$ or V_{PPL}.
7. Byte access – Even. In this x8 mode, $A_0 = V_{IL}$ outputs or inputs the "even" byte (low byte) of the x16 word on D_0–D_7.
8. Byte access – Odd. In this x8 mode, $A_0 = V_{IH}$ outputs or inputs the "odd" byte (high byte) of the x16 word on D_0–D_7. This is accomplished internal to the card by transposing D_8–D_{15} to D_0–D_7.
9. Odd byte only access. In this x8 mode, A_0 = X outputs or inputs the "odd" byte (high byte) of the x16 word on D_8–D_{15}.
10. x16 word accesses present both "even" (low) and "odd" (high) bytes. $A_0 = V_{IL}$ or V_{IH} = "Don't Care".

Table 2B. Attribute Memory Bus Operations

Pins/ Operation	$\overline{REG}$	$\overline{CE_2}$	$\overline{CE_1}$	$\overline{OE}$	$\overline{WE}$	(1, 6) V_{PP2}	(1, 6) V_{PP1}	A0	D_8–D_{15}	D_0–D_7
READ-ONLY										
Read (x8) (Notes 7, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IL}	High Z	Data Out-Even
Read (x8) (Notes 8, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IH}	High Z	Not Valid
Read (x8) (Note 8)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Not Valid	High Z
Read (x16) (Notes 8, 9, 10)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Not Valid	Data Out-Even
Output Disable	V_{IL}	X	X	V_{IH}	V_{IH}	V_{PPL}	V_{PPL}	X	High Z	High Z
Standby	X	V_{IH}	V_{IH}	X	X	V_{PPL}	V_{PPL}	X	High Z	High Z
READ/WRITE										
Read (x8) (Notes 2, 7, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data Out-Even
Read (x8) (Notes 2, 8, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Not Valid
Read (x8) (Note 9)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	X	Not Valid	High Z
Read (x16) (Notes 2, 9)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPH}	X	Not Valid	Data Out-Even
Write (x8) (Notes 4, 7, 10)	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data In-Even
Write (x8) (Notes 4, 8, 10)	V_{IL}	V_{IIH}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Not Valid
Write (x8) (Notes 4, 9, 10)	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	X	Not Valid	High Z
Write (x16) (Note 10)	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	Not Valid	Data In-Even
Output Disable	V_{IL}	X	X	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	High Z	High Z
Standby (Note 3)	X	V_{IH}	V_{IH}	X	X	V_{PPH}	V_{PPH}	X	High Z	High Z

Legend:

X = Don't Care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2$ V, See DC Characteristics for voltage levels of V_{PPH}, 0 V < An, V_{CC} + 2 V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or < V_{CC} +2 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3.
3. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
4. Refer to Table 3 for valid D_{IN} during a write operation.
5. Refer to Table 4 for valid D_{IN} during a write operation.
6. $V_{PPX} = V_{PPH}$ or V_{PPL}.
7. In this x8 mode, $A_0 = V_{IL}$ outputs or inputs the "even" byte (low byte) of the x16 word on D_0–D_7.
8. Only even-byte data is valid during Attribute Memory Read function.
9. During Attribute Memory Read function, $\overline{REG}$ and $\overline{OE}$ must be active for the entire cycle.
10. During Attribute Memory Write function, $\overline{REG}$ and $\overline{WE}$ must be active for the entire cycle, $\overline{OE}$ must be inactive for the entire cycle.

Table 3. Command Definitions for Byte-Wide Operations

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Note 6)	Write	X	00H/FFH	Read	RA	RD
Read Auto Select (Note 7)	Write	X	90H	Read	00H/01H	01H/A2H
Embedded Set-up/Erase Embedded Erase™ (Note 4)	Write	X	30H	Write	X	30H
Embedded Set-up Program/ Embedded Program™ (Note 5)	Write	X	50H	Write	PA	PD
Reset (Note 6)	Write	X	FFH	Write	X	FFH

Notes:

1. Bus operations are defined in Table 2A.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   SA = Address of memory segment to be erased.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. Figure 1 illustrates the Embedded Erase Algorithm.
5. Figure 2 illustrates the Embedded Programming Algorithm.
6. Please reference Reset Command section.
7. Please reference Auto Select section.
   Address: 00H/01H = MFG code / Device code addresses.
   Data: 01H/A2H = MFG code data / Device code data.

Table 4. Command Definitions for Word-Wide Operations

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Note 6)	Write	X	0000H/ FFFFH	Read	RA	RD
Read Auto Select (Note 7)	Write	X	9090H	Read	0000H/ 0101H	0101H/ A7A7H
Embedded Erase Set-up/Erase	Write	SA	3030H	Write	X	3030H
Embedded Set-up Program/ Embedded Program	Write	X	5050H	Write	PA	PD
Reset (Note 6)	Write	X	FFFFH	Write	X	FFFFH

Notes:

1. Bus operations are defined in Table 2A.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   SA = Address of memory segment to be erased.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. Figure 1 illustrates the Embedded Electrical Erase Algorithm.
5. Figure 2 illustrates the Embedded Programming Algorithm.
6. Please reference Reset Command section.
7. Please reference Auto Select section.

FLASH MEMORY PROGRAM/ERASE OPERATIONS

Details of AMD's Embedded Program and Erase Operations

Embedded Erase™ Algorithm

The automatic memory segment erase does not require the device to be entirely pre-programmed prior to executing the Embedded erase set-up command and Embedded erase command. Upon executing the Embedded erase command, the addressed memory segment automatically will program and verify the entire memory for an all zero data pattern. The system is not required to provide any controls or timing during these operations.

When the memory segment is automatically verified to contain an all zero pattern, a self-timed chip erase and verify begin. The erase and verify operation are complete when the data on DQ7 of the memory segment is "1" (see Write Operation Status section) at which time the device returns to Read mode. The system is not required to provide any control or timing during these operations.

When using the Embedded Erase algorithm, the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verify command is required). The margin voltages are internally generated in the same manner as when the standard erase verify command is used.

The Embedded erase set-up command is a command only operation that stages the memory segment for automatic electrical erasure of all bytes in the array. Embedded erase set-up is performed by writing 30H to the command register of the addressed memory segment.

To commence automatic segment erase, the command 30H must be written again to the command register. The automatic erase begins on the rising edge of the $\overline{WE}$ and terminates when the data on DQ7 of the memory segment is "1" (see Write Operation Status section) at which time the device returns to Read mode.

Figure 1 and Table 5 illustrate the Embedded Erase algorithm, a typical command string and bus operations.

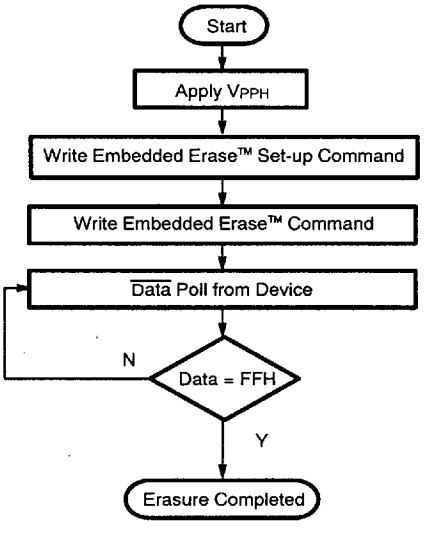


Figure 1. Embedded Erase™ Algorithm in Byte-Wide Mode

Table 5. Embedded Erase Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH} (1)
Write	Embedded Erase Set-up Command	Data = 30H
Write	Embedded Erase Command	Data = 30H
Read		Data Polling to Verify Erasure
Standby		Compare Output to FFH
Read		Available for Read Operations

Note:

1. See DC Characteristics for value of V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V. Refer to Principles of Operation.

Embedded Program™ Algorithm

The Embedded Program Set-up is a command only operation that stages the addressed memory segment for automatic programming. Embedded Program Set-up is performed by writing 50H to the command register.

Once the Embedded Program Set-up operation is performed, the next $\overline{WE}$ pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the $\overline{WE}$ pulse. Data is internally latched on the rising edge of the $\overline{WE}$ pulse. The rising edge of $\overline{WE}$ also begins the programming operation. The system is not required to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin. The automatic programming operation is completed when the data on DQ7 of the addressed memory segment is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to Read mode (no program verify command is required).

Figure 2 and Table 6 illustrate the Embedded Program algorithm, a typical command string, and bus operation.

Reset Command

The reset command initializes the memory segment to the read mode. In addition, it also provides a safe method to abort any memory segment operation (including program or erase). The reset command must be written two consecutive times after the program set-up command. This will safely reset the segment memory to the read mode. Memory contents are not altered. Following any other command, write the reset command once to the segment. This will safely abort any operation and reset the device to the Read mode.

Table 6. Embedded Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH} (1)
Write	Embedded Program Set-up Command	Data = 50H
Write	Embedded Program Command	Valid Address/Data
Read		$\overline{Data}$ Polling to Verify Completion
Read		Available for Read Operations

Note:

1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V. Refer to Principles of Operation. Device is either powered-down, erase inhibit or program inhibit.

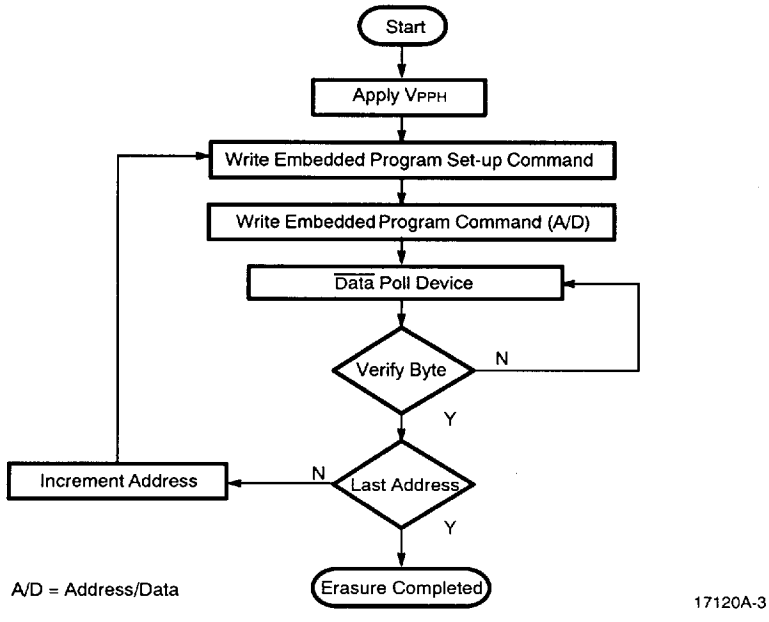


Figure 2. Embedded Programming Algorithm in Byte-Wide Mode

Write Operation Status

Data Polling—DQ7

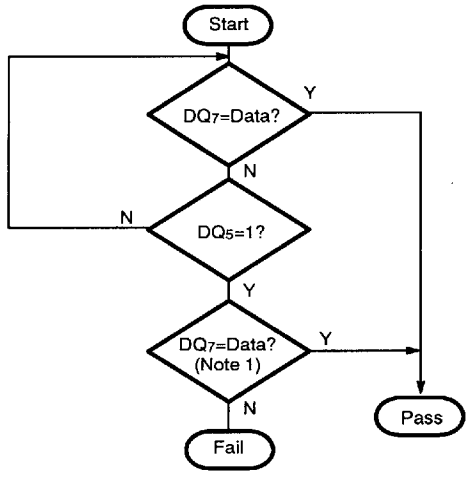
The Flash Memory PC Card features Data Polling as a method to indicate to the host system that the Embedded algorithms are either in progress or completed.

While the Embedded Programming algorithm is in operation, an attempt to read the device will produce the compliment of expected Valid data on DQ7 of the addressed memory segment. Upon completion of the Embedded Program algorithm an attempt to read the device will produce Valid data on DQ7. The Data Polling feature is valid after the rising edge of the second WE pulse of the two write pulse sequence.

While the Embedded Erase algorithm is in operation, DQ7 will read "0" until the erase operation is completed. Upon completion of the erase operation, the data on DQ7 will read "1". The Data Polling feature is valid after the rising edge of the second WE pulse of the two Write pulse sequence.

The Data Polling feature is only active during Embedded Programming or erase algorithms.

See Figures 3a and 4a for the Data Polling timing specifications and diagrams.



Note:

1. DQ_7 is rechecked even if DQ_5 = 1 because DQ_7 may change simultaneously with DQ_5.

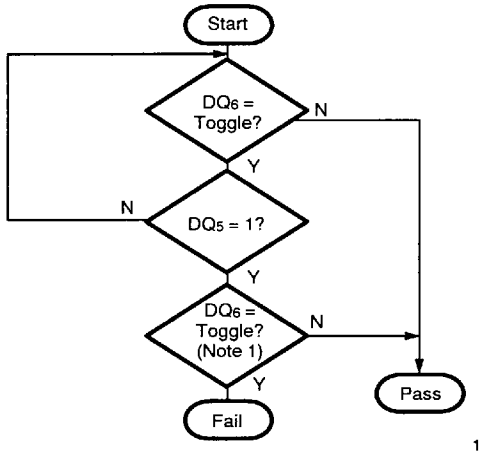
Figure 3a. $\overline{\text{Data}}$ Polling Algorithm

Toggle Bit—DQ6

The Flash Memory PC Card also features a "Toggle Bit" as a method to indicate to the host system that the Embedded algorithms are either in progress or completed.

While the Embedded Program or Erase algorithm is in progress, successive attempts to read data from the device will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase algorithm is completed, DQ6 will stop toggling and valid data will be read. The toggle bit is valid after the rising edge of the first $\overline{\text{WE}}$ pulse of the two write pulse sequence, unlike $\overline{\text{Data}}$ Polling which is valid after the rising edge of the second $\overline{\text{WE}}$ pulse. This feature allows the user to determine if the device is partially through the two write pulse sequence.

See Figures 3b and 4a for the $\overline{\text{Data}}$ Polling timing specifications and diagrams.



Note:

1. DQ_6 is rechecked even if DQ_5 = 1 because DQ_6 may stop toggling at the same time as DQ_5 changing to "1".

Figure 3b. Toggle Bit Algorithm

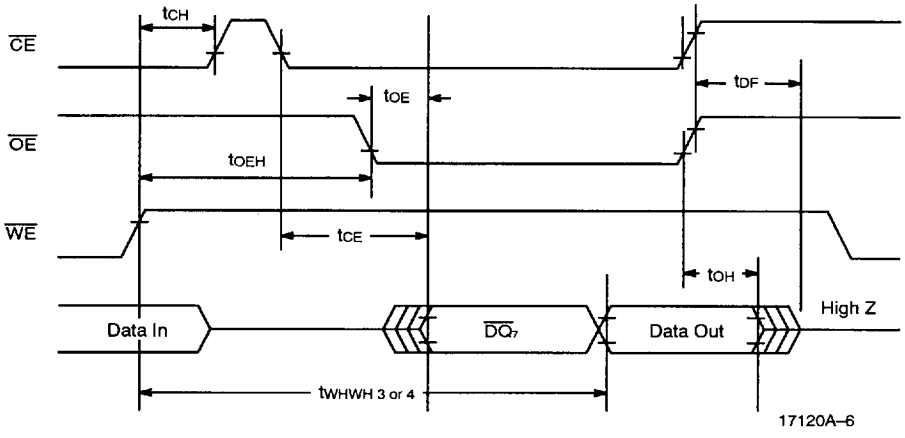
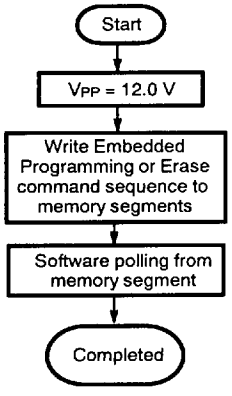


Figure 4a. AC Waveforms for Data Polling During Embedded Algorithm Operations

EMBEDDED ALGORITHM BYTE-WIDE PROGRAMMING AND ERASURE OVERVIEW

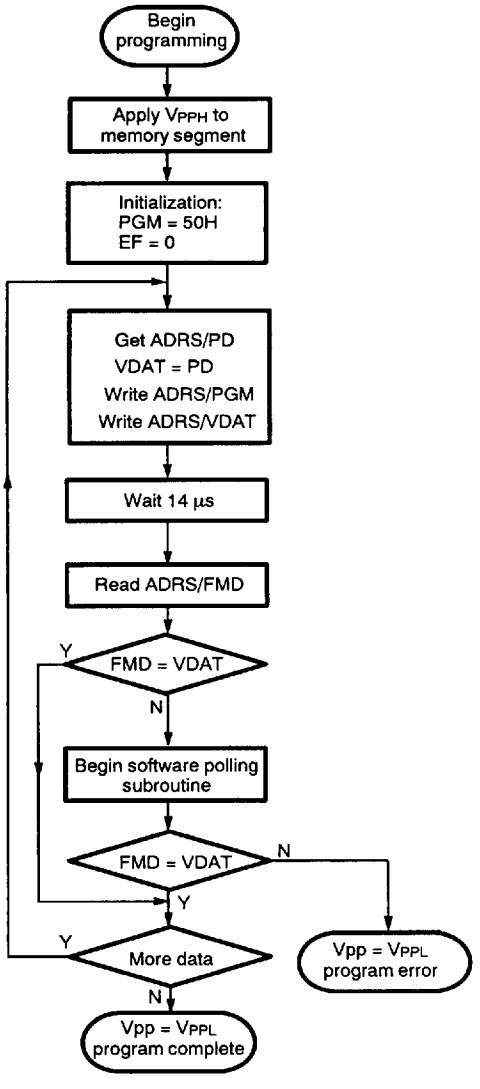


17120A-9

The Embedded Algorithm operations completely automate the programming and erase procedure by internally executing the algorithmic command sequence of original AMD devices. The devices automatically provide Write Operation Status information with standard read operations (addresses are a don't care).

Figure 5.

EMBEDDED ALGORITHM BYTE-WIDE PROGRAMMING FLOW CHART



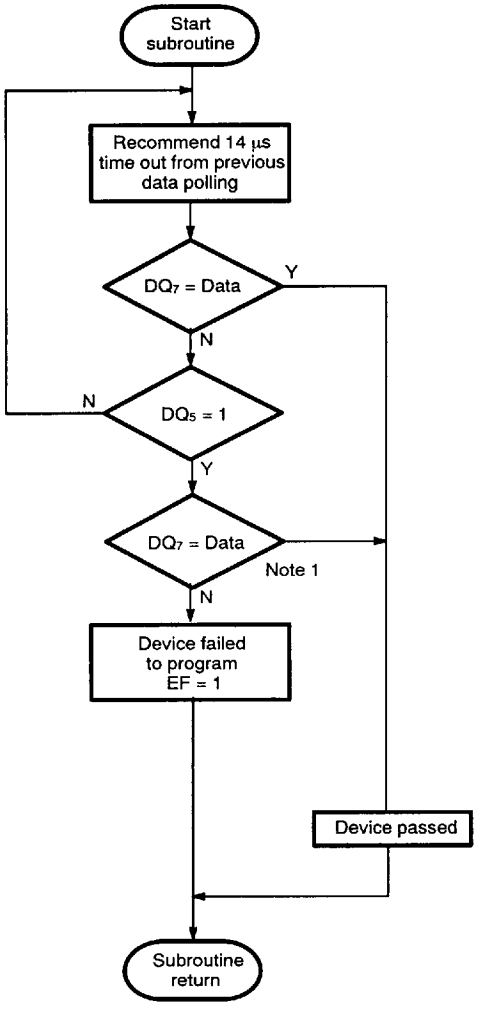
Activity	
Initialize Programming Variables:	*PGM = Embedded Set up Command* *EF = Error Flag*
ADRS = Appropriate address for memory segment.	*PD = Program Data* *VDAT = Valid Data.*
FMD = Flash Memory Data.	
EF = 0 = No Programming error	*EF = 1 = Programming error*

17120A–7

Figure 6.

EMBEDDED ALGORITHM BYTE-WIDE SOFTWARE POLLING FOR PROGRAMMING

Subroutine



DQ5 = 1
N = Program time not exceeded limit
Y = Program time exceed limit, device failed

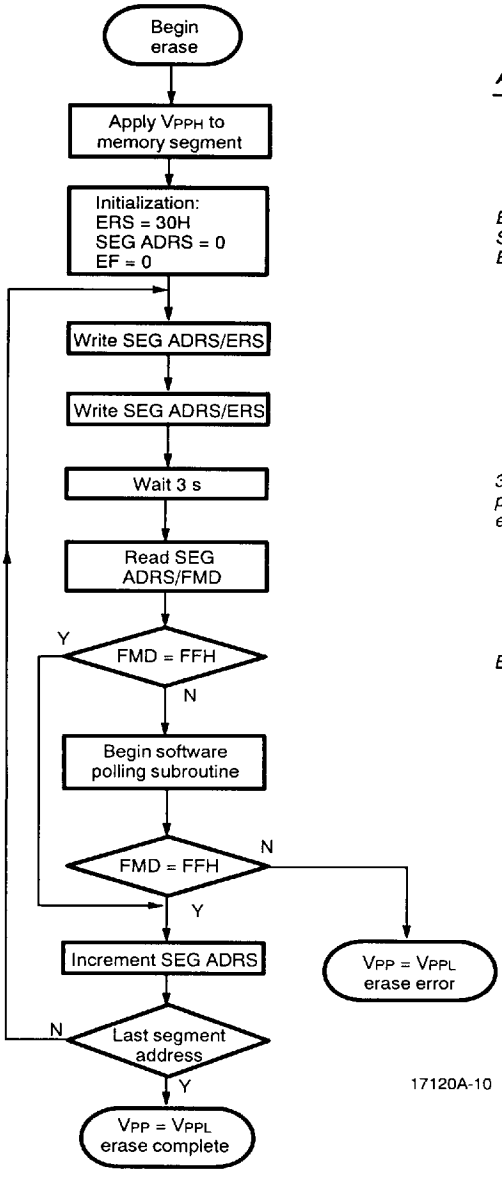
17120A-8

Note:

1. DQ_7 is checked even if $DQ_5 = 1$ because DQ_7 may have changed simultaneously with DQ_5 or immediately after DQ_5.

Figure 7.

EMBEDDED ALGORITHM BYTE-WIDE ERASURE FLOW CHART



Activity

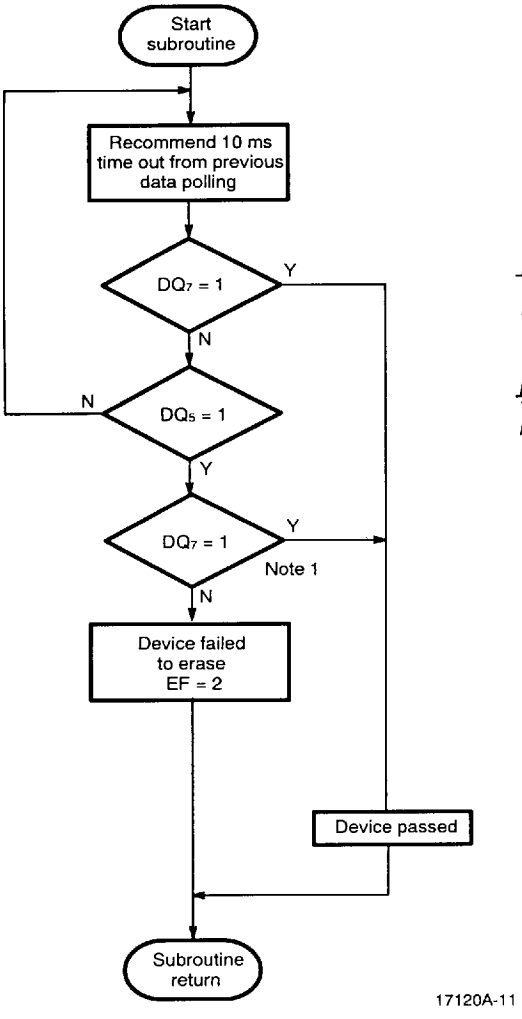
ERS = Erase Command
SEGment ADdReSs = 0
Error Flag = 0

3 seconds wait = 2 seconds memory segment preprogram time +1 second memory segment erase time.

Erased Flash Memory Data = FFH.

Figure 8.

EMBEDDED ALGORITHM BYTE-WIDE SOFTWARE POLLING ERASE SUBROUTINE



DQ7 = 1
Y = Erase Complete
N = Erase not Complete

DQ5 = 1
Y = Erase time exceeded limit, Device failed.
N = Erase time has not exceeded limit.

Figure 9.

WORD-WIDE PROGRAMMING AND ERASING

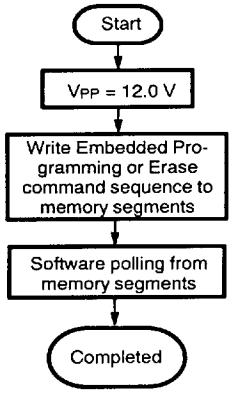
Word-Wide Programming

The word-wide programming sequence will be as usual. The program word command is 5050H. Each byte is independently programmed. For example, if the high byte of the word indicates the successful completion of programming via one of its program status bits such as DQ7, software polling should continue to monitor the low byte for program completion and data verification. During the Embedded Programming operations the device executes programming pulses in 14 μs increments. Status reads provide information on the progress of the byte programming relative to the last complete program pulse. Status information is automatically updated upon completion of each internal program pulse. Status information does not change within the 14 μs program pulse width.

Word-Wide Erasing

The word-wide erasing is similar to word-wide programming. The erase word command is 3030H. Each byte is independently erased and verified. Word-wide erasure reduces total erase time when compared to byte erasure. Each Flash memory device in the card may erase at different rates. Therefore each device (byte) must be verified separately. The alternate method mentioned above also apply to erasure. Since the same 40 MHz system, 1 second of CPU time is equivalent to 40 million clock cycles.

EMBEDDED ALGORITHM WORD-WIDE PROGRAMMING AND ERASURE OVERVIEW

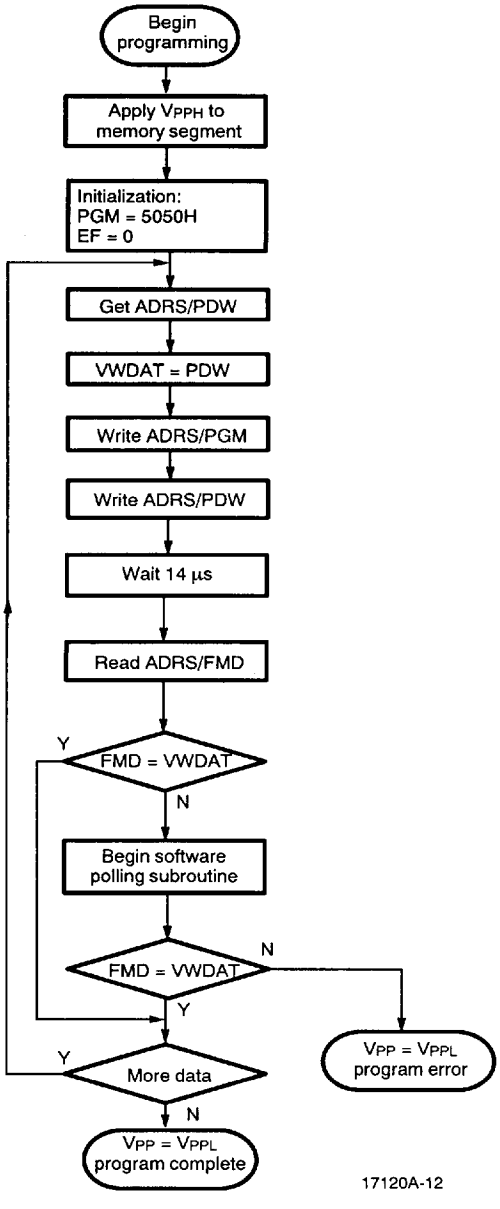


17120A-14

The Embedded Algorithm operations completely automate the parallel programming and erase procedures by internally executing the algorithmic command sequences of AMD's Flashrite and Flasherase algorithms. The devices automatically provide Write Operation Status information with standard read operations.

Figure 10.

EMBEDDED ALGORITHM WORD-WIDE PROGRAMMING FLOW CHART



Activity

Initialize Programming Variables:
PGM = Embedded Set up Command
EF = Error Flag

ADRS = Appropriate address for memory segment.
PDW = Program Data Word
VWDAT = Valid Word Data
EF = Error Flag
EF = 0 = No failure
EF = 1 = Low byte program error
EF = 2 = High byte program error
EF = 3 = Word-wide program error

FMD = Valid Word Data

Figure 11.

EMBEDDED ALGORITHM WORD-WIDE SOFTWARE POLLING PROGRAM SUBROUTINE

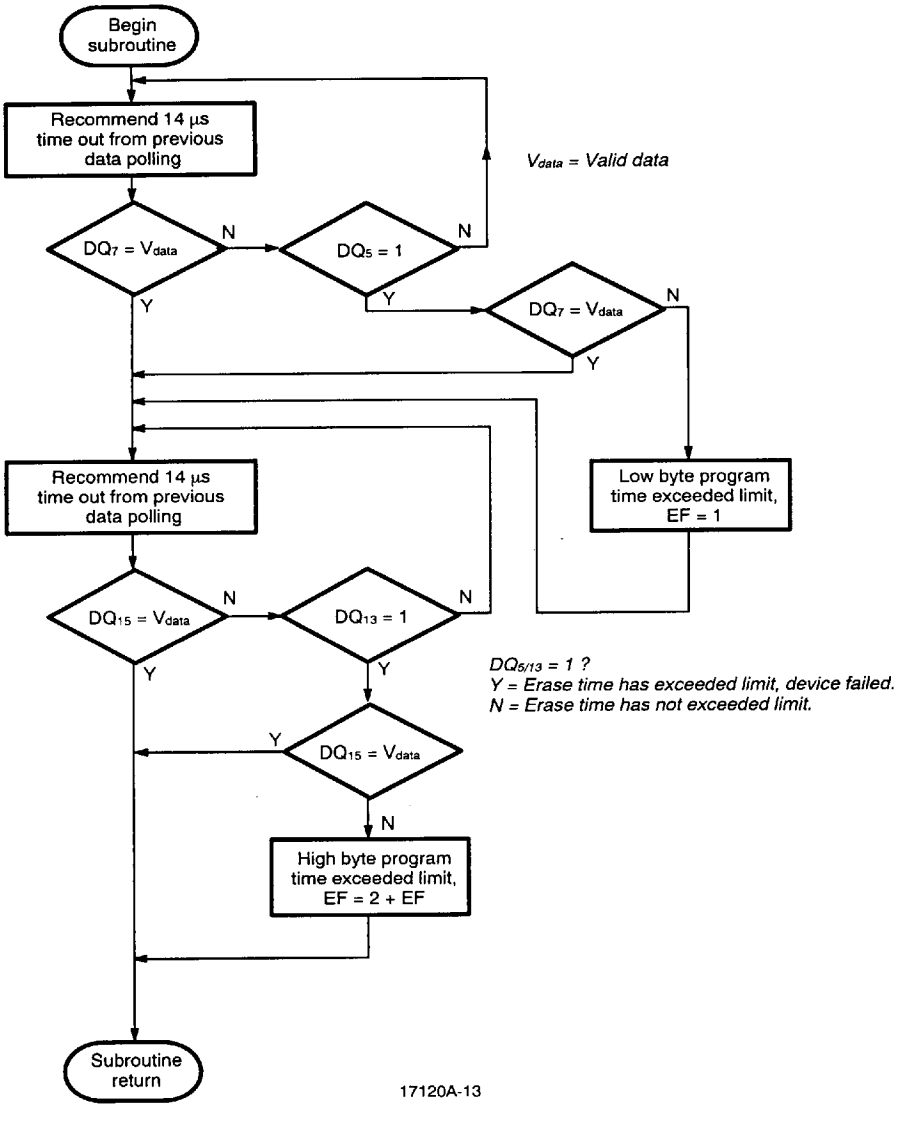
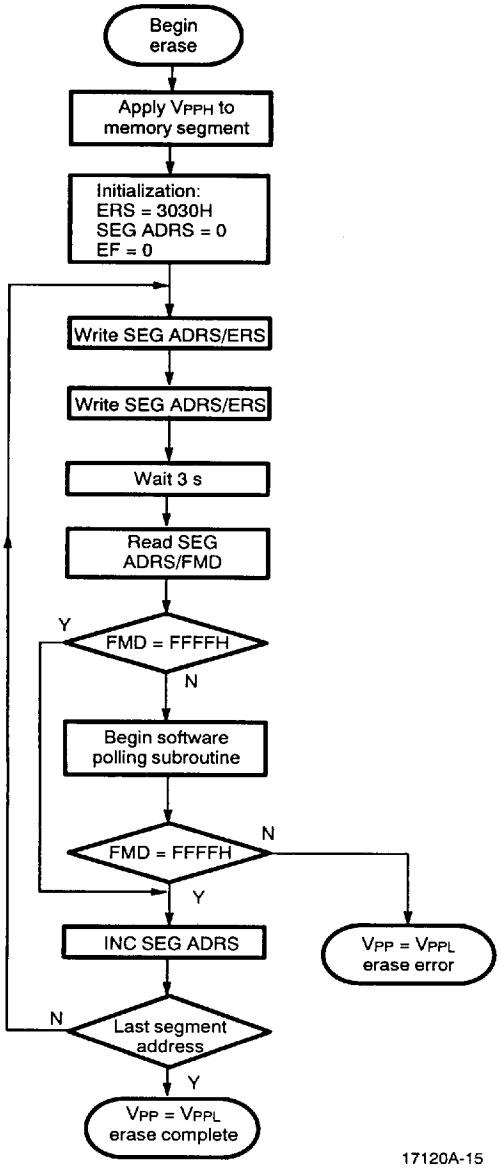


Figure 12.

EMBEDDED ALGORITHM WORD-WIDE ERASURE FLOW CHART



Activity

ERS = Erase Command
SEG ADRS = Segment Address

EF = Error Flag
EF = 0 = No failure
EF = 1 = Low byte Erase error
EF = 2 = High byte Erase error
EF = 3 = Word-wide Erase error

FMD = Flash Memory Data

Figure 13.

EMBEDDED ALGORITHM WORD-WIDE SOFTWARE POLLING ERASE SUBROUTINE

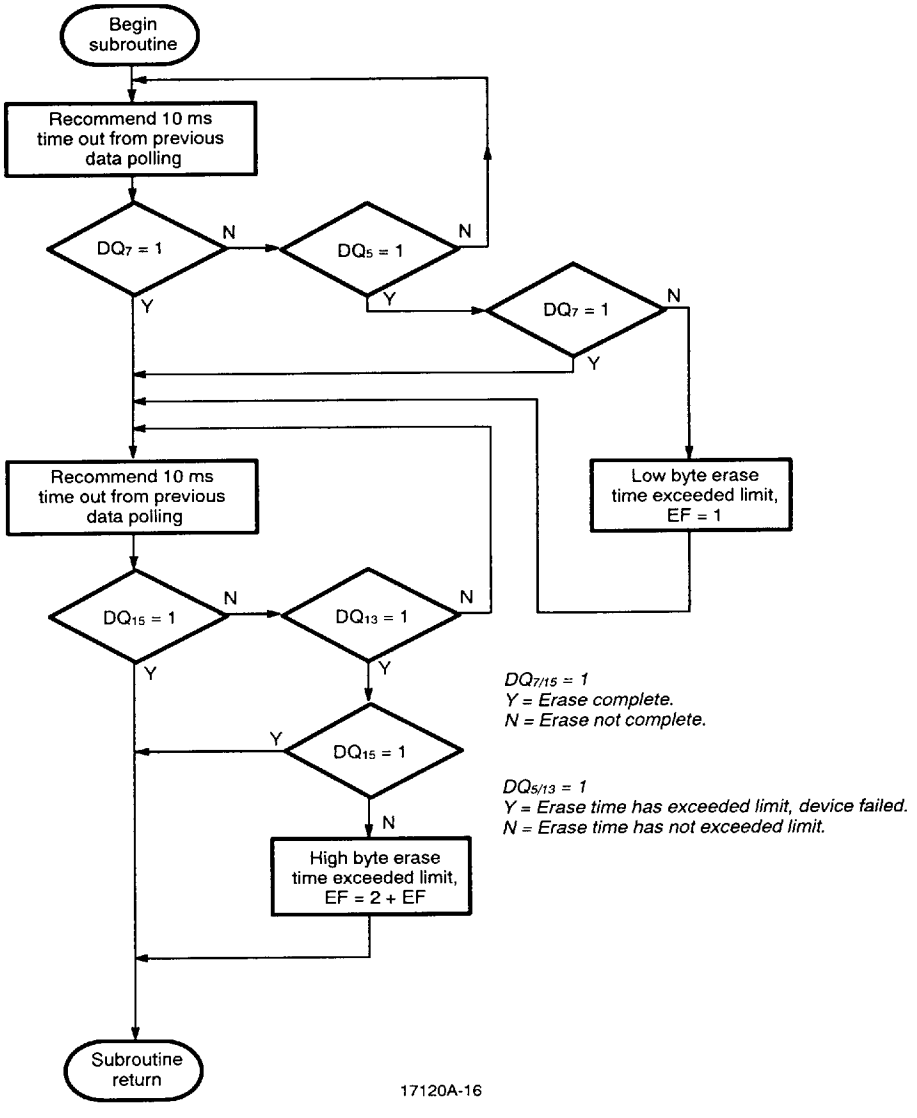


Figure 14.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −30°C to +70°C

Ambient Temperature
with Power Applied ..... −10°C to +70°C

Voltage with Respect To Ground
All pins except V_{PP} (Note 1) ..... −2.0 V to +7.0 V

V_{CC} (Note 1) ..... −2.0 V to +7.0 V

V_{PP} (Note 2) ..... −2.0 V to +14.0 V

Output Short Circuit Current (Note 3) ..... 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is −0.5 V. During voltage transitions, inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.

2. Minimum DC input voltage on V_{PP} pins is −0.5 V. During voltage transitions, V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC input voltage on V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.

3. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second. Conditions equal V_{OUT} = 0.5 V or 5.0 V, V_{CC} = V_{CC} max. These values are chosen to avoid test problems caused by tester ground degradation. This parameter is sampled and not 100% tested, but guaranteed by characterization.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C) ..... 0°C to +60°C

V_{CC} Supply Voltages ..... +4.75 V to 5.25 V

V_{PP} Supply Voltages

Read Only ..... 0 V to +6.5 V

Program, Erase, Verify,
and Read ..... +11.4 V to +12.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

Byte Wide Operation

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}		1.0	±20	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}		1.0	20	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. CE = V_{CC} ± 0.2 V		0.4	0.8	mA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., CE = V_{IL}, OE = V_{IH}, I_{OUT} = 0 mA, at 6 MHz		25	50	mA
I_{CC2}	V_{CC} Programming Current	CE = V_{IL} Programming in Progress		3.0	30	mA
I_{CC3}	V_{CC} Erase Current	CE = V_{IL} Erasure in Progress		5.0	30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} ≤ V_{CC}			10	µA
I_{PP1}	V_{PP} Read Current	V_{PP} > V_{CC}		0.2	0.4	mA
		V_{PP} ≤ V_{CC}			0.04	
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPL} Programming in Progress		8.0	30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage	Except $\overline{CE}$, $\overline{REG}$ = 3.2 V Min.	2.4		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA V_{CC} = V_{CC} Min.			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = –2.0 mA V_{CC} = V_{CC} Min.	3.8			V
V_{PPL}	V_{PP} During Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0		V_{CC}+2	V
V_{PPH}	V_{PP} During Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2			V

Notes:
1. One Flash device active, seven in standby.
2. Only one Vpp is active.

DC CHARACTERISTICS
Word-Wide Operation

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = Vcc or Vss		1.0	±20	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = Vcc or Vss		1.0	20	µA
I_{CCS}	Vcc Standby Current	V_{CC} = V_{CC} Max. CE = V_{CC} ± 0.2 V		0.4	0.8	mA
I_{CC1}	Vcc Active Read Current	V_{CC} = V_{CC} Max., CE = V_{IL}, OE = V_{IH}, I_{OUT} = 0 mA, at 6 MHz		40	80	mA
I_{CC2}	Vcc Programming Current	CE = V_{IL} Programming in Progress		6	60	mA
I_{CC3}	Vcc Erase Current	CE = V_{IL} Erasure in Progress		10	60	mA
I_{PPS}	VPP Standby Current	$V_{PP} \leq V_{CC}$			10	µA
I_{PP1}	VPP Read Current	$V_{PP} > V_{CC}$		0.4	0.8	mA
		$V_{PP} \leq V_{CC}$			0.08	
I_{PP2}	VPP Programming Current	V_{PP} = V_{PPL} Programming in Progress		16	60	mA
I_{PP3}	VPP Erase Current	V_{PP} = V_{PPH} Erasure in Progress		20	60	mA
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage	Except $\overline{CE}$, $\overline{REG}$ = 3.2 V Min.	2.4		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA V_{CC} = V_{CC} Min.			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = 2.0 mA V_{CC} = V_{CC} Min.	3.8			V
V_{PPL}	VPP During Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0		V_{CC}+2	V
V_{PPH}	VPP During Read/Write Operations		11.4		12.6	V
V_{LKO}	Low Vcc Lock-Out Voltage		3.2			V

Notes:
1. Two Flash devices active, six in standby.
2. V_{pp1} and V_{pp2} are active.

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN1}	Address Capacitance	V_{IN} = 0		21	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0		21	pF
C_{IN2}	Control Capacitance	V_{IN} = 0 ($\overline{CE}$, $\overline{REG}$)		47	pF
$C_{I/O}$	I/O Capacitance	$V_{I/O}$ = 0		21	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0 MHz.

SWITCHING AC CHARACTERISTICS

Read Only Operation (Note 1)

Parameter Symbols		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
t_{AVAV}	t_{RC}	Read Cycle Time	250		ns
t_{ELQV}	t_{CE}	Chip Enable Access Time		250	ns
t_{AVQV}	t_{ACC}	Address Access Time		250	ns
t_{GLQV}	t_{OE}	Output Enable Access Time		150	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z	5		ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z		60	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5		ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z		60	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change	5		ns
t_{WHGL}		Write Recovery Time before Read	6		µs

Note:

1. Input Rise and Fall Times (10% to 90%): ≤ 10 ns, Input Pulse levels: V_{OL} and V_{OH}, Timing Measurement Reference Level – Inputs: V_{IL} and V_{IH} Outputs: V_{IL} and V_{IH}

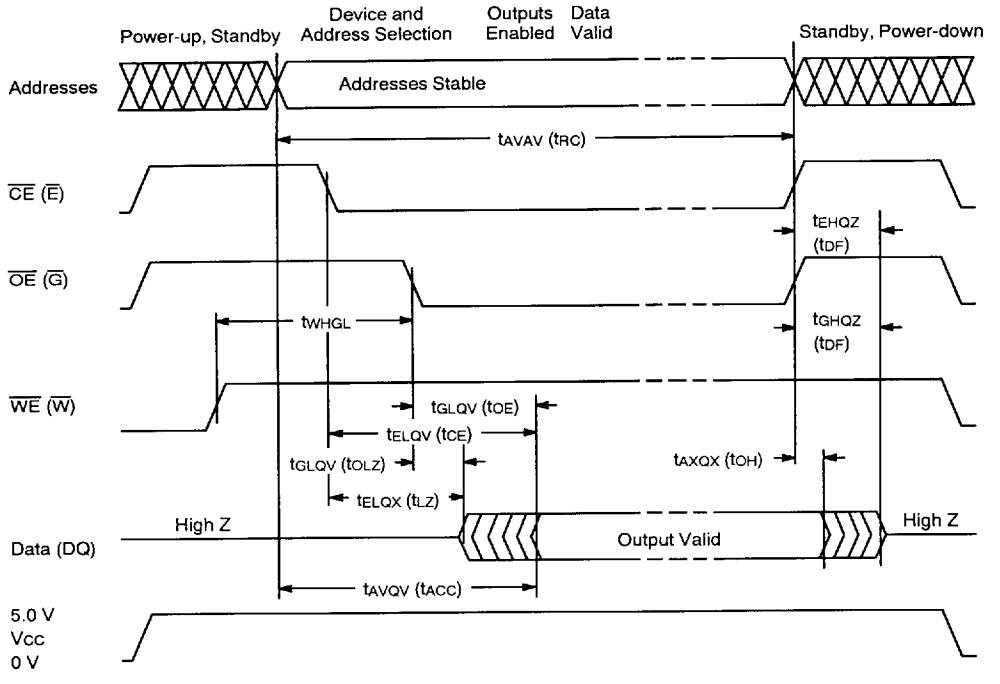
AC CHARACTERISTICS

Write/Erase/Program Operations

Parameter Symbols		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
t_{AVAV}	t_{WC}	Write Cycle Time	250		ns
t_{AVWL}	t_{AS}	Address Set-Up Time	0		ns
t_{WLAX}	t_{AH}	Address Hold Time	100		ns
t_{DVWH}	t_{DS}	Data Set-Up Time	80		ns
t_{WHDX}	t_{DH}	Data Hold Time	30		ns
t_{OEH}		Output Enable Hold Time for Embedded Algorithm	30		ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	6		µs
t_{GHWL}		Read Recovery Time before Write	0		µs
t_{WLOZ}		Output in High-Z from Write Enable	5		ns
t_{WHOZ}		Output in Low-Z from Write Enable		60	ns
t_{ELWL}	t_{CS}	Chip Enable Set-Up Time	40		ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	0		ns
t_{WLWH}	t_{WP}	Write Pulse Width	100		ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	50		ns
t_{WHWH3}		Embedded Programming Operation (Notes 1, 2, 3)	14		µs
t_{WHWH4}		Embedded Erase Operation for each 128 KB Memory Segment (Notes 1, 2, 4)	3		s
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW	100		ns

Notes:

1. Rise/Fall < = 10 ns.
2. Maximum specification not needed due to the devices internal stop timer that will stop any erase or write operation that exceed the device specification.
3. Embedded Program Operation of 14 µs consist of 10 µs program pulse and 4 µs write recovery before read. This is the minimum time for one pass through the programming algorithm.
4. Embedded Erase Operation of 3 seconds consists of 2 seconds memory segment pre-programming times and 1 second memory segment erase time for each 128K byte memory segment. This is typical time for embedded erase operation.



Note: $\overline{CE}$ refers to $\overline{CE}_{1,2}$

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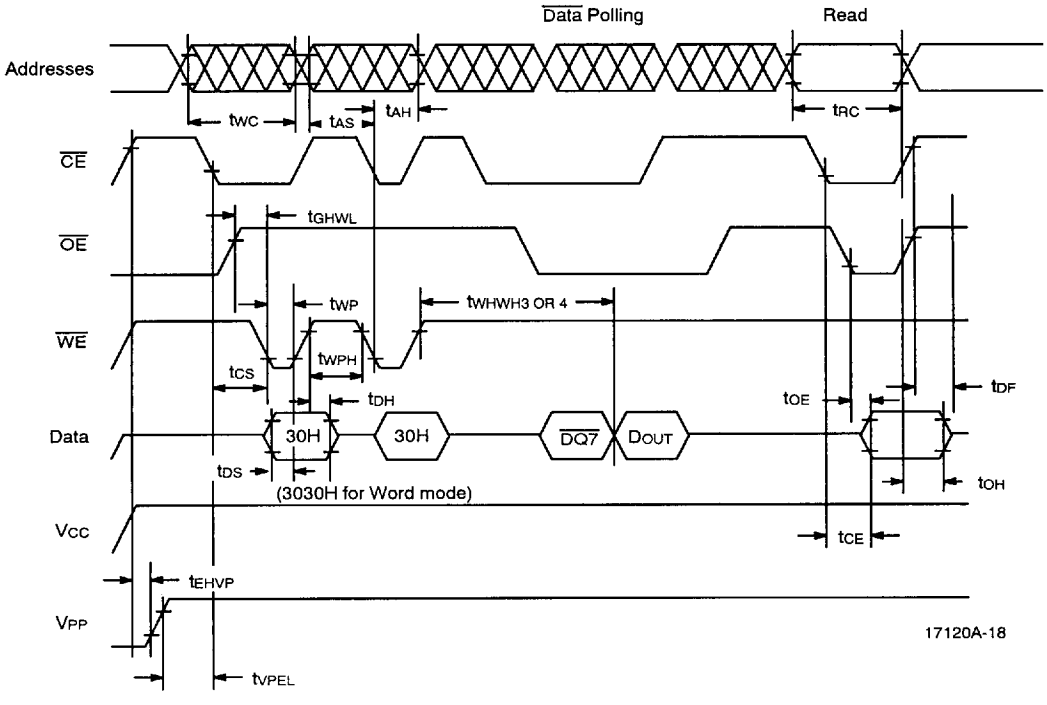
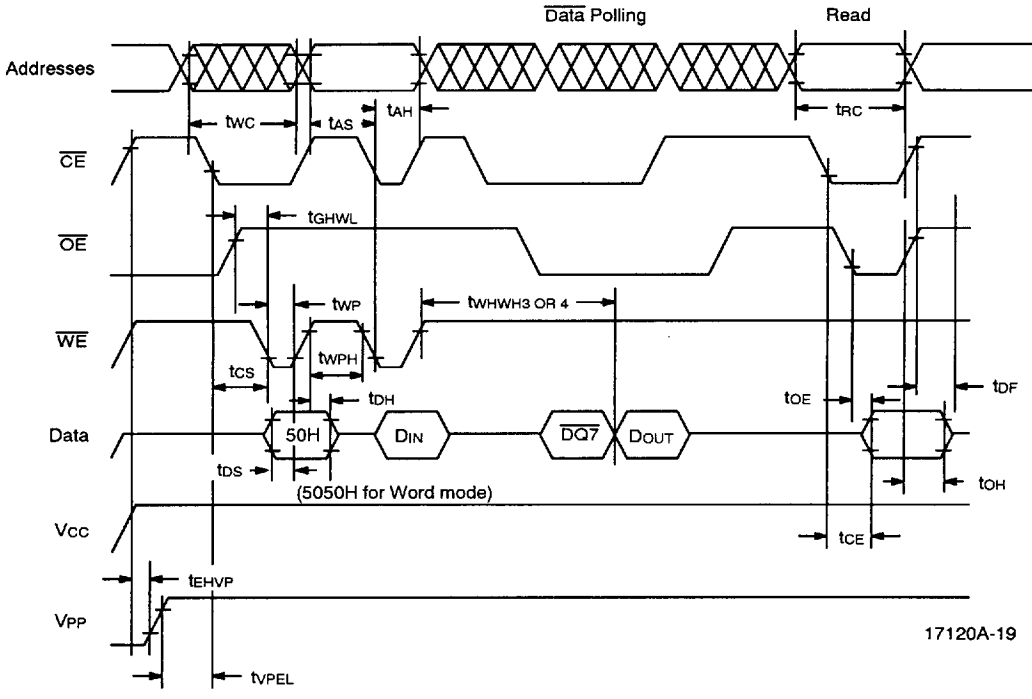
Figure 15. AC Waveforms for Read Operations



Notes:

1. D_{IN} is data input to the device.
2. $\overline{D_{Q7}}$ is the output of the complement of the data written to the device.
3. D_{OUT} is the output of the data written to the device.

Figure 16. AC Waveforms for Embedded Erase Operation



Notes:

1. D_{IN} is data input to the device.
2. $\overline{DQ7}$ is the output of the complement of the data written to the device.
3. D_{OUT} is the output of the data written to the device.

Figure 17. AC Waveforms for Embedded Programming Operation

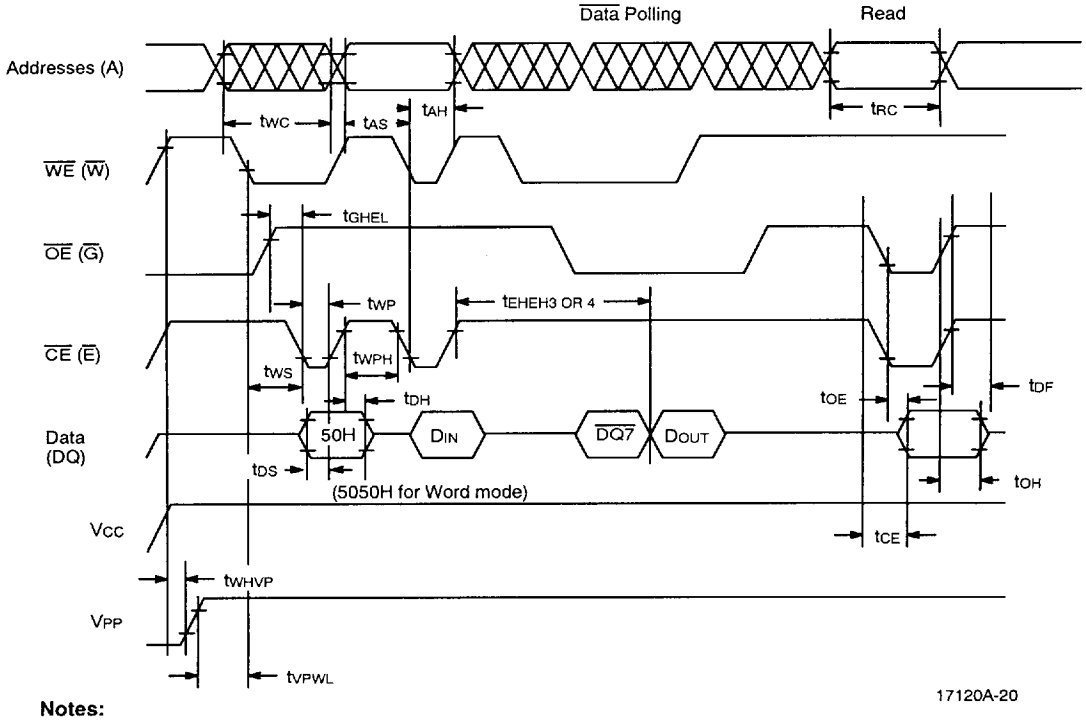
AC CHARACTERISTICS–ALTERNATE $\overline{CE}$ CONTROLLED WRITES

Write/Erase/Program Operations

Parameter Symbols		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
t_{AVAV}	t_{WC}	Write Cycle Time	250		ns
t_{AVEL}	t_{AS}	Address Set-Up Time	0		ns
t_{ELAX}	t_{AH}	Address Hold Time	100		ns
t_{DVEH}	t_{DS}	Data Set-Up Time	80		ns
t_{EHDX}	t_{DH}	Data Hold Time	30		ns
t_{GLDV}	t_{OE}	Output Enable Hold Time for Embedded Algorithm	10	150	ns
t_{GHEL}		Read Recovery Time before Write	0		µs
t_{WLEL}	t_{WS}	WE Set-Up Time before $\overline{CE}$	0		ns
t_{EHWH}	t_{CP}	WE Hold Time	0		ns
t_{ELEH}	t_{CP}	Write Pulse Width	100		ns
t_{EHEL}	t_{CPH}	Write Pulse Width HIGH (Note 3)	50		ns
t_{EHEH3}		Embedded Programming Operation (Note 4)	14		µs
t_{EHEH4}		Embedded Erase Operation for each 128 KB Memory Segment (Notes 1, 2, 4)	3		s
t_{VPWL}		V_{PP} Set-Up Time to Write Enable LOW	100		ns

Notes:

1. Rise/Fall < =10 ns
2. Maximum specification not needed due to the internal stop timer that will stop any erase or write operation that exist the device specification.
3. Chip Enable Controlled Programming:
   Flash Programming is controlled by the valid combination of the Chip Enable ($\overline{CE}_{1,2}$) and Write Enable ($\overline{WE}$) signals. For system that uses the Chip Enable signal(s) to define the write pulse width, all Set-up, Hold, and inactive Write Enable timing should be measured relative to the Chip Enable signal(s).
4. Embedded Program Operation of 14 µs consist of 10 µs program pulse and 4 µs write recovery before read. This is the minimum time for one pass through the programming algorithm.
5. Embedded Erase Operation of 3 seconds consists of 2 seconds memory segment pre-programming times and 1 second memory segment erase time for each 128K byte memory segment. This is typical time for embedded erase operation.



Notes:

1. D_{IN} is data input to the device.
2. $\overline{D_{Q7}}$ is the output of the complement of the data written to the device.
3. D_{OUT} is the output of the data written to the device.

Figure 18. Alternate AC Waveforms for $\overline{CE}$ Controlled Embedded Programming or Erasing Operation

CARD INFORMATION STRUCTURE

The AmC001AFLKA contains a separate 512 byte EEPROM memory for the Card Information Structure. All or part of the 512 byte could be used for the card's attribute memory space. This allows all of the Flash memory to be used for the common memory space. Part of the common memory space could also be mapped into the attribute memory space if more than 512 bytes of CIS are needed.

The EEPROM used in the AmC001AFLKA is a NEC μPD28C05GX-20-EJA designed to operate from a 5 V single power supply. The μPD28C05 provides a DATA polling function that provides the End of Write Cycle, Chip Erase and Auto Erase and Programming functions.

SYSTEM DESIGN AND INTERFACE INFORMATION

Power Up and Power Down Protection

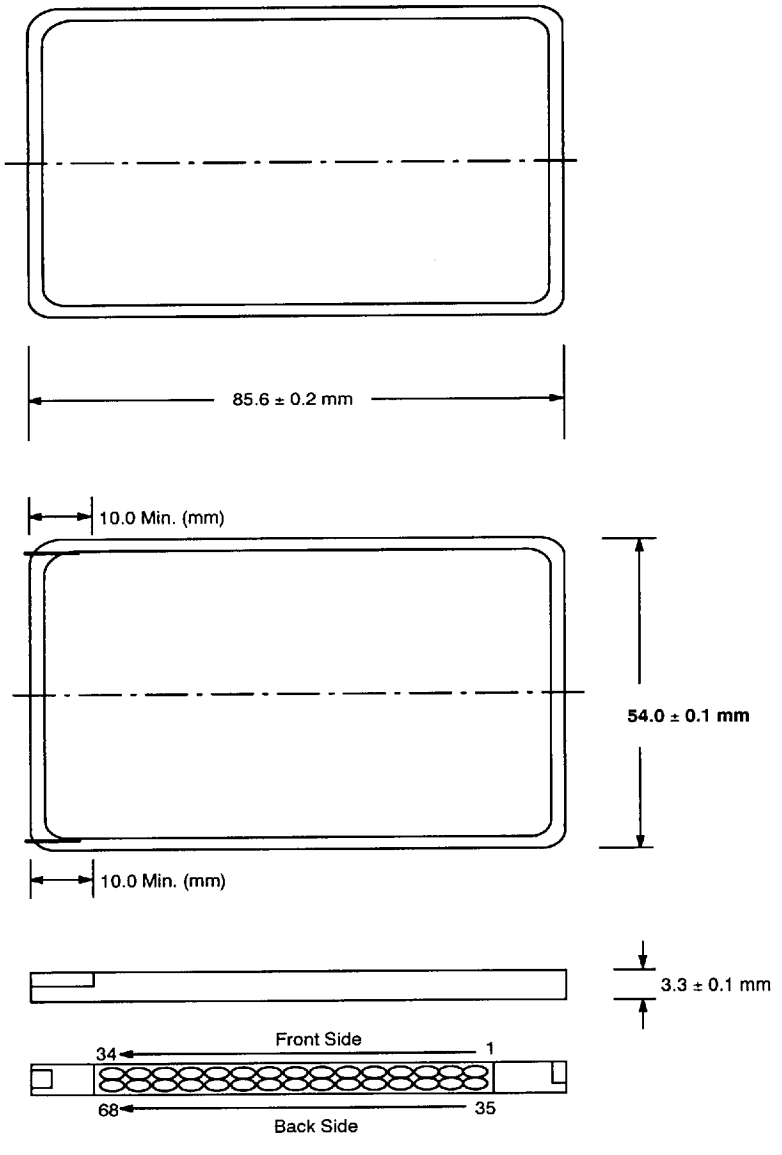
The PCMCIA standard socket provides for proper power up and power down sequencing via different pin lengths to ensure that hot insertion and removal of the PC card will not result in card damage or data loss.

AMD's Flash memory devices are designed to protect against accidental programming or erasure caused by spurious system signals that might exist during hot insertion, hot removal, or power transitions. The AMD PC card will power-up into a READ mode and the card will function as a read only memory as long as V_{pp} is less than V_{cc} +2V. Erasing of the memory segments can be accomplished only by writing the proper Erase command to the card twice along with the proper Chip Enable, Output Enable and Write Enable control signals.

System Power Supply Decoupling

The AMD Flash memory card has a 0.1 μF decoupling capacitor between the V_{cc} and the GND pins, and between the V_{pp} and the GND pins. It is recommended the system side also have a 4.7 μF capacitor between the V_{cc} and the GND pins, and between the V_{pp} and the GND pi ns.

PHYSICAL DIMENSIONS
Type 1 PC Card



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