SRAM

256K x 8 SRAM

OUTPUT ENABLE,
EVOLUTIONARY PINOUT

AVAILABLE AS MILITARY SPECIFICATION
- MIL STD-883

FEATURES

- High Speed: 20, 25, 35ns
- High-performance, low power, CMOS
- Fast OE\ access times: 8, 10, 12ns
- Low Power with 2V Data Retention
- Fully Static, No Clocks
- Single +5V ±10% power supply
- Easy memory expansion with CE\ and OE\ options
- All inputs and outputs are TTL-compatible

OPTIONS MARKING

- **Timing**

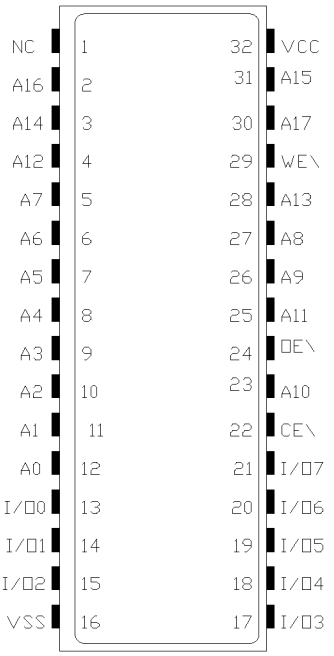
20ns access	-20
25ns access	-25
35ns access	-35
45ns access	-45

- **Packages**

Ceramic Dip (600 mil)	CW	No. 112

- 2V data retention/ low power

PIN ASSIGNMENT (Top View)
32-Pin DIP



GENERAL DESCRIPTION

The AS5C2008 is organized as 262,144 x 8 bit wide. For flexibility in high-speed memory applications, ASI offers chip enable (CE\) and output enable (OE\) capabilities. These features can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable (WE\) and CE\ inputs are both LOW. Reading is accomplished when WE\ remains HIGH and CE\ and OE\ go LOW. The device offers a reduced power standby mode when disabled, by lowering VCC to 2V and maintaining CE\ = 2V. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss
Vcc .....-.5V to +7.0V
Storage Temperature .....-55°C to +150°C
Short Circuit Output Current (per I/O).....20mA
Voltage on any Pin Relative to Vss.....-.5V to Vcc+1 V
Junction Temperature**.....+150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
** Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-55°C ≤ T A ≤ 125°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+.3	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	V_{IN}=V_{SS} to V_{CC}, VCC=5.5V	I_{LI}		10	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}		10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

			MAX					
DESCRIPTION	CONDITIONS	SYMBOL	-20	-25	-35	-45	UNITS	NOTES
Power Supply Current: Operating	CE\ ≤ V_{IL}; V_{CC} = MAX f =5MHz outputs open	I_{CC}	150	150	150	150	mA	3
Power Supply Current: Standby	CE\ ≥ V_{IH}; V_{CC} = MAX f =5MHz outputs open	I_{SB}	50	50	50	50	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Output Capacitance	T_A = 25°C; 1 = MHz	C_I	8	pF	4
Input Capacitance	V_{CC} = 5V	C_O	10	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 5) (-55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ±10%)

DESCRIPTION		-20		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle Time	t_{RC}	20		25		35		45		ns	
Address access time	t_{AA}		20		25		35		45	ns	
Chip Enable access time	t_{ACE}		20		25		35		45	ns	
Output hold from address change	t_{OH}	3		3		3		3		ns	
Chip Enable to output in Low-Z	t_{LZCE}	3		3		3		3		ns	4,6,7
Chip disable to output in High-Z	t_{HZCE}		15		17		20		30	ns	4,6,7
Output Enable access time	t_{AOE}		10		12		15		15	ns	
Output Enable to output in Low-Z	t_{LZOE}	0		0		0		0		ns	4,6,7
Output disable to output in High-Z	t_{HZOE}		12		15		20		20	ns	4,6,7
WRITE Cycle											
WRITE cycle time	t_{WC}	20		25		35		45		ns	
Chip Enable to end of write	t_{CW}	16		20		25		30		ns	
Address valid to end of write	t_{AW}	16		20		25		30		ns	
Address setup time	t_{AS}	0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		ns	
WRITE pulse width	t_{WP1}	16		20		25		30		ns	
Data setup time	t_{DS}	12		15		20		20		ns	
Data hold time	t_{DH}	0		0		0		0		ns	
Write disable to output in Low-Z	t_{LZWE}	3		3		3		3		ns	4,6,7
Write Enable to output in High-Z	t_{HZWE}		12		15		20		20	ns	4,6,7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

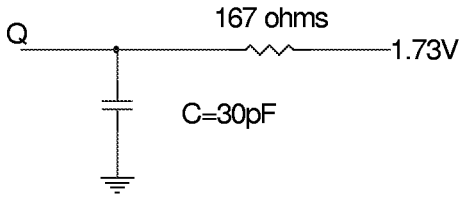


Fig. 1 Output Load Equivalent

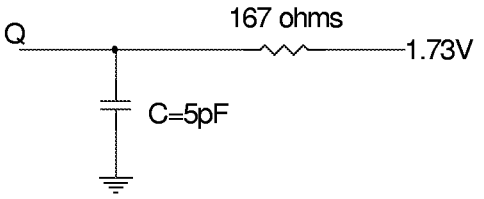


Fig. 2 Output Load Equivalent

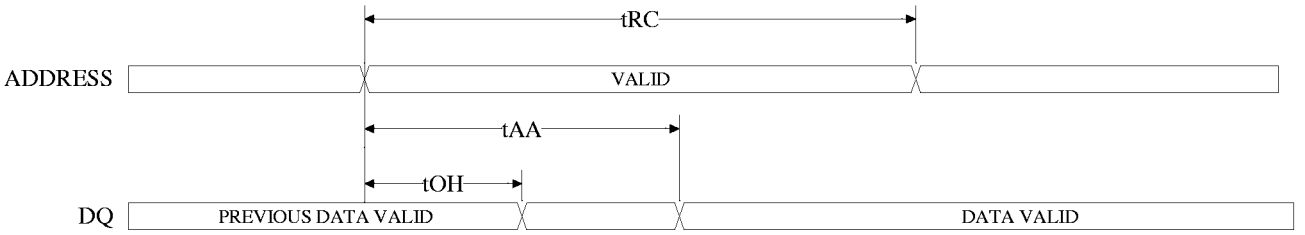
NOTES

1. All voltages referenced to V_{SS} (GND).
2. -2V for pulse width < 20ns
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is guaranteed but not tested.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^tLZCE, ^tLZWE, ^tLZOE, ^tHZCE, ^tHZOE and ^tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ^tHZCE is less than ^tLZCE, and ^tHZWE is less than ^tLZWE.
8. WE\ is HIGH for READ cycle.
9. Device is continuously selected. Chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^tRC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Output enable (OE\) is inactive (HIGH).
14. Output enable (OE\) is active (LOW).
15. ASI does not warrant functionality nor reliability of any product in which the junction temperature exceeds 150°C. Care should be taken to limit power to acceptable levels.

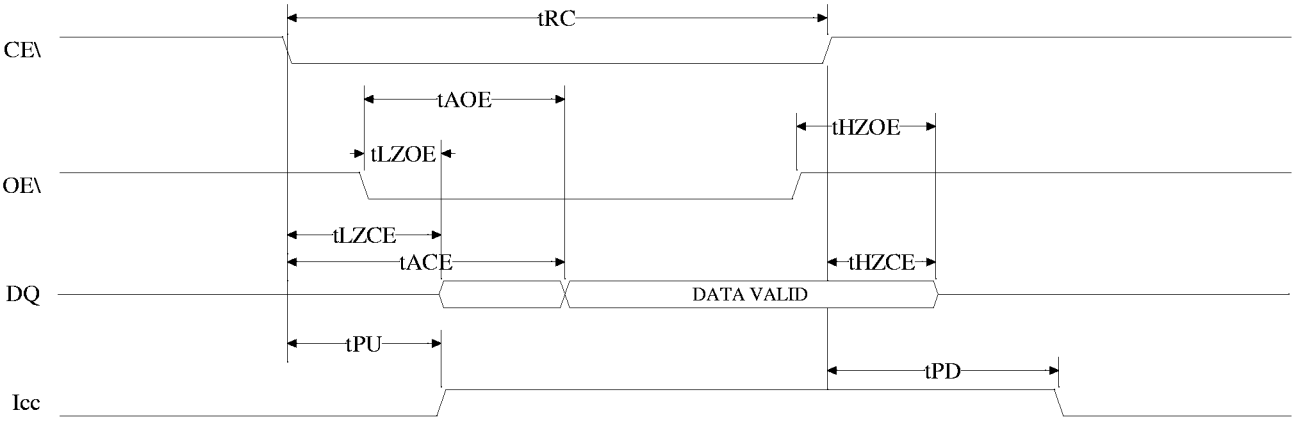
DATA RETENTION ELECTRICAL CHARACTERISTICS

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS
VCC for Retention Data	CE\ ≥V_{CC}-0.2V	V_{DR}	2.0	5.5	V
Data Retention Current	VCC = 3V	I_{CCDR1}		4.0	mA

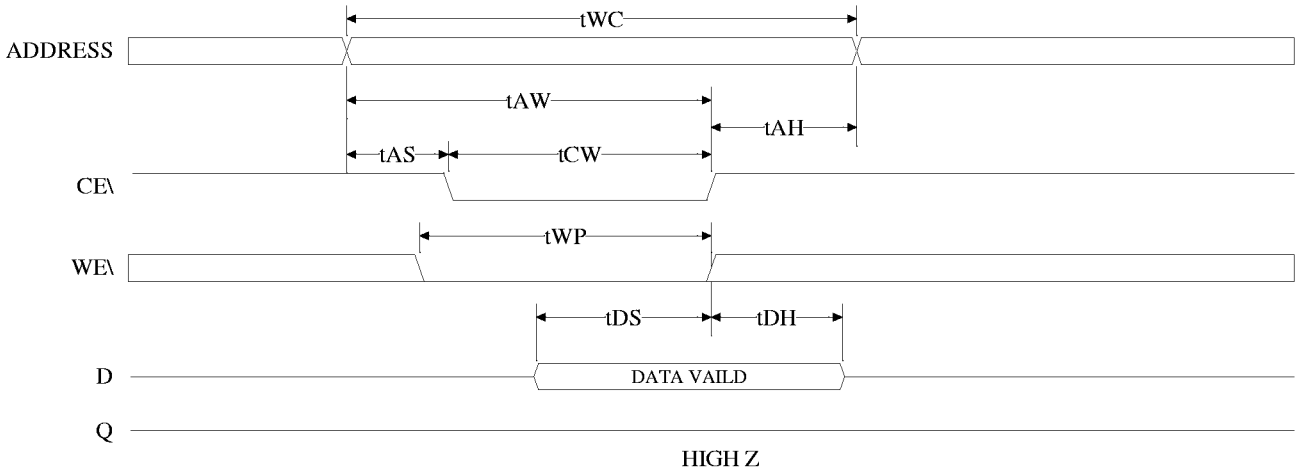
READ CYCLE NO. 1 [8,9]
(Write Enabled Controlled)



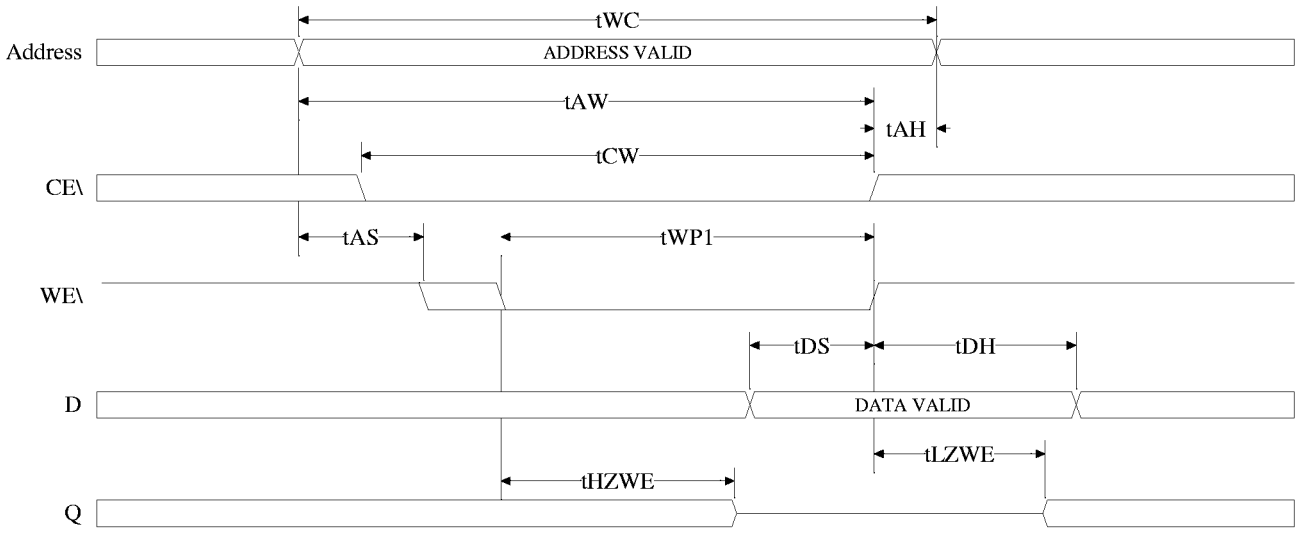
READ CYCLE NO. 2 [7,8,10]
(Write Enabled Controlled)



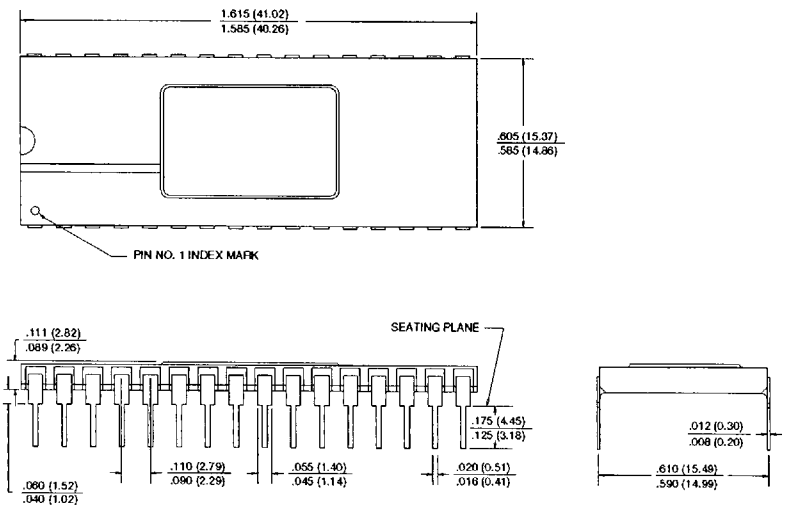
WRITE CYCLE NO. 1 [12]
(Chip Enabled Controlled)



WRITE CYCLE NO. 2 [12, 13]
(Write Enabled Controlled)



PACKAGE NO. 112
32 CDIP (600 mils)



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