

CYPRESS
SEMICONDUCTOR

CYM1821

16K x 32 Static RAM Module

Features

- High-density 512-Kbit SRAM module
- High-speed CMOS SRAMs
 - Access time of 12 ns
- Low active power
 - 4W (max.)
- SMD technology
- TTL-compatible inputs and outputs
- Low profile
 - Max. height of .50 in.
- Small PCB footprint
 - 1.0 sq. in.
- JEDEC-compatible pinout
- 2V data retention (L version)
- SIMM version socket-compatible with CYM1831 and CYM1841

Functional Description

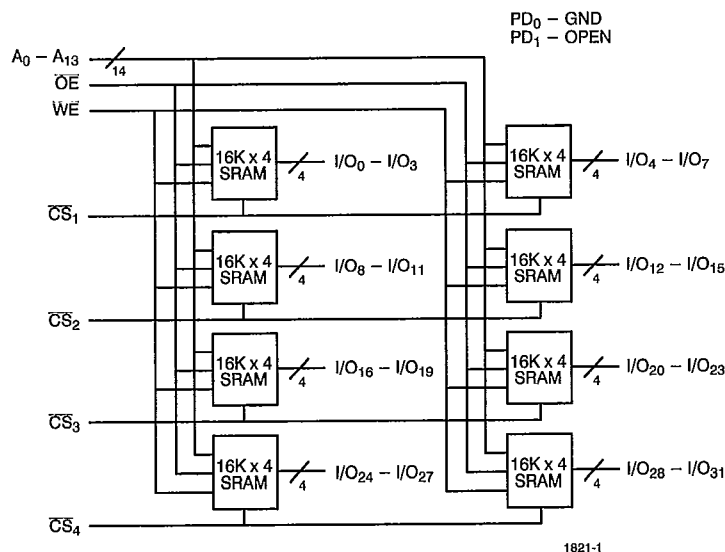
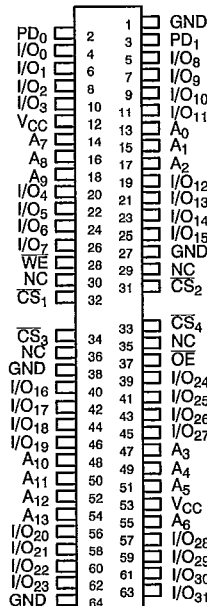
The CYM1821 is a high-performance 512-Kbit static RAM module organized as 16K words by 32 bits. This module is constructed from eight 16K x 4 SRAM SOJ packages mounted on an epoxy laminate board with pins. Four chip selects ($\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$, and $\overline{CS}_4$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

Writing to each byte is accomplished when the appropriate chip selects ($\overline{CS}_N$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O_X) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the chip selects ($\overline{CS}_N$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O_X).

The data input/output pins stay in the high-impedance state when write enable ($\overline{WE}$) is LOW, or the appropriate chip selects are HIGH.

Two pins (PD_0 and PD_1) are used to identify module memory density in applications where alternate versions of the JEDEC standard modules can be interchanged.

Logic Block Diagram**Pin Configuration**ZIP
Top View**Selection Guide**

	1821-12	1821-15	1821-20	1821-25	1821-35	1821-45
Maximum Access Time (ns)	12	15	20	25	35	45
Maximum Operating Current (mA)	960	960	720	720	720	720
Maximum Standby Current (mA)	450	450	160	160	160	160

**Maximum Ratings**

(Above which the useful life may be impaired.)

Storage Temperature - 65°C to +150°C
 Ambient Temperature with
 Power Applied - 10°C to +85°C
 Supply Voltage to Ground Potential - 0.5V to +7.0V
 DC Voltage Applied to Outputs
 in High Z State - 0.5V to +7.0V
 DC Input Voltage - 0.5V to +7.0V
 Output Current into Outputs (LOW) 20 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	1821-12 1821-15		1821-20 1821-25 1821-35 1821-45		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage		- 0.5	0.8	- 0.5	0.8	V
I _{Ix}	Input Load Current	GND ≤ V _I ≤ V _{CC}	- 20	+ 20	- 20	+ 20	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	- 20	+ 20	- 20	+ 20	μA
I _{OS}	Output Short Circuit Current ^[1]	V _{CC} = Max., V _{OUT} = GND		- 350		- 350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, CS ≤ V _{IL}		960		720	mA
I _{SB1}	Automatic CS Power-Down Current ^[2]	Max. V _{CC} , CS ≥ V _{IH} , Min. Duty Cycle = 100%		450		160	mA
I _{SB2}	Automatic CS Power-Down Current ^[2]	Max. V _{CC} , CS _N ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		160		160	mA

Capacitance^[3]

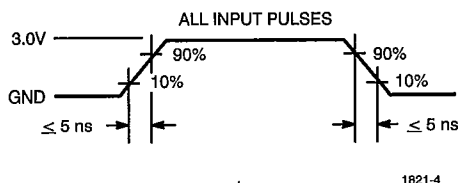
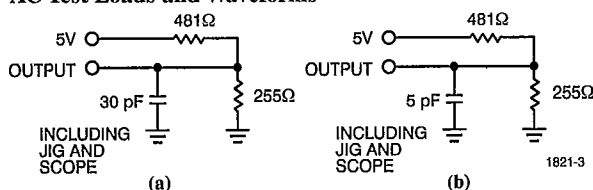
Parameter	Description	Test Conditions	Max.	Unit
C _{INA}	Input Capacitance (ADDR, OE, WE)	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	70	pF
C _{INB}	Input Capacitance (CS)		35	pF
C _{OUT}	Output Capacitance		20	pF

Notes:

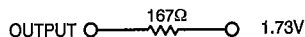
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V_{CC} on the CS input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
- Tested on a sample basis.



AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

Switching Characteristics Over the Operating Range^[4]

Parameter		Description	1821-12		1821-15		1821-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE									
t _{RC}	Read Cycle Time	12		15		20		ns	
t _{AA}	Address to Data Valid		12		15		20	ns	
t _{OHA}	Data Hold from Address Change	2		2		3		ns	
t _{ACS}	$\overline{CS}$ LOW to Data Valid		12		15		20	ns	
t _{DOE}	$\overline{OE}$ LOW to Data Valid		10		10		10	ns	
t _{LZOE}	$\overline{OE}$ LOW to Low Z	2		2		3		ns	
t _{HZOE}	$\overline{OE}$ HIGH to High Z		8		8		8	ns	
t _{LZCS}	$\overline{CS}$ LOW to Low Z ^[5]	3		3		5		ns	
t _{HZCS}	$\overline{CS}$ HIGH to High Z ^[5, 6]		8		8		8	ns	
t _{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns	
t _{PD}	$\overline{CS}$ HIGH to Power-Down		12		15		20	ns	
WRITE CYCLE ^[7]									
t _{WC}	Write Cycle Time	12		15		20		ns	
t _{SCS}	$\overline{CS}$ LOW to Write End	10		12		15		ns	
t _{AW}	Address Set-Up to Write End	10		12		15		ns	
t _{HA}	Address Hold from Write End	2		2		2		ns	
t _{SA}	Address Set-Up to Write Start	0		0		2		ns	
t _{PWE}	$\overline{WE}$ Pulse Width	10		12		15		ns	
t _{SD}	Data Set-Up to Write End	10		10		10		ns	
t _{HD}	Data Hold from Write End	2		2		2		ns	
t _{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		3		ns	
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[6]	0	7	0	7	0	7	ns	

Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{LZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
- t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ± 500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range (continued)^[4]

Parameter	Description	1821–25		1821–35		1821–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	25		35		45		ns
t _{AA}	Address to Data Valid		25		35		45	ns
t _{OHA}	Data Hold from Address Change	3		3		3		ns
t _{ACS}	$\overline{CS}$ LOW to Data Valid		25		35		45	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		15		25		30	ns
t _{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		ns
t _{HZOE}	$\overline{OE}$ HIGH to High Z		15		20		20	ns
t _{LZCS}	$\overline{CS}$ LOW to Low Z ^[5]	5		10		10		ns
t _{HZCS}	$\overline{CS}$ HIGH to High Z ^[5, 6]		10		15		20	ns
t _{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t _{PD}	$\overline{CS}$ HIGH to Power-Down		25		35		45	ns
WRITE CYCLE ^[7]								
t _{WC}	Write Cycle Time	25		35		45		ns
t _{SCS}	$\overline{CS}$ LOW to Write End	20		25		35		ns
t _{AW}	Address Set-Up to Write End	20		25		35		ns
t _{HA}	Address Hold from Write End	2		2		2		ns
t _{SA}	Address Set-Up to Write Start	2		2		2		ns
t _{PWE}	WE Pulse Width	20		25		30		ns
t _{SD}	Data Set-Up to Write End	13		15		20		ns
t _{HD}	Data Hold from Write End	2		2		2		ns
t _{LZWE}	WE HIGH to Low Z	3		5		5		ns
t _{HZWE}	WE LOW to High Z ^[6]	0	7	0	10	0	15	ns

Data Retention Characteristics (L Version Only)

Parameter	Description	Test Conditions	CYM1821		Unit
			Min.	Max.	
V _{DR}	V _{CC} for Retention Data	V _{CC} = 2.0V, CS ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	2		V
I _{CCDR}	Data Retention Current			8	mA
t _{CDR} ^[8]	Chip Deselect to Data Retention Time		0		ns
t _R ^[8]	Operation Recovery Time		t _{RC} ^[9]		ns
I _{IL} ^[8]	Input Leakage Current			10	μA

Notes:

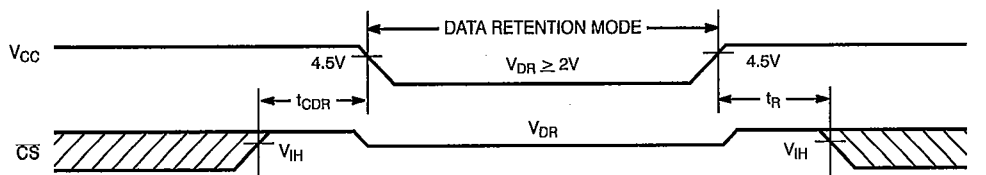
8. Guaranteed, not tested.

9. t_{RC} = Read Cycle Time.



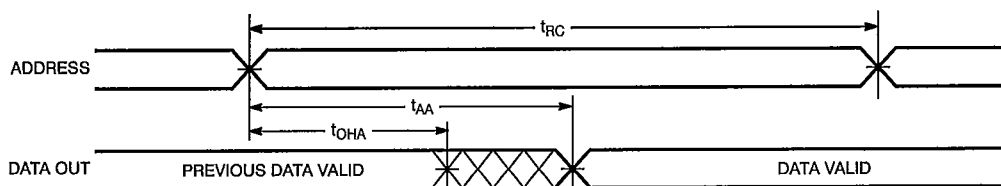
CYM1821

Data Retention Waveform

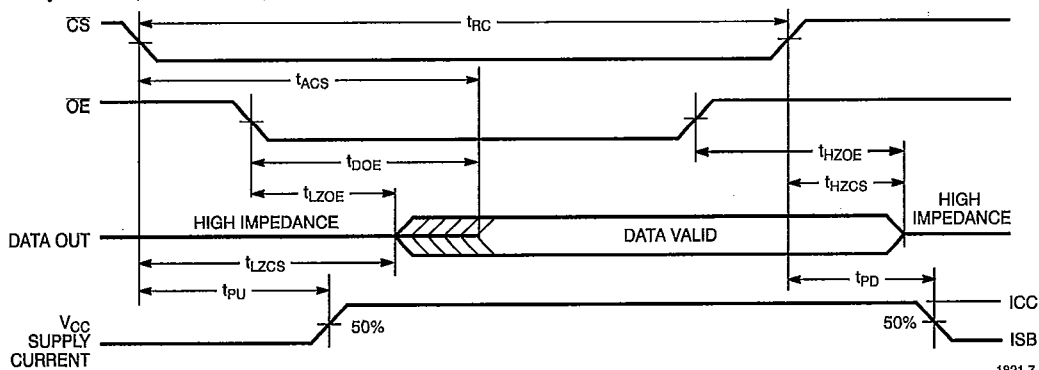


1821-5

Switching Waveforms

Read Cycle No. 1^[10, 11]

1821-6

Read Cycle No. 2 ($\overline{WE}$ Controlled)^[10, 12]

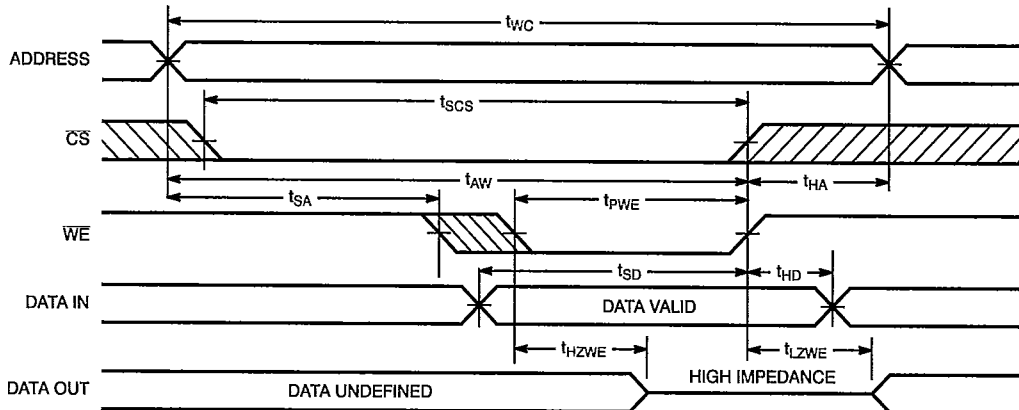
1821-7

Notes:

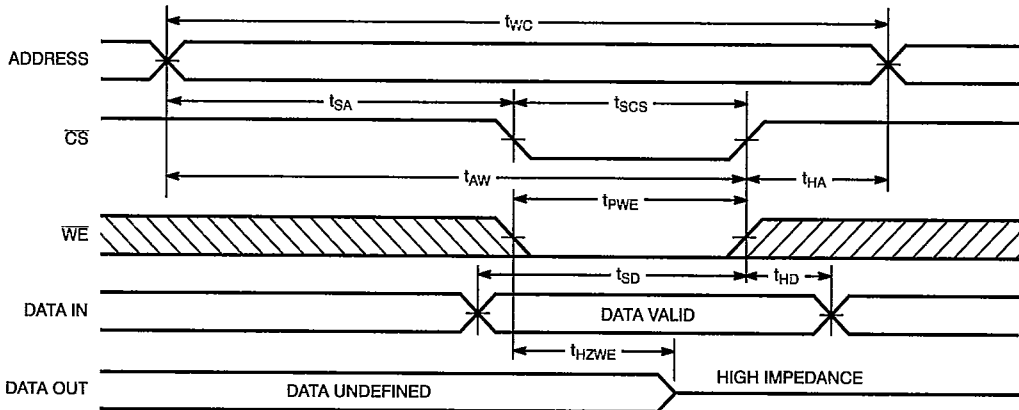
10. $\overline{WE}$ is HIGH for read cycle.11. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.12. Address valid prior to or coincident with $\overline{CS}$ transition LOW.



Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{WE}$ Controlled)^[7]

1621-8

Write Cycle No. 2 ($\overline{CS}$ Controlled)^[7, 13]

1621-9

Note:

13. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

CYPRESS
SEMICONDUCTOR

CYM1821

Truth Table

CS _N	WE	OE	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
12	CYM1821PM-12C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1821PZ-12C	PZ01	64-Pin Plastic ZIP Module	
15	CYM1821PM-15C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1821PZ-15C	PZ01	64-Pin Plastic ZIP Module	
20	CYM1821PM-20C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1821LPM-20C	PM01	64-Pin Plastic SIMM Module	
	CYM1821PZ-20C	PZ01	64-Pin Plastic ZIP Module	
	CYM1821LPZ-20C	PZ01	64-Pin Plastic ZIP Module	
25	CYM1821PM-25C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1821LPM-25C	PM01	64-Pin Plastic SIMM Module	
	CYM1821PZ-25C	PZ01	64-Pin Plastic ZIP Module	
	CYM1821LPZ-25C	PZ01	64-Pin Plastic ZIP Module	
35	CYM1821PM-35C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1821LPM-35C	PM01	64-Pin Plastic SIMM Module	
	CYM1821PZ-35C	PZ01	64-Pin Plastic ZIP Module	
	CYM1821LPZ-35C	PZ01	64-Pin Plastic ZIP Module	
45	CYM1821PM-45C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1821LPM-45C	PM01	64-Pin Plastic SIMM Module	
	CYM1821PZ-45C	PZ01	64-Pin Plastic ZIP Module	
	CYM1821LPZ-45C	PZ01	64-Pin Plastic ZIP Module	

Document #: 38-M-00015-D