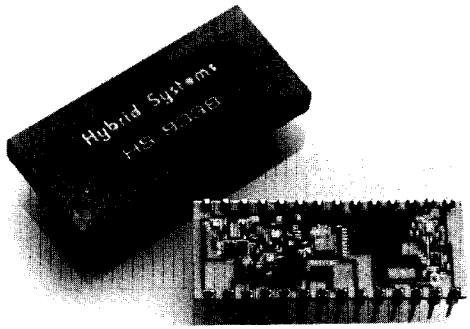
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS9338

COMPLETE μP COMPATIBLE 12-BIT DAC

FEATURES

- Output ranges: 0 to +10V, ±10V,
- Coding: binary; offset binary
- Linearity: ±0.01%
- Settling time: 2.5μS
- μP compatible
- 28-pin package
- CMOS, TTL compatible
- Double buffered inputs



DESCRIPTION

HS9338 is a μP compatible, complete 12-bit double buffered digital-to-analog converter. To enhance application flexibility, the data input registers have been configured as 3 independent, 4-bit bytes. This enables the user to directly interface to 4, 8, and 12-bit data buses. HS9338 comes complete with interface control logic. The three separate byte enable inputs latch data from the bus into the appropriate primary data latches. The LDAC input transfers data from the primary latches to the DAC register. In addition to these input functions are two chip select inputs and a read/write input allowing direct memory-map configurations. All input controls are static to allow hardwired configurations.

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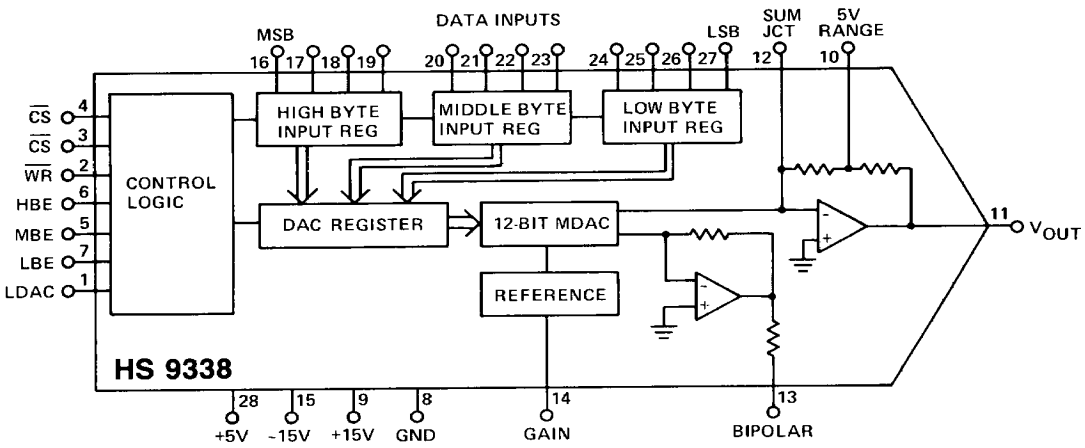
FUNCTIONAL DIAGRAM



SPECIFICTIONS

(Typical @25°C unless otherwise noted. Power supply voltages: +15V, −15V, +5V, (±5%))

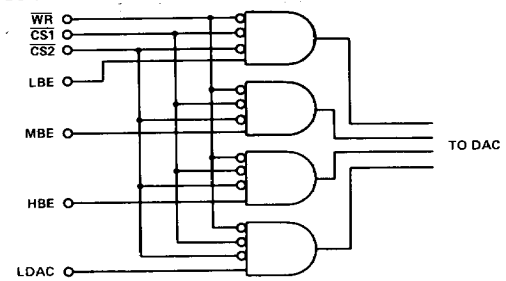
MODEL	HS 9338-2	HS 9338-0
DIGITAL INPUT		
Resolution	12 Bit	*
Unipolar Code	Binary	*
Bipolar Code	Offset Binary	*
Logic Compatibility[1]	CMOS, TTL	*
Control Logic Inputs		
I_{IH} @V_{IH} = 2.4V	20μA	*
I_{IL} @V_{IL} = 0.4V	−0.36mA	*
Data Input Current[5]	±1μA	*
ANALOG OUTPUT		
Scale Factor Accuracy[2]	±0.1% FSR	*
Initial Offset[2]		
Bipolar	±0.1% FSR max	*
Unipolar	±0.05% FSR max	*
Voltage Range[2]		
Bipolar	±10V,	*
Unipolar	0 to +10V	*
STATIC PERFORMANCE		
Integral Linearity[3]	±0.015% FSR max	±0.050% FSR max
Differential Linearity	±0.024 FSR max	±0.097% FSR max
Monotonicity	12 Bits	10 Bits
DYNAMIC PERFORMANCE		
Full Scale Transition		*
Settling Time	5μS max	*
	2.5μS max	
Full Scale Transition		*
Slew Rate	10V/μS min	
Delay to Analog Output		*
From Bits Input[4]	220nS	*
From LDAC	220nS	*
From CS[4] or WE[4]	225nS	
STABILITY		
Scale Factor	20ppm FSR	*
Integral Linearity	1ppm FSR max	*
Differential Linearity	1ppm FSR max	*
Offset Drift		*
Bipolar	10ppm/°C	*
Unipolar	5ppm/°C	*
Monotonicity Temperature Range	0°C to +70°C	
±15V POWER SUPPLY		
+15V Supply Current	12mA	*
−15V Supply Current	10mA	*
PSRR	0.005%/%	*
+5V POWER SUPPLY		
+5V Supply Current	24mA	*
TEMPERATURE RANGE		
Operating	−55°C to +125°C	*
Storage	−65°C to +155°C	*
MECHANICAL		
Case Style	Plastic	*

NOTES: 1. Control inputs are TTL and 5V CMOS only; data inputs are fully CMOS and TTL compatible. 2. See APPLICATION NOTES for adjustment procedures. 3. Specified as "Best Straight Line". 4. Operating the unit with the DAC Register transparent may result in output "glitches" due to logic skewing with the unit. 5. Digital Input Voltage must not exceed supply voltage or go below −0.5V. "0" 0.8V, 2.4V "1" V_{DD}.

*Same as HS 9338-2

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below −0.5 volts.

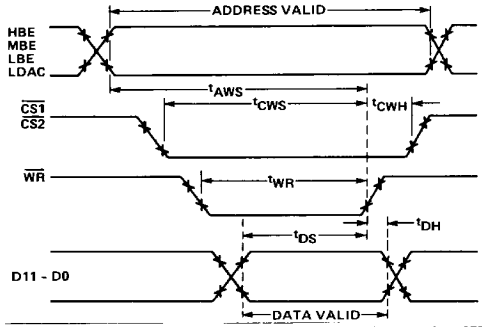
CONTROL LOGIC FUNCTIONAL DIAGRAM



TRUTH TABLE

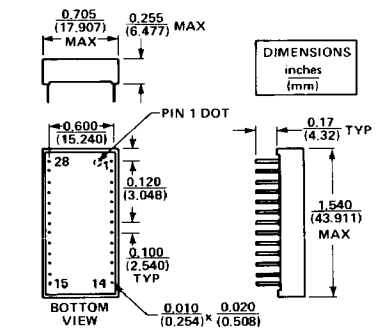
HS 9338 CONTROL INPUTS							HS 9338 OPERATION
$\overline{WR}$	$\overline{CS1}$	$\overline{CS2}$	LBE	MBE	HBE	LDAC	
1 X X	X 1 X	X X 1	X	X	X	X	Device not selected Output reflects previously loaded data
0	0	0	1	0	0	0	Write data into low byte data register
0	0	0	0	1	0	0	Write data into middle byte data register
0	0	0	0	0	1	0	Write data into high byte data register
0	0	0	0	0	0	1	Load DAC register with data in low byte middle byte and high byte data registers
0	0	0	1	1	1	0	Write data simultaneous into all data registers
0	0	0	1	1	1	1	Write data directly into DAC register

TIMING DIAGRAM



t_{DS} : Data setup time, 250 nsec
t_{DH} : Data hold time, 20 nsec
t_{WR} : Write pulse width, 350 nsec
t_{CWS} : Chip select to write setup time, 375 nsec
t_{CWH} : Chip select to write hold time, 0 nsec
t_{AWS} : Address to write setup time, 250 nsec

PACKAGE OUTLINE



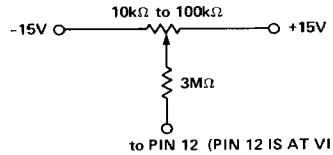
PIN DIAGRAM

PIN	FUNCTION
1	LDAC, LOADS DAC REGISTER AND CHANGES OUTPUT
2	$\overline{WR}$, WRITE INPUT, ACTIVATES ALL CONTROLS
3	$\overline{CS2}$, CHIP SELECT INPUT 2
4	$\overline{CS1}$, CHIP SELECT INPUT 1
5	MBE, MIDDLE BYTE ENABLE, D4 TO D7
6	HBE, HIGH BYTE ENABLE, D8 TO D11
7	LBE, LOW BYTE ENABLE, D0 TO D3
8	GND, GROUND, ANALOG AND DIGITAL GROUND CONNECTED INTERNALLY
9	V_{CC}, +15V SUPPLY
10	RANGE, 5V OUTPUT RANGE INPUT
11	V_{OUT}, DAC VOLTAGE OUTPUT
12	SUMJCT, SUMMING JUNCTION OF OUTPUT OPAMP
13	BIPOLAR, CONNECTED TO SUMJCT FOR BIPOLAR OUTPUT RANGE
14	GAIN, INPUT TO ADJUST FULL SCALE OUTPUT VOLTAGE
15	V_{EE}, -15V SUPPLY
16	D11, DATA INPUT, WEIGHT 2^{-1}, MSB
17	D10, DATA INPUT, WEIGHT 2^{-2}
18	D9, DATA INPUT, WEIGHT 2^{-3}
19	D8, DATA INPUT, WEIGHT 2^{-4}
20	D7, DATA INPUT, WEIGHT 2^{-5}
21	D6, DATA INPUT, WEIGHT 2^{-6}
22	D5, DATA INPUT, WEIGHT 2^{-7}
23	D4, DATA INPUT, WEIGHT 2^{-8}
24	D3, DATA INPUT, WEIGHT 2^{-9}
25	D2, DATA INPUT, WEIGHT 2^{-10}
26	D1, DATA INPUT, WEIGHT 2^{-11}
27	D0, DATA INPUT, WEIGHT 2^{-12}, LSB
28	V_{DD}, +5V SUPPLY, CONTROL LOGIC

OUTPUT CONNECTIONS

RANGE	OUTPUT	CONNECT PIN 12	CONNECT PIN 10	CONNECT PIN 13
0 to +10V	PIN 11	OPEN	OPEN	OPEN
−10V to +10V	PIN 11	PIN 13	OPEN	PIN 12
−5V to +5V	PIN 11	PIN 13	PIN 12	PIN 12

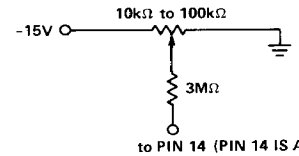
OUTPUT OFFSET ADJUST



RANGE: ±0.25% F.S.

Adjust for V_{out} = 0.000 Volt at input code 00 . . . 0 for unipolar operation or at input code 10 . . . 0 for bipolar operation.

OUTPUT GAIN ADJUST

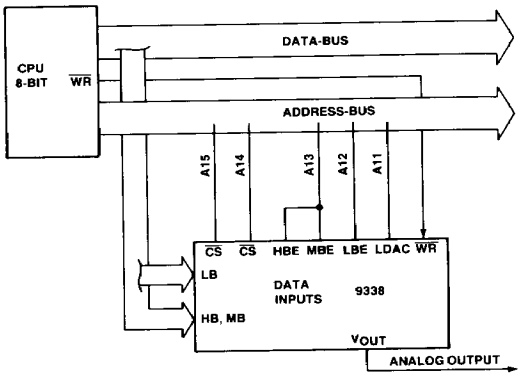


RANGE: ±0.5%

Adjust for V_{out} = +9.9976 Volt at input code 11 . . . 1 (4.9988 Volt on 0-5V range) or for V_{out} = -10.000 Volt at input code 00 . . . 0 (-5.0000 Volt on ±5V range) if set up for bipolar operation.

APPLICATIONS INFORMATION

INTERFACING THE HS9338 TO AN 8-BIT PROCESSOR USING NO EXTERNAL COMPONENTS

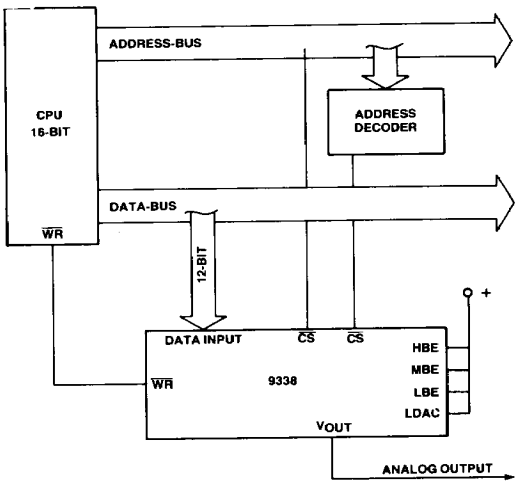


This mode of operation requires 13k bytes of unused addresses. No additional address decoder is necessary. The two chip-select input together with the byte-enable and load-DAC inputs are used to control all functions of the DAC. Through selecting the address-lines the user can vary the addresses used to control the DAC. In the above figure the control signals have the following address-configurations (hex):

HBE, MBE	2000
LBE	1000
LDAC	0800

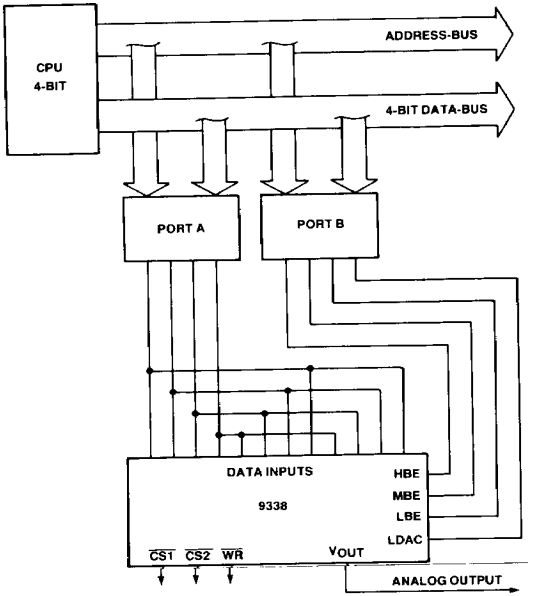
The LDAC input should not be tied together to the LBE input to ensure correct data transfer between the DAC registers.

INTERFACING THE HS9338 TO A 16-BIT MICROPROCESSOR



Interfacing the HS9338 to a 16-Bit microprocessor is quite easy, because no multiplexing of the data inputs is necessary. An address decoder and the second chip-select input is used to select the DAC.

INTERFACING THE HS9338 to a 4-BIT MICROPROCESSOR USING 4-BIT I/O-PORTS



This figure shows how to operate the HS 9338 with two 4-Bit ports. The chip-selects are tied to ground allowing continuous operation; they can be used for operating more DAC's at the same port. In the first step data should appear at the port A outputs; in the second step the control flags should appear on port B.

PRODUCT SCREENING AND QUALIFICATION

Products cataloged as Class B are fully screened in accordance with Method 5004 of MIL-STD-883, Class B.

Hybrid Systems is equipped to perform qualification and quality conformance testing of its products to the Class B requirements of MIL-STD-883, Method 5005. Processing to applicable Class S requirements is available where the higher confidence level is required.

ORDERING INFORMATION

MODEL	DESCRIPTION
HS 9338-2	µP DAC, 0.01% Linearity
HS 9338-0	µP DAC, 0.05% Linearity

Specifications subject to change without notice.