Contents

1.Description

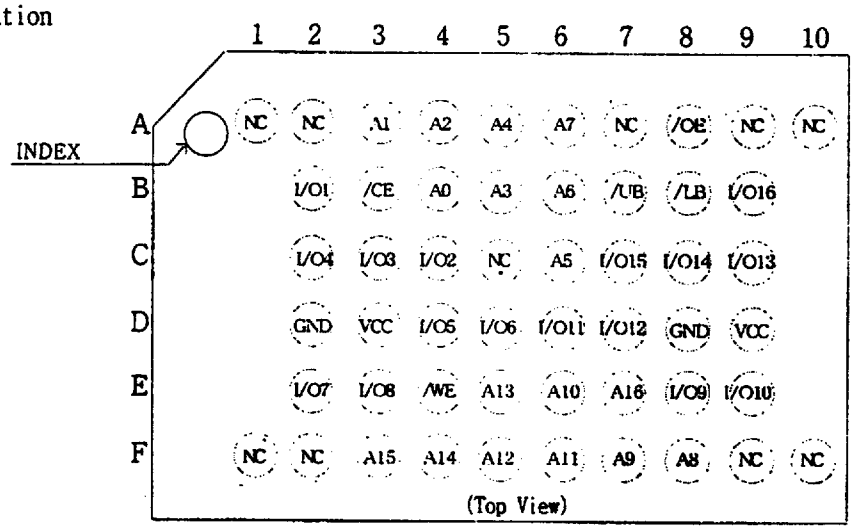
The LH51V2016JY-85LL is a static RAM organized as 131,072x16 bit with provides low-power standby mode.
It is fabricated using silicon-gate CMOS process technology.

Features

○Access Time	....	85 ns (Max.)
○Operating current	....	45 mA (Max.)
	....	5 mA (Max. t_{RC}. t_{WC}=1 μs)
○Standby current	....	45 μA (Max.)
○Data retention current	....	1.0 μA (Max. V_{CCDR}=3V,Ta=25℃)
○Single power supply	....	2.7V to 3.6V
○Operating temperature	....	−25℃ to +85℃

○Fully static operation
○Three-state output
○Not designed or rated as radiation hardened
○52 pin CSP (FBGA052-P-0610) plastic package
○P-type bulk silicon

2.Pin Configuration



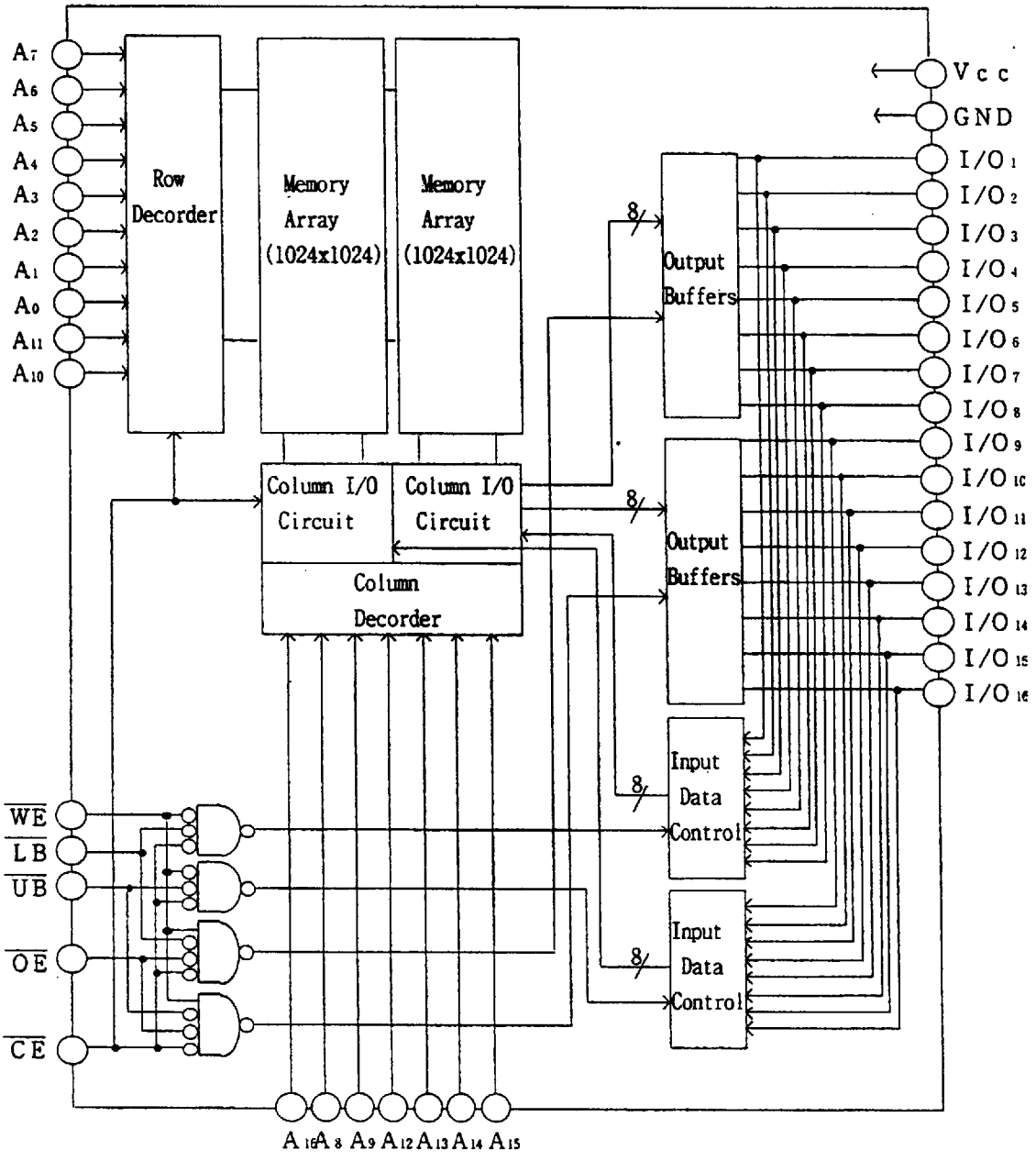
Pin Name	Function
A_0 to A_{16}	Address inputs
$\overline{CE}$	Chip enable
$\overline{LB}$	Byte enable (I/O_1 to I/O_8)
$\overline{UB}$	Byte enable (I/O_9 to I/O_{16})
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
I/O_1 to I/O_{16}	Data inputs/outputs
Vcc	Power supply
GND	Ground
NC	Non connection

3.Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O1 to I/O8	I/O9 to I/O16	Supply current
H	*	*	*	*	Standby	High impedance	High impedance	Standby (ISB)
L	L	H	L	L	Read	Data output	Data output	Active (Icc)
			L	H	Read	Data output	High impedance	Active (Icc)
			H	L	Read	High impedance	Data output	Active (Icc)
L	*	L	L	L	Write	Data input	Data input	Active (Icc)
			L	H	Write	Data input	High impedance	Active (Icc)
			H	L	Write	High impedance	Data input	Active (Icc)
L	H	H	*	*	Output disable	High impedance	High impedance	Active (Icc)
L	*	*	H	H	Output disable	High impedance	High impedance	Active (Icc)

(*=Don't Care, L=Low, H=High)

4.Block Diagram



5. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage(*1)	Vcc	−0.3 to +4.6	V
Input voltage(*1)	V_{IN}	−0.3(*2) to Vcc+0.3	V
Operating temperature	T_{opr}	−25 to +85	℃
Storage temperature	T_{stg}	−65 to +150	℃

Note) *1. The maximum applicable voltage on any pin with respect to GND.
*2. Undershoot of −3.0V is allowed width of pulse bellow 30ns.

6. Recommended DC Operating Conditions

(Ta= −25℃ to +85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	2.7	3.0	3.6	V
Input voltage	V_{IH}	2.2		Vcc+0.3	V
	V_{IL}	−0.3 (*3)		0.8	V

Note) *3. Undershoot of −3.0V is allowed width of pulse below 30ns.

7. DC Electrical Characteristics

(Ta= −25℃ to +85℃, Vcc= 2.7V to 3.6V)

Parameter	Symbol	Conditions		Min.	Typ. (*4)	Max.	Unit
Input leakage current	I_{LI}	V_{IN}=0V to Vcc		−1.0		1.0	μA
Output leakage current	I_{LO}	$\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} $V_{I/O}$=0V to Vcc		−1.0		1.0	μA
Operating supply current	I_{CC1}	$\overline{CE}$=V_{IL}, V_{IN}=V_{IL} or V_{IH} $I_{I/O}$=0mA	t_{CYCLE} =Min			45	mA
	I_{CC2}	$\overline{CE}$≦0.2V, V_{IN}≦0.2V or Vcc−0.2V $I_{I/O}$=0mA	t_{CYCLE} =1.0μS			5	mA
Standby current	I_{SB}	$\overline{CE}$≧Vcc−0.2V			0.6	45	μA
	I_{SB1}	$\overline{CE}$=V_{IH}				3	mA
Output voltage	V_{OL}	I_{OL}= 2.0mA				0.4	V
	V_{OH}	I_{OH}=−1.0mA		2.4			V

Note) *4. Typical values at Vcc=3V, Ta=25℃.

8. AC Electrical Characteristics

AC Test Conditions

Input pulse level	0.6V to 2.4V
Input rise and fall time	5 ns
Input and Output timing Ref. level	1.4V
Output load	1TTL+CL (30pF) (*5)

Note) *5. Including scope and jig capacitance.

Read cycle (Ta=−25℃ to +85℃, Vcc=2.7V to 3.6V)

Parameter	Symbol	Min.	Max.	Unit	
Read cycle time	t_{RC}	85		ns	
Address access time	t_{AA}		85	ns	
Chip enable access time	t_{ACE}		85	ns	
Byte enable access time	t_{BE}		45	ns	
Output enable to output valid	t_{OE}		45	ns	
Output hold from address change	t_{OH}	10		ns	
$\overline{CE}$ Low to output active	t_{LZ}	10		ns	*6
$\overline{OE}$ Low to output active	t_{OLZ}	5		ns	*6
$\overline{LB}$, $\overline{UB}$ Low to output active	t_{BLZ}	5		ns	*6
$\overline{CE}$ High to output in High impedance	t_{HZ}	0	40	ns	*6
$\overline{OE}$ High to output in High impedance	t_{OHZ}	0	35	ns	*6
$\overline{LB}$, $\overline{UB}$ High to output in High impedance	t_{BHZ}	0	35	ns	*6

Write cycle (Ta=−25℃ to +85℃, Vcc=2.7V to 3.6V)

Parameter	Symbol	Min.	Max.	Unit	
Write cycle time	t_{WC}	85		ns	
$\overline{CE}$ Low to end of write	t_{CW}	75		ns	
Address valid to end of write	t_{AW}	75		ns	
Byte enable to end of write	t_{BW}	75		ns	
Address setup time	t_{AS}	0		ns	
Write pulse width	t_{WP}	65		ns	
Write recovery time	t_{WR}	0		ns	
Input data setup time	t_{DW}	35		ns	
Input data hold time	t_{DH}	0		ns	
$\overline{WE}$ High to output active	t_{OW}	5		ns	*6
$\overline{WE}$ Low to output in High impedance	t_{WZ}	0	40	ns	*6

Note) *6. Active output to High impedance and High impedance to output active tests specified for a ±200mV transition from steady state levels into the test load.

9. Data Retention Characteristics

(Ta= −25℃ to +85℃)

Parameter	Symbol	Conditions		Min.	Typ. (*7)	Max.	Unit
Data Retention supply voltage	V_{CCDR}	$\overline{CE} \geq V_{CCDR}-0.2V$		2.0		3.6	V
Data Retention supply current	I_{CCDR}	$V_{CCDR}=3V$	Ta=25℃		0.6	1.0	μA
			Ta=40℃			3.0	μA
		$\overline{CE} \geq V_{CCDR}-0.2V$				35	μA
Chip enable setup time	t_{CDR}			0			ns
Chip enable hold time	t_R			5			ms

Note) *7. Typical values at Ta=25℃.

10. Pin Capacitance

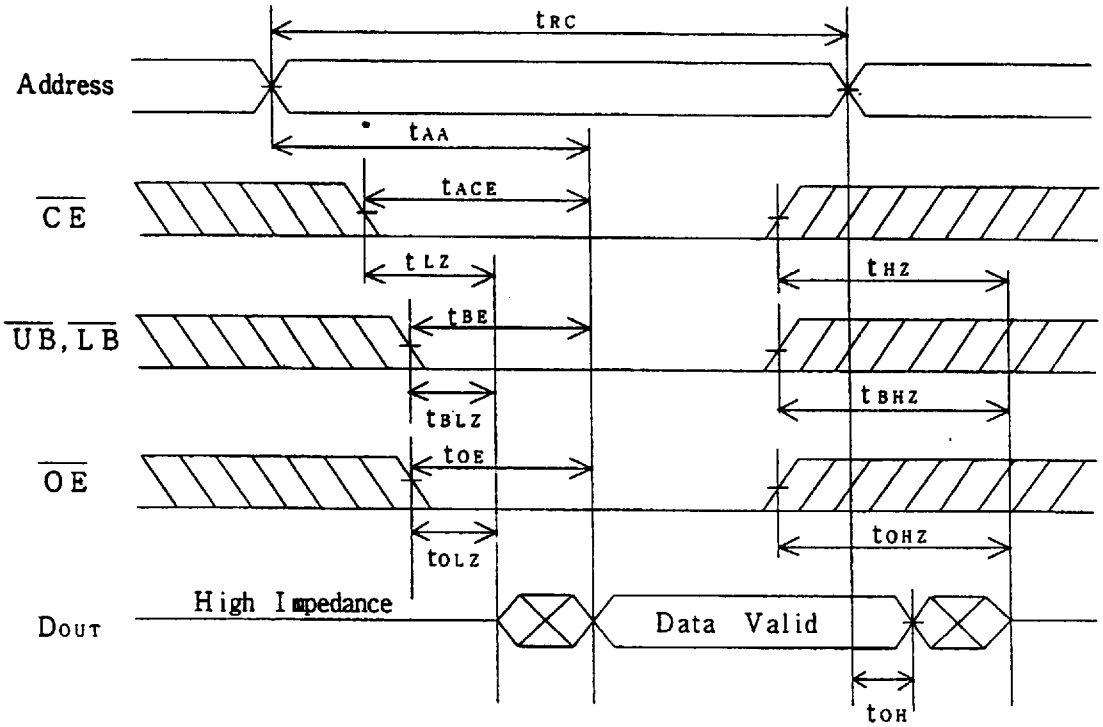
(Ta=25℃, f=1MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Input capacitance	C_{IN}	$V_{IN}=0V$			10	pF	*8
I/O capacitance	$C_{I/O}$	$V_{I/O}=0V$			10	pF	*8

Note) *8. This parameter is sampled and not production tested.

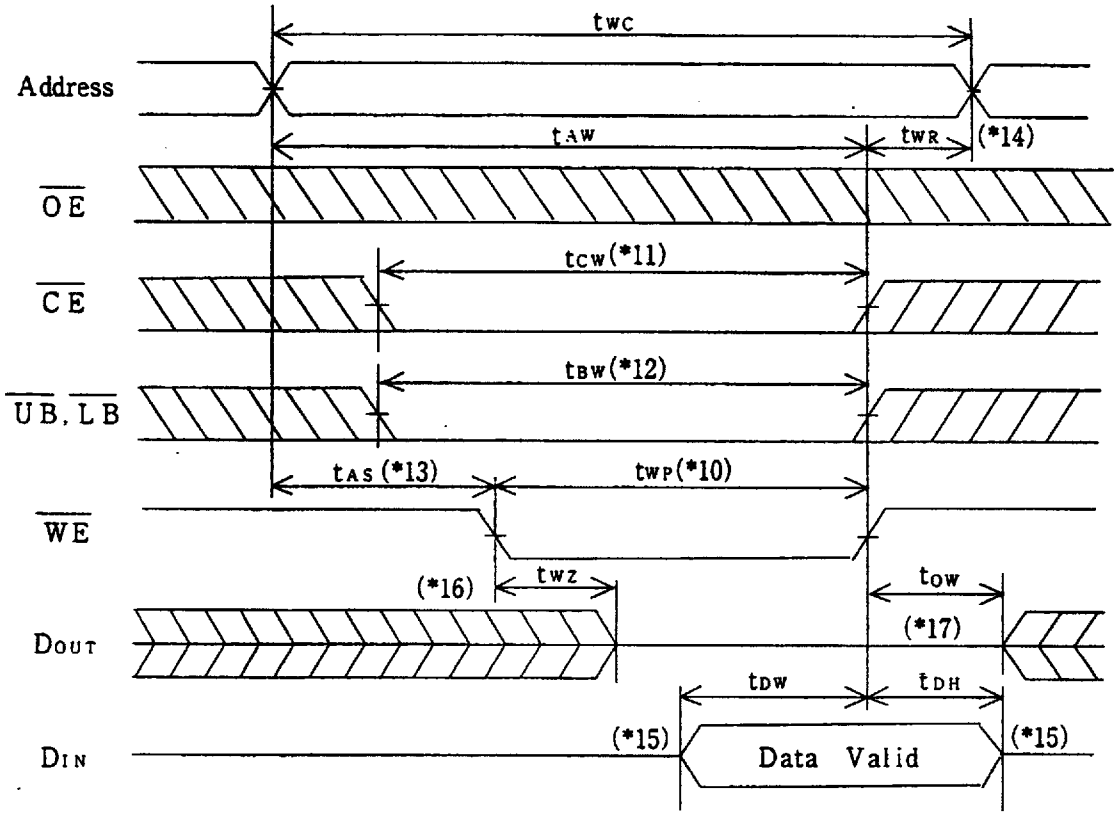
11. Timing Chart

Read cycle timing chart (*9)

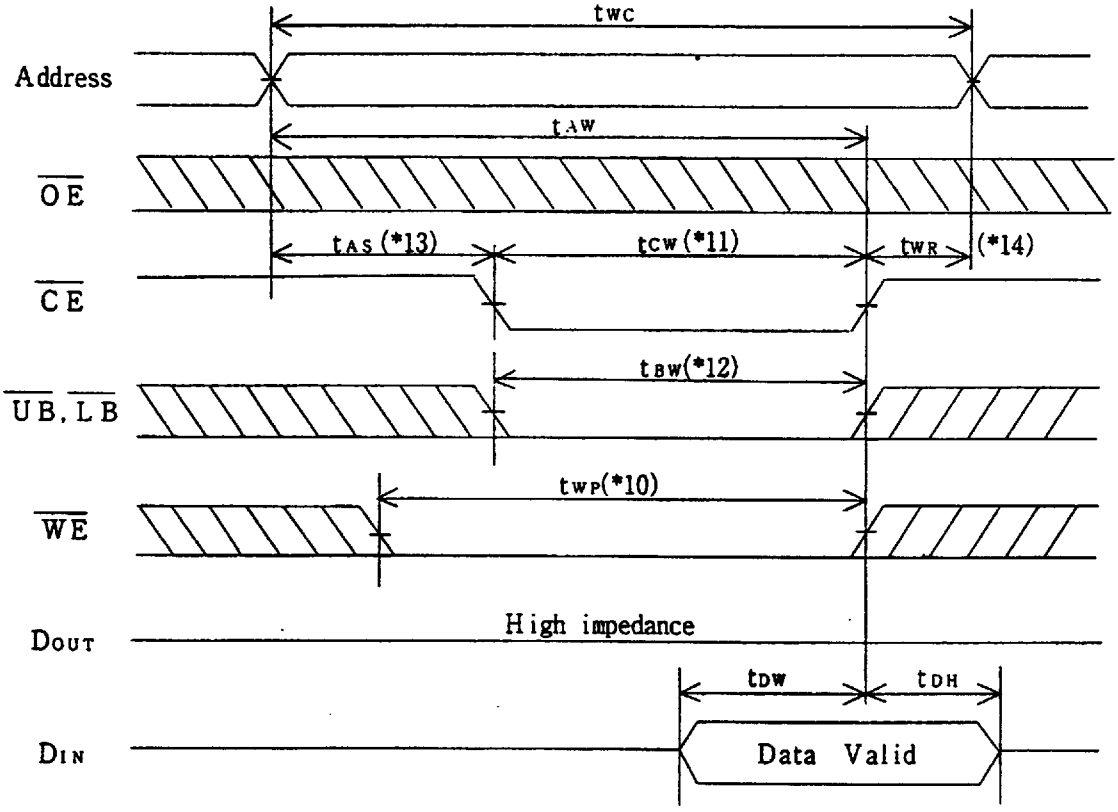


Note) *9. $\overline{WE}$ is high for Read cycle.

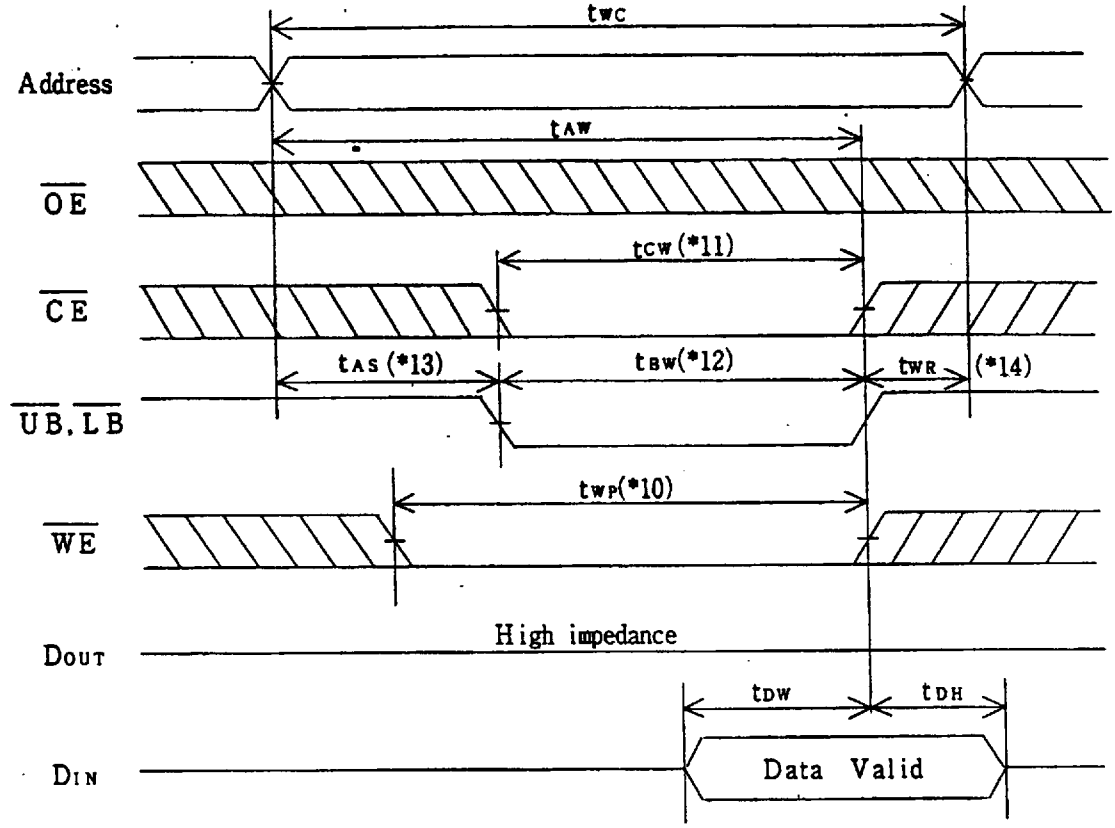
Write cycle timing chart ($\overline{WE}$ Controlled)



Write cycle timing chart ($\overline{CE}$ Controlled)



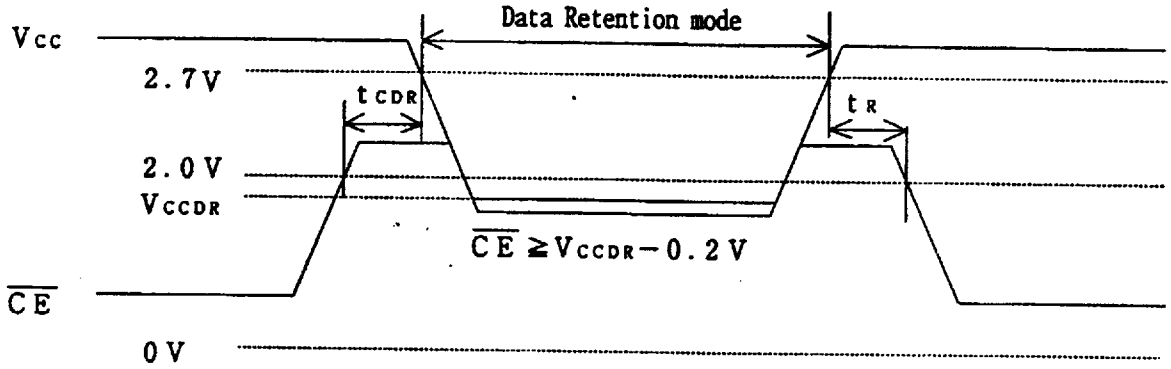
Write cycle timing chart ($\overline{UB}$,$\overline{LB}$ Controlled)



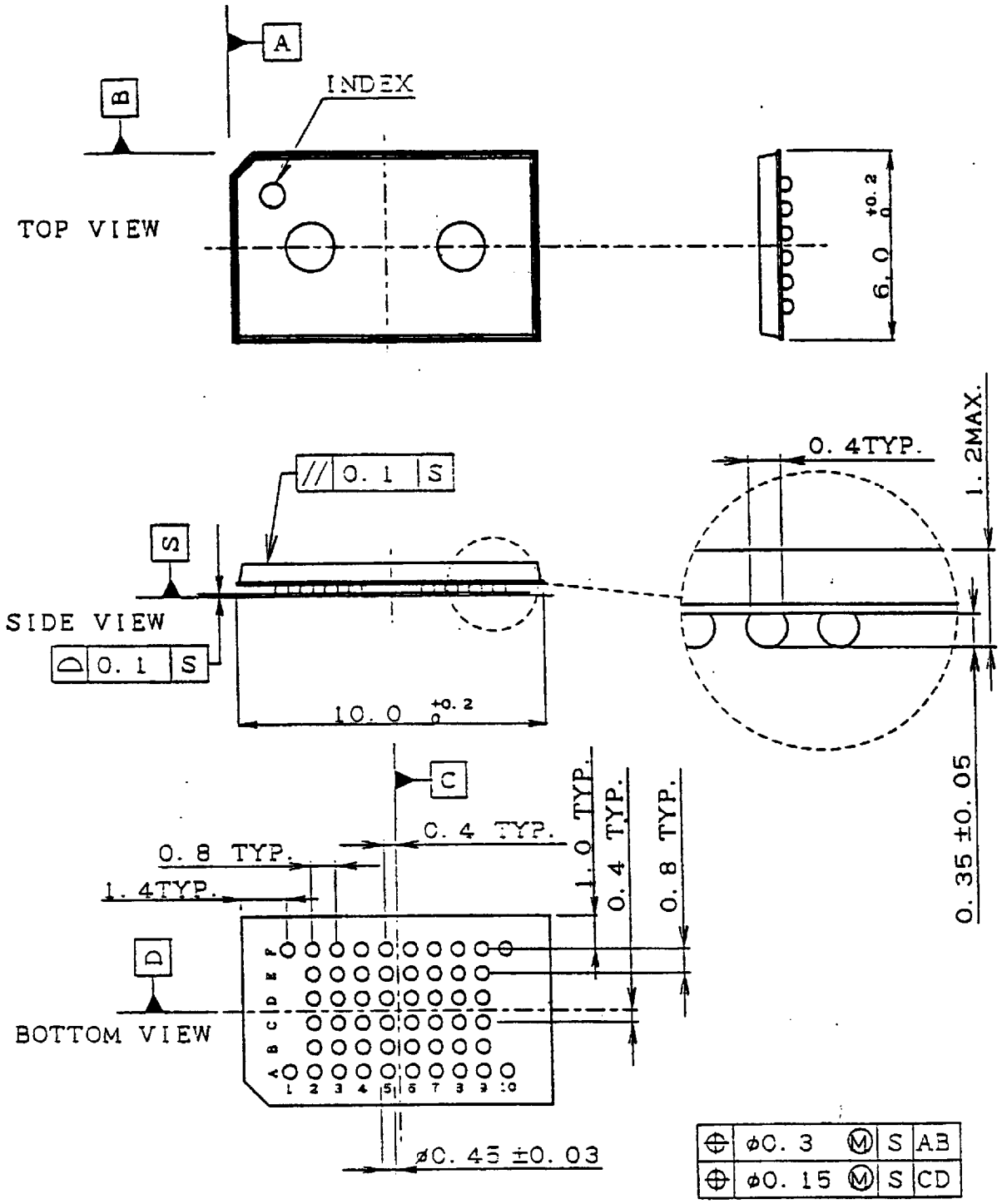
Note) * 10. A write occurs during the overlap of a low $\overline{CE}$, a low $\overline{WE}$, and a low $\overline{UB}$ or $\overline{LB}$. A write begins at the latest transition among $\overline{CE}$ going low, $\overline{WE}$ going low, and $\overline{UB}$ or $\overline{LB}$ going low. A write ends at the earliest transition among $\overline{CE}$ going high, $\overline{WE}$ going high, and $\overline{UB}$ or $\overline{LB}$ going high.

* 11. t_{CW} is measured from the later of $\overline{CE}$ going low to the end of write.
* 12. t_{BW} is measured from the time of $\overline{UB}$ or $\overline{LB}$ going low to the end of write.
* 13. t_{AS} is measured from the address valid to the beginning of write.
* 14. t_{WR} is measured from the end of write to the address change.
* 15. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
* 16. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
* 17. If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ going high or before $\overline{WE}$ going high, the outputs remain in high impedance state.

Data Retention timing chart ($\overline{CE}$ Controlled)



SHARP



改訂 DATE	改訂事 REVISE		担当 CHARGE	尺度 SCALE	単位 UNIT	適用機種 APPLICABLE MODEL	
				5/1	1=1/1mm		
				電子マトリクス MATRIX	10 × 6	名称 NAME	CSP052-P-0610 (FBGA052-P-0610)
				電子数 COUNTS	52		
				電子ピッチ PITCH	0.8	コード CODE	CSP-GR-052-1 -0610
日付 DATE	1997. 12. 16			シャープ株式会社 SHARP CORPORATION			
設計 DESIGN	製図 DRAW	写図 TRACE	検図 CHECK	承認 APPROVE	IC福山事業本部 FUKUYAMA IC GROUP	図番 DRAWING No.	AA2070
M. Matsu				実装プロセス技術部 TOP MODULE ASSEMBLY ENGINEERING DEPT.			