Contents

1. Decription

The LH51V256HT-85SL is a static RAM organized as 32,768×8 bit with provides low-power standby mode.

It is fabricated using silicon-gate CMOS process technology.

Features

○Access Time . . . . 250 ns (Max.)
. . . . 100 ns (Max.at Vcc=2.7V)

○Operating current . . . . 25 mA (Max.at Vcc=3.6V)
. . . . 5 mA (Max.at Vcc=3.6V, tRC, twc=1μs)

○Standby current . . . . 5 μA (Max.at Vcc=3.6V, Ta=85℃)

○Data retention current . . . . 0.2 μA (Max.at VccDR=3.0V, Ta=25℃)

○Low voltage operating range . . . . 1.8V to 3.6V

○Operating temperature . . . . −40℃ to +85℃

○Fully static operation

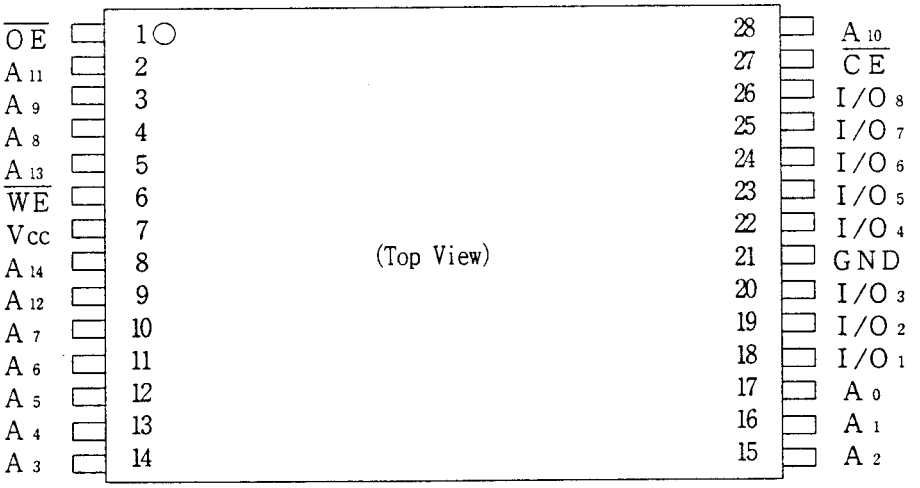
○Three-state output

○Not designed or rated as radiation hardened

○ 28pin TSOP(TSOP28-P-0813) plastic package

○P-type bulk silicon

2. Pin Configuration



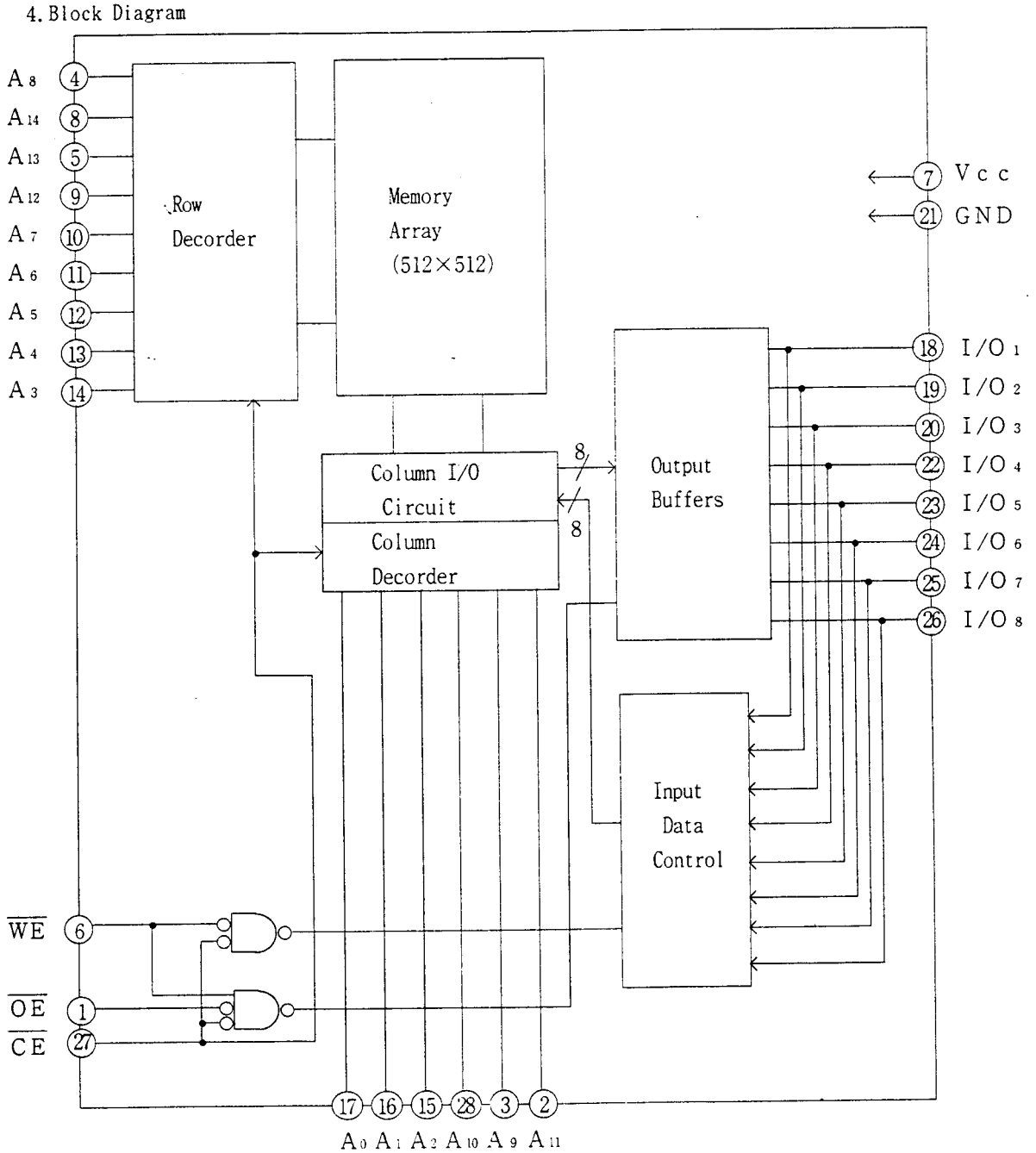
Pin Name	Function
A_0 to A_{14}	Address inputs
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
I/O_1 to I/O_8	Data inputs/outputs
Vcc	Power supply
GND	Ground

3. Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O_1 to I/O_8	Supply current
H	*	*	Standby	High impedance	Standby (I_{SB})
L	H	L	Read	Data output	Active (I_{CC})
L	H	H	Output disable	High impedance	Active (I_{CC})
L	L	*	Write	Data Input	Active (I_{CC})

(*=Don't Care, L=Low, H=High)

4. Block Diagram



5. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage (*1)	V_{CC}	−0.3 to +4.6	V
Input voltage (*1)	V_{IN}	−0.3 (*2) to Vcc+0.3	V
Operating temperature	T_{opr}	−40 to +85	℃
Storage temperature	T_{stg}	−65 to +150	℃

Note) *1. The maximum applicable voltage on any pin with respect to GND.
*2. Undershoot of −3.0V is allowed width of pluse bellow 50ns.

6. Recommended DC Operating Conditions

(Ta= −40℃ to +85℃)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		V_{CC}	1.8		3.6	V
Input voltage	Vcc=1.8V to 3.6V	V_{IH}	Vcc−0.2		Vcc+0.3	V
		V_{IL}	−0.3 (*3)		0.2	
	Vcc=2.7V to 3.6V	V_{IH}	2.0		Vcc+0.3	V
		V_{IL}	−0.3 (*3)		0.6	

Note) *3. Undershoot of −3.0V is allowed width of pluse below 50ns.

7. DC Electrical Characteristics

(Ta=−40℃ to +85℃, Vcc=1.8V to 3.6V)

Parameter	Symbol	Conditions	Min.	Typ. (*4)	Max.	Unit
Input leakage current	I_{LI}	V_{IN}=0V to V_{CC}	−1.0		1.0	μA
Output leakage current	I_{LO}	$\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH} $V_{I/O}$=0V to V_{CC}	−1.0		1.0	μA
Operating supply current	I_{CC}	Minmum cycle $\overline{CE}$=V_{IL}, V_{IN}=V_{IL} or V_{IH} $I_{I/O}$=0mA		14	25	mA
	I_{CC1}	t_{RC}, t_{WC}=1μs $\overline{CE}$=V_{IL}, , V_{IN}=V_{IL} or V_{IH} $I_{I/O}$=0mA			5	mA
Standby current	I_{SB}	$\overline{CE}$ ≧ V_{CC}−0.2V, V_{CC}=3.6V		0.02	5	μA
	I_{SB1}	$\overline{CE}$=V_{IH}, V_{CC}=3.6V			0.4	mA
Output voltage	V_{OL}	I_{OL}= 0.5mA			0.6	V
	V_{OH}	I_{OH}=−0.5mA	Vcc-0.5			V

Note) *4. Typical values at Vcc=3.0V, Ta=25℃.

8. AC Electrical Characteristics

AC Test Conditions

Input pulse level	0V to Vcc	
Input rise and fall time	5ns	
Input and Output timing Ref. level	Vcc=2.7V to 3.6V	1.5V
	Vcc=1.8V to 3.6V	1/2 Vcc
Output load	C_L=30pF (*5)	

Note) *5. Including scope and jig capacitance.

Read cycle

(Ta=−40℃ to +85℃, Vcc= 1.8V to 3.6V)

Parameter	Vcc	1.8V to 3.6V		2.7V to 3.6V		Unit	
	Symbol	Min.	Max.	Min.	Max.		
Read cycle time	t_{RC}	250		100		ns	
Address access time	t_{AA}		250		100	ns	
$\overline{CE}$ access time	t_{ACE}		250		100	ns	
Output enable to output valid	t_{OE}		150		50	ns	
Output hold from address change	t_{OH}	10		10		ns	
$\overline{CE}$ Low to output active	t_{LZ}	10		10		ns	*6
$\overline{OE}$ Low to output active	t_{OLZ}	10		10		ns	*6
$\overline{CE}$ High to output in High impedance	t_{HZ}	0	60	0	60	ns	*6
$\overline{OE}$ High to output in High impedance	t_{OHZ}	0	60	0	60	ns	*6

Write cycle

(Ta=−40℃ to +85℃, Vcc= 1.8V to 3.6V)

Parameter	Vcc	1.8V to 3.6V		2.7V to 3.6V		Unit	
	Symbol	Min.	Max.	Min.	Max.		
Write cycle time	t_{WC}	250		100		ns	
$\overline{CE}$ Low to end of write	t_{CW}	200		80		ns	
Address valid to end of write	t_{AW}	200		80		ns	
Address setup time	t_{AS}	0		0		ns	
Write pluse width	t_{WP}	150		60		ns	
Write recovery time	t_{WR}	0		0		ns	
Input data setup time	t_{DW}	100		40		ns	
Input data hold time	t_{DH}	0		0		ns	
$\overline{WE}$ High to output active	t_{OW}	10		10		ns	*6
$\overline{WE}$ Low to output in High impedance	t_{WZ}	0	60	0	60	ns	*6
$\overline{OE}$ High to output in High impedance	t_{OHZ}	0	60	0	60	ns	*6

Note) *6. Active output to High impedance and High impedance to output active tests specified for a ±200mV transition from steady levels into the test load.

9. Data Retention Characteristics

(Ta= −40℃ to +85℃)

Paramenter	Symbol	Conditions		Min.	Typ. (*7)	Max.	Unit
Data Retention supply voltage	V_{CCDR}	$\overline{CE} \geqq V_{CCDR} - 0.2$ V		1.8		3.6	V
Data Retention supply current	I_{CCDR}	V_{CCDR} = 3 V	Ta = 25℃		0.02	0.2	μA
		$\overline{CE} \geqq V_{CCDR} - 0.2$ V				4	μA

Note) * 7. Typical values at Ta=25℃.

10. Pin Capacitance

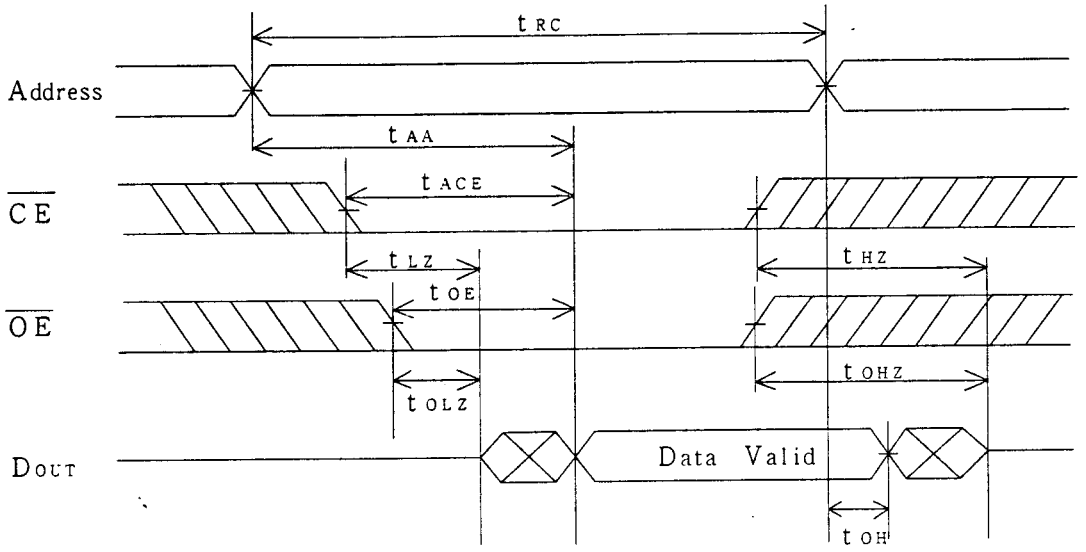
(Ta= 25℃, f = 1MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF	* 8
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF	* 8

Note) * 8. This parameter is sampled and not production tested.

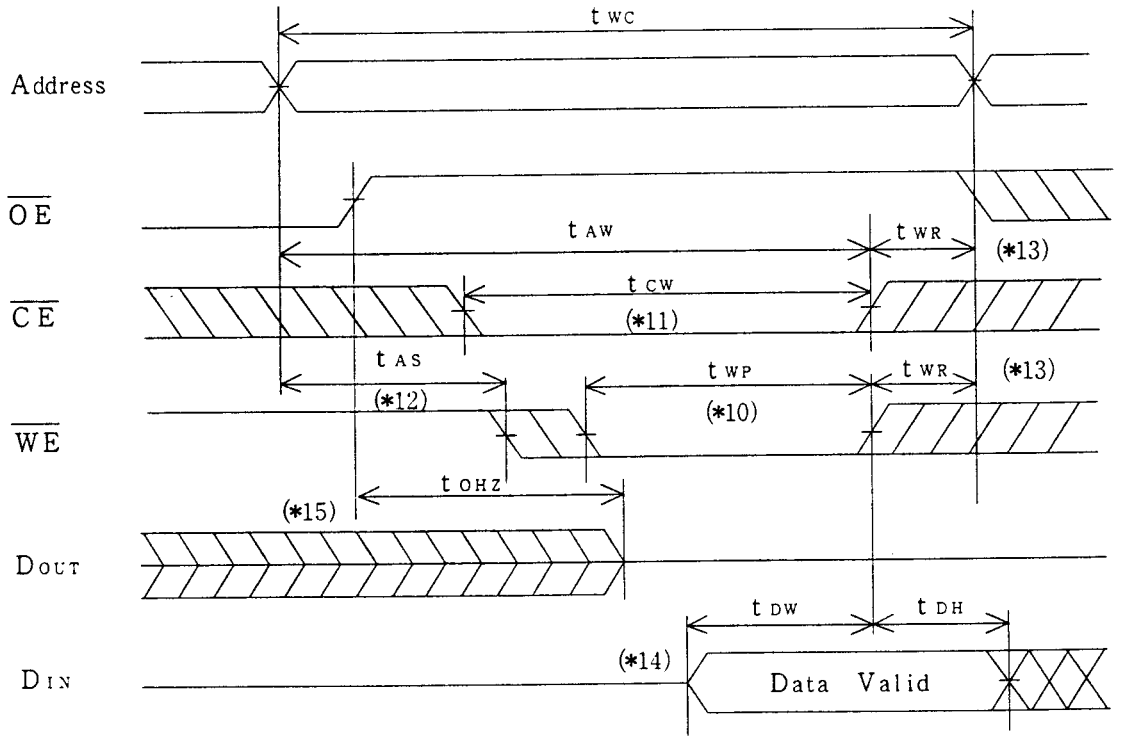
11. Timing Chart

Read cycle timing chart— (＊9)

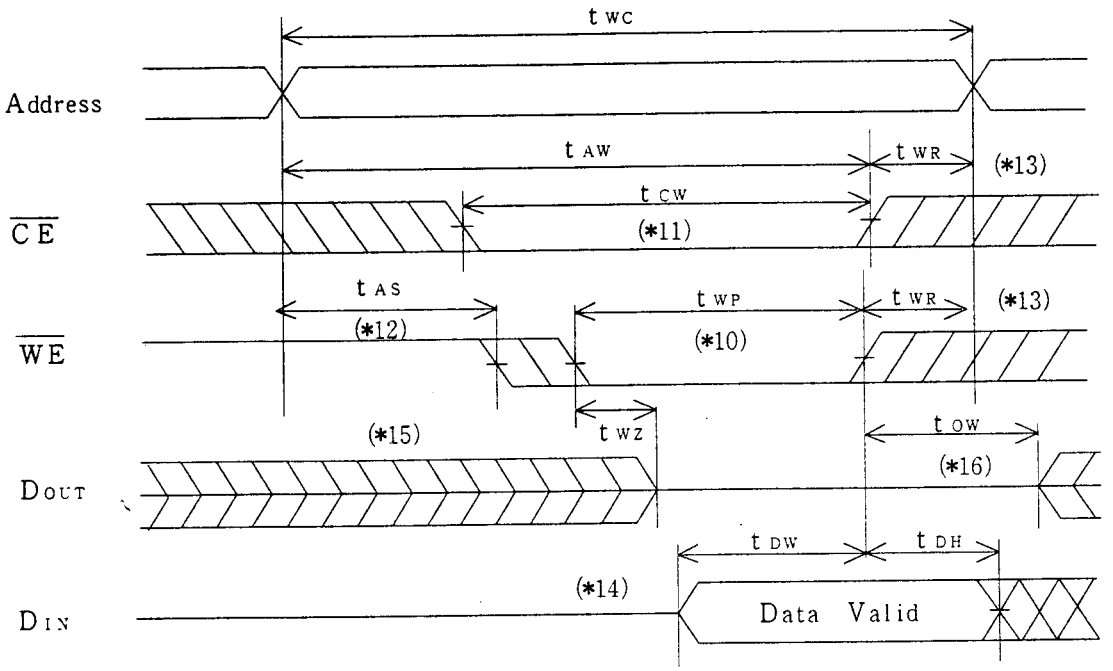


Note) ＊9. $\overline{WE}$ is high for Read cycle.

Write cycle timing chart— ($\overline{OE}$ Controlled)



Write cycle timing chart— ($\overline{OE}$ Low fixed)



Note) * 10. A write occurs during the overlap of a low $\overline{CE}$, and a low $\overline{WE}$,
A write begins at the latest transition among $\overline{CE}$ going low, and $\overline{WE}$ going low.
A write ends at the earliest transition among $\overline{CE}$ going high, and $\overline{WE}$ going high.
t_{WP} is measured from the beginning of write to the end of write.

* 11. t_{CW} is measured from the later of $\overline{CE}$ going low to the end of write.
* 12. t_{AS} is measured from the address valid to the beginning of write.
* 13. t_{WR} is measured from the end of write to the address change.
* 14. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
* 15. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
* 16. If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ going high or before $\overline{WE}$ going high, the outputs remain in high impedance state.