

FEATURES

- ❑ 45 ns Worst-Case Multiply Time
- ❑ Low Power CMOS Technology
- ❑ Replaces TRW MPY016/TMC216, Cypress CY7C516, IDT 7216L, and AMD Am29516
- ❑ Two's Complement, Unsigned, or Mixed Operands
- ❑ Three-State Outputs
- ❑ DESC SMD No. 5962-86873
- ❑ Available 100% Screened to MIL-STD-883, Class B
- ❑ Package Styles Available:
 - 64-pin Sidebrazed, Hermetic DIP
 - 68-pin Commercial PGA
 - 68-pin Ceramic PGA
 - 68-pin Plastic LCC, J-Lead
 - 68-pin Ceramic LCC

DESCRIPTION

The LMU16 and LMU216 are high-speed, low power 16-bit parallel multipliers. The LMU16 and LMU216 are functionally identical; they differ only in packaging. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

The LMU16 and LMU216 produce the 32-bit product of two 16-bit numbers. Data present at the A inputs, along with the TCA control bit, is loaded into the A register on the rising edge of CLK A. B data and the TCB control bit are similarly loaded by CLK B. The TCA and TCB controls specify the A and B operands as two's complement when HIGH, or unsigned magnitude when LOW.

RND is loaded on the rising edge of the logical OR of CLK A and CLK B. RND, when HIGH, adds '1' to the most significant bit position of the least significant half of the product. Subsequent truncation of the 16 least significant bits produces a result correctly rounded to 16-bit precision.

At the output, the Right Shift control (RS) selects either of two output formats. RS LOW produces a 31-bit product with a copy of the sign bit inserted in the MSB position of the least significant half. RS HIGH gives a full 32-bit product. Two 16-bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP) as defined by RS. These registers are loaded on the rising edge of CLK M and CLK L respectively. For asynchronous output, these registers may be made transparent by setting the feed through control (FT) HIGH.

The two halves of the product may be routed to a single 16-bit three-state output port (MSP) via a multiplexer. MSPSEL LOW causes the MSP outputs to be driven by the most significant half of the result. MSPSEL HIGH routes the least significant half of the result to the MSP outputs. In addition, the LSP is available via the B port through a separate three-state buffer.

The output multiplexer control MSPSEL uses a pin which is a supply ground in the TRW MPY016H/TMC216H. When this control is LOW (GND), the function is that of the MPY016H/TMC216H, thus allowing full compatibility.

LMU16/216 BLOCK DIAGRAM

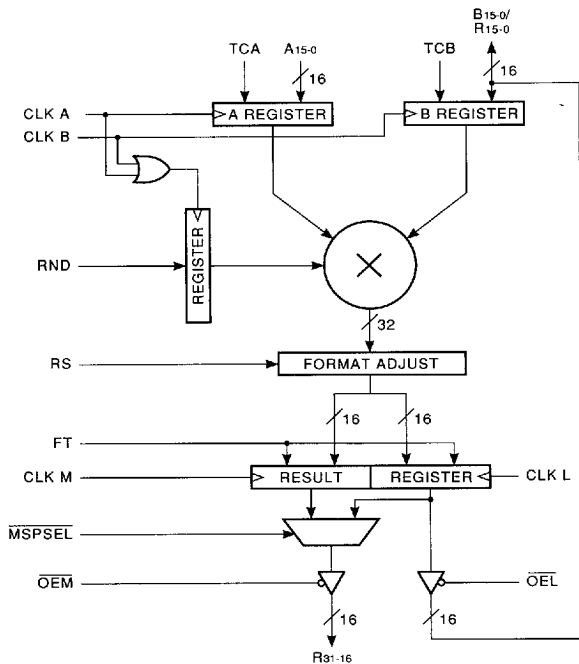


FIGURE 1A. INPUT FORMATS

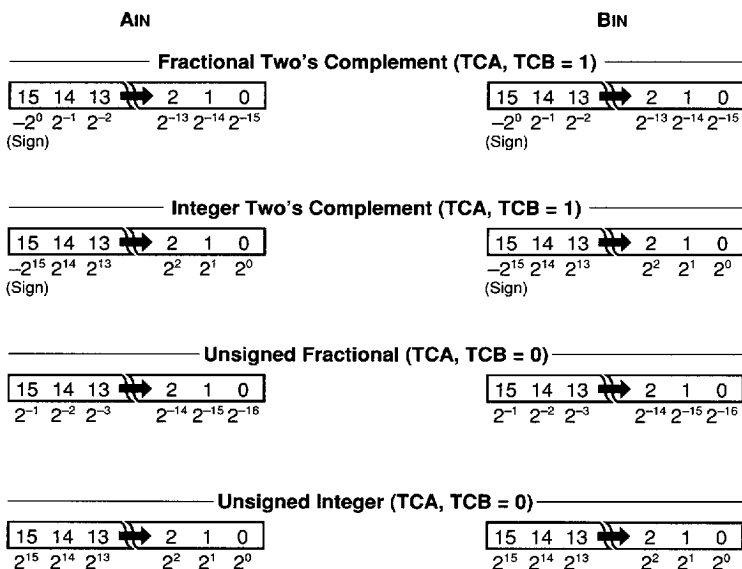
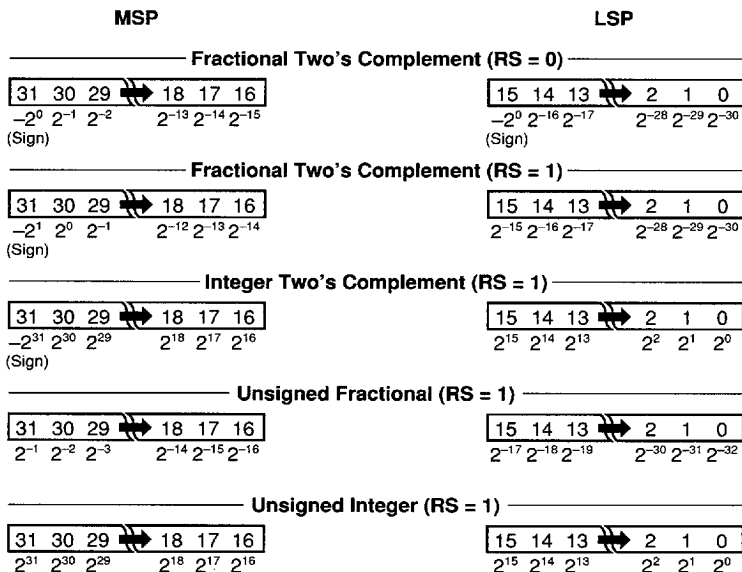


FIGURE 1B. OUTPUT FORMATS



MAXIMUM RATINGS Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V _{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V _{CC} ≤ 5.25 V
Active Operation, Military	−55°C to +125°C	4.50 V ≤ V _{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS Over Operating Conditions (Note 4)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V _{OH}	Output High Voltage	V _{CC} = Min., I _{OH} = −2.0 mA	3.5			V
V _{OL}	Output Low Voltage	V _{CC} = Min., I _{OL} = 8.0 mA			0.5	V
V _{IH}	Input High Voltage		2.0		V _{CC}	V
V _{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I _{Ix}	Input Current	Ground ≤ V _{IN} ≤ V _{CC} (Note 12)			±20	μA
I _{OZ}	Output Leakage Current	Ground ≤ V _{OUT} ≤ V _{CC} (Note 12)			±20	μA
I _{CC1}	V _{CC} Current, Dynamic	(Notes 5, 6)		12	25	mA
I _{CC2}	V _{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

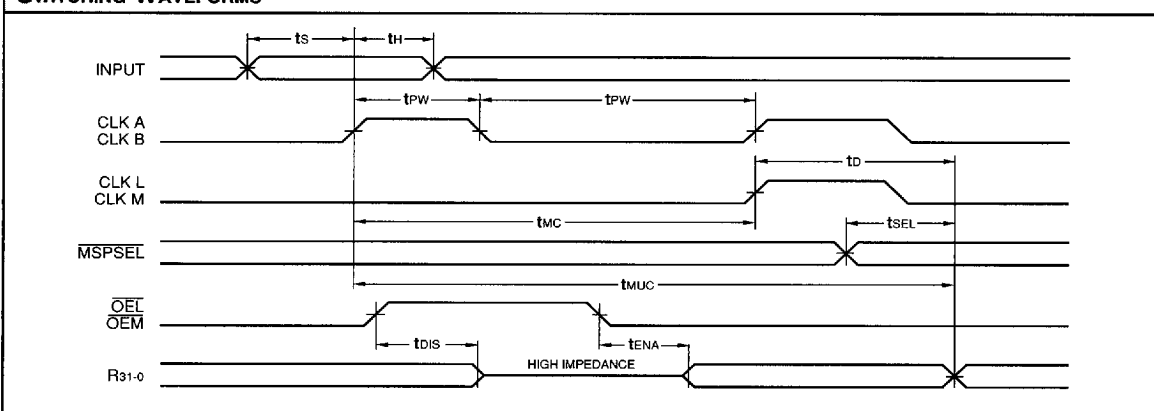
COMMERCIAL OPERATING RANGE (0°C to +70°C) Notes 9, 10 (ns)

Symbol Parameter		LMU16/216–					
		65		55		45	
		Min	Max	Min	Max	Min	Max
t _{MC}	Clocked Multiply Time		65		55		45
t _{MUC}	Unclocked Multiply Time		85		75		65
t _{PW}	Clock Pulse Width	15		15		15	
t _S	Input Setup Time	15		15		15	
t _H	Input Hold Time	1		1		1	
t _D	Output Delay		30		30		30
t _{SEL}	Output Select Delay		25		25		25
t _{ENA}	Three-State Output Enable Delay (Note 11)		25		25		25
t _{DIS}	Three-State Output Disable Delay (Note 11)		25		25		25

MILITARY OPERATING RANGE (–55°C to +125°C) Notes 9, 10 (ns)

Symbol Parameter		LMU16/216–					
		75		65		55	
		Min	Max	Min	Max	Min	Max
t _{MC}	Clocked Multiply Time		75		65		55
t _{MUC}	Unclocked Multiply Time		95		85		75
t _{PW}	Clock Pulse Width	20		15		15	
t _S	Input Setup Time	15		15		15	
t _H	Input Hold Time	2		2		2	
t _D	Output Delay		35		30		30
t _{SEL}	Output Select Delay		30		30		30
t _{ENA}	Three-State Output Enable Delay (Note 11)		25		25		25
t _{DIS}	Three-State Output Disable Delay (Note 11)		25		25		25

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above VCC will be clamped beginning at -0.6 V and VCC + 0.6 V. The device can withstand indefinite operation with inputs in the range of -0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of VCC or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except tENA/tDIS test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified IOH and IOL at an output voltage of VOH min and VOL max respectively. Alternatively, a diode bridge with upper and lower current sources of IOH and IOL respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For tENABLE and tDISABLE measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 pF ceramic capacitor should be installed between VCC and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device VCC and the tester common, and device ground and tester common.

b. Ground and VCC supply planes must be brought directly to the DUT socket or contactor fingers.

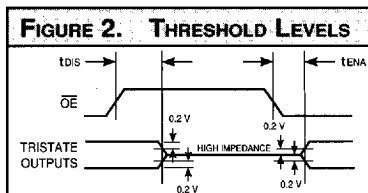
c. Input voltages should be adjusted to compensate for inductive ground and VCC noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from

the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

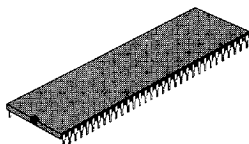
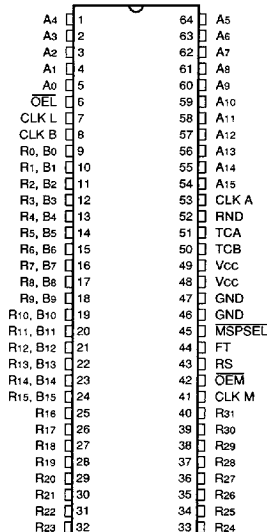
11. Transition is measured ± 200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

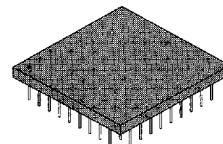
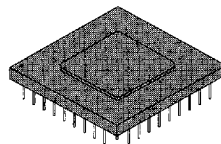
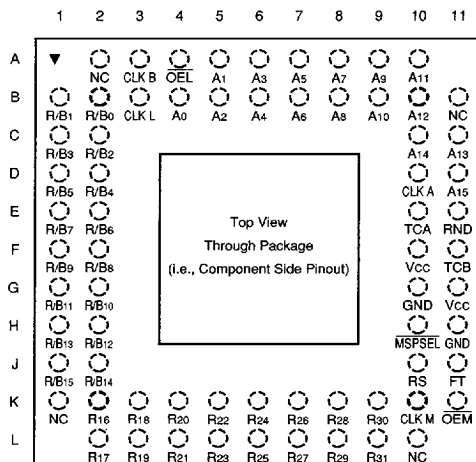


LMU16 — ORDERING INFORMATION

64-pin



68-pin

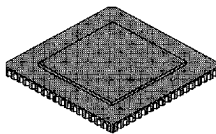
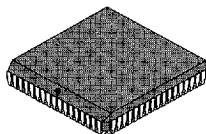
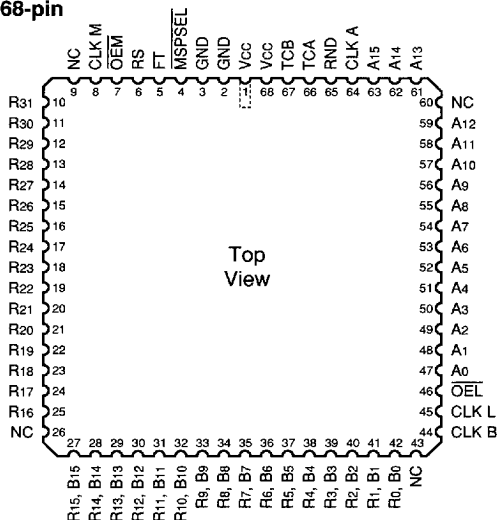


Speed	Sidebraze Hermetic DIP (D6)	Commercial Pin Grid Array (E2)	Ceramic Pin Grid Array (G2)
	0°C to +70°C — COMMERCIAL SCREENING		
65 ns	LMU16DC65	LMU16EC65	LMU16GC65
55 ns	LMU16DC55	LMU16EC55	LMU16GC55
45 ns	LMU16DC45	LMU16EC45	LMU16GC45
	-55°C to +125°C — COMMERCIAL SCREENING		
75 ns	LMU16DM75		LMU16GM75
65 ns	LMU16DM65		LMU16GM65
55 ns	LMU16DM55		LMU16GM55
	-55°C to +125°C — MIL-STD-883 COMPLIANT		
75 ns	LMU16DMB75		LMU16GMB75
65 ns	LMU16DMB65		LMU16GMB65
55 ns	LMU16DMB55		LMU16GMB55

Multipliers

LMU216 — ORDERING INFORMATION

68-pin



Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)		
0°C to +70°C — COMMERCIAL SCREENING				
65 ns	LMU216JC65	LMU216KC65		
55 ns	LMU216JC55	LMU216KC55		
45 ns	LMU216JC45	LMU216KC45		
-55°C to +125°C — COMMERCIAL SCREENING				
75 ns		LMU216KM75		
65 ns		LMU216KM65		
55 ns		LMU216KM55		
-55°C to +125°C — MIL-STD-883 COMPLIANT				
75 ns		LMU216KMB75		
65 ns		LMU216KMB65		
55 ns		LMU216KMB55		

Multipliers