2GB- 256Mx72, ECC, DDR SDRAM DIMM REGISTERED MODULE

DESCRIPTION

The WED3EG72256SXX-JD3 is a 256Mx72 Double Data Rate SDRAM memory module based on 1 Gigabit DDR SDRAM components. The module consists of eighteen, 256Mx4 DDR SDRAMs in 66 pin TSOP packages mounted on a 184 pin FR4 substrate.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges and Burst Lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURES

- Double data rate architecture; two data transfers per clock cycle
- Clock speeds of 100MHz and 133MHz
- Bi-directional data strobes ($\overline{DQS}$)
- Differential clock inputs (CK & $\overline{CK}$)
- DLL aligns DQ and DQS transition with CK transition
- Programmable Read latency 2, 2.5 (clock)
- Programmable Burst Length (2, 4, 8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto and self refresh
- Serial presence detect
- JEDEC standard 184 pin DIMM package
- Power supply: Vdd: 2.5V ± 0.2V, Vddq: 2.5V ± 0.2V

OPERATING FREQUENCIES

	262JD3 (DDR266@CL=2)	265JD3 (DDR266@CL=2.5)	202JD2 (DDR200@CL=2)
Speed	133MHz	133MHz	100MHz
CL-tRCD-tRP	2-3-3	2.5-3-3	2-2-2

Advance information: Speed may not be available.

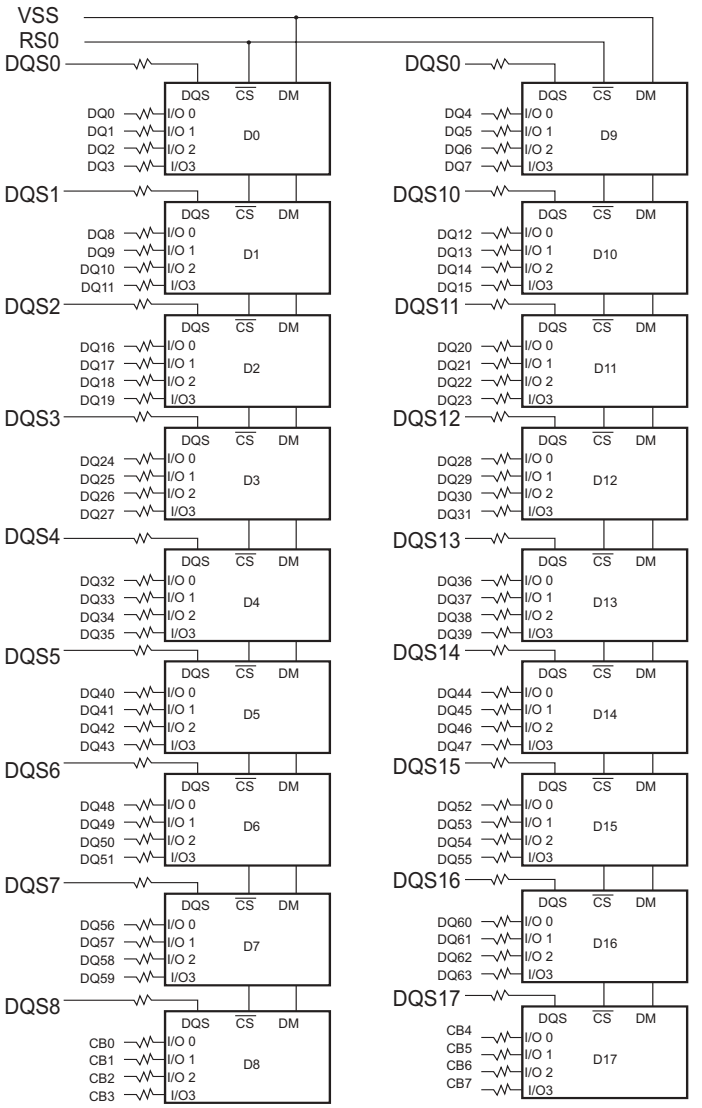
PIN CONFIGURATION (FRONT SIDE/BACK SIDE)

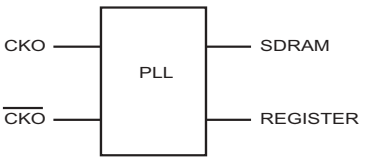
PIN	FRONT	PIN	FRONT	PIN	FRONT	PIN	BACK	PIN	BACK	PIN	BACK
1	VREF	32	A5	62	VDDQ	93	VSS	124	VSS	154	$\overline{RAS}$
2	DQ0	33	DQ24	63	$\overline{WE}$	94	DQ4	125	A6	155	DQ45
3	VSS	34	VSS	64	DQ41	95	DQ5	126	DQ28	156	VDDQ
4	DQ1	35	DQ25	65	$\overline{CAS}$	96	VDDQ	127	DQ29	157	$\overline{CS0}$
5	DQS0	36	DQS3	66	VSS	97	DQS9	128	VDDQ	158	$\overline{NC}$
6	DQ2	37	A4	67	DQS5	98	DQ6	129	DQS12	159	DQS14
7	VDD	38	VDD	68	DQ42	99	DQ7	130	A3	160	VSS
8	DQ3	39	DQ26	69	DQ43	100	VSS	131	DQ30	161	DQ46
9	NC	40	DQ27	70	VDD	101	NC	132	VSS	162	DQ47
10	$\overline{RESET}$	41	A2	71	NC	102	NC	133	DQ31	163	NC
11	VSS	42	VSS	72	DQ48	103	NC	134	CB4	164	VDDQ
12	DQ8	43	A1	73	DQ49	104	VDDQ	135	CB5	165	DQ52
13	DQ9	44	CB0	74	VSS	105	DQ12	136	VDDQ	166	DQ53
14	DQS1	45	CB1	75	NC	106	DQ13	137	$\overline{CK0}$	167	A13
15	VDDQ	46	VDD	76	NC	107	DQS10	138	$\overline{CK0}$	168	VDD
16	NC	47	DQS8	77	VDDQ	108	VDD	139	VSS	169	DQS15
17	NC	48	A0	78	DQS6	109	DQ14	140	DQS17	170	DQ54
18	VSS	49	CB2	79	DQ50	110	DQ15	141	A10	171	DQ55
19	DQ10	50	VSS	80	DQ51	111	NC	142	CB6	172	VDDQ
20	DQ11	51	CB3	81	VSS	112	VDDQ	143	VDDQ	173	NC
21	CKE0	52	BA1	82	VDDID	113	NC	144	CB7	174	DQ60
22	VDDQ		**KEY**	83	DQ56	114	DQ20		**KEY**	175	DQ61
23	DQ16	53	DQ32	84	DQ57	115	A12	145	VSS	176	VSS
24	DQ17	54	VDDQ	85	VDD	116	VSS	146	DQ36	177	DQS16
25	DQS2	55	DQ33	86	DQS7	117	DQ21	147	DQ37	178	DQ62
26	VSS	56	DQS4	87	DQ58	118	A11	148	VDD	179	DQ63
27	A9	57	DQ34	88	DQ59	119	DQS11	149	DQS13	180	VDDQ
28	DQ18	58	VSS	89	VSS	120	VDD	150	DQ38	181	SA0
29	A7	59	BA0	90	NC	121	DQ22	151	DQ39	182	SA1
30	VDDQ	60	DQ35	91	SDA	122	A8	152	VSS	183	SA2
31	DQ19	61	DQ40	92	SCL	123	DQ23	153	DQ44	184	VDDSPD

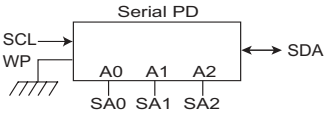
PIN DESCRIPTION

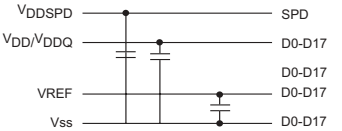
Pin Name	Function	Pin Name	Function
A0 ~ A13	Address input (Multiplexed)	VDD	Power supply (2.5V)
BA0 ~ BA1	Bank Select Address	VDDQ	Power Supply for DQS (2.5V)
DQ0 ~ DQ63	Data input/output	VSS	Ground
DQS0 ~ DQS17	Data Strobe input/output	VREF	Power Supply for reference
CK0, $\overline{CK0}$	Clock input	VDDSPD	Serial EEPROM Power/Supply (2.3V to 3.6V)
CKE0	Clock enable input	SDA	Serial data I/O
$\overline{CS0}$,	Chip select input	SCL	Serial clock
$\overline{RAS}$	Row address strobe	SA0 ~ 2	Address in EEPROM
$\overline{CAS}$	Column address strobe	$\overline{NC}$	No Connection
$\overline{WE}$	Write enable	VDDID	VDD Identification flag
CB0 ~ CB7	Check bit (Data-in/data-out)	Reset	RESET ENABLE

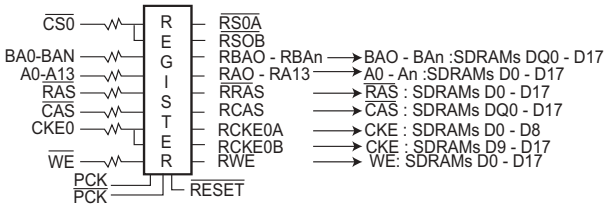
FUNCTIONAL BLOCK DIAGRAM:











Notes"

1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS resistors should be 22 Ohms.
4. Address and control resistors should be 22 Ohms.

POWER & DC OPERATING CONDITIONS (SSTL_2 IN/OUT)

Recommend operating conditions (voltage referenced to Vss = øV, TA = ø to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage (for device with a nominal VDD of 2.5V)	VDD	2.3	2.7	–	–
I/O Supply voltage	VDDQ	2.3	2.7	V	
I/O Reference voltage	VREF	VDDQ/2-50mV	VDDQ/2+50mV	V	1
I/O Termination voltage (system)	VTT	VREF-0.04	VREF+0.04	V	2
Input logic high voltage	VIH (DC)	VREF+0.15	VDDQ+0.3	V	4
Input logic low voltage	VIL (DC)	-0.3	VREF-0.15	V	4
Input Voltage Level, CK and $\overline{CK}$ inputs	VIN (DC)	-0.3	VDDQ+0.3	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	VID(DC)	0.3	VDDQ+0.6	V	3
Input leakage current	I_I	-2	2	uA	
Output leakage current	IOZ	-5	5	uA	
Output High Current (Normal strength driver); VOUT = VTT + 0.84V	IOH	-16.8		mA	
Output High Current (Normal strength driver); VOUT = VTT - 0.84V	IOL	16.8		mA	
Output High Current (Half strength driver); VOUT = VTT + 0.45V	IOH	-9		mA	
Output High Current (Half strength driver); VOUT = VTT - 0.45V	IOL	9		mA	

Notes:

1. *Includes ± 25mV margin for DC offset on VREF, and a combined total of ± 50mV margin for all AC noise and DC offset on VREF, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on VREF and internal DRAM noise coupled to VREF, both of which may result in VREF noise. VREF should be de-coupled with an inductance of £ 3nH.*
2. *VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF.*
3. *VID is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.*
4. *These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a VREF that has been bandwidth limited to 200MHZ.*

AC OPERATING CONDITIONS

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage,	VIH (AC)	VREF+ 0.31	-	V	3
Input Low (Logic 0) Voltage,	VIL (AC)	-VREF - 0.31		V	3
clock Input Differential Voltage, CK and CK inputs	VID (AC)	0.7	VDDQ+0.6	V	1
clock Input Crossing Point Voltage, CK and CK inputs	VIX (AC)	0.5XVDDQ-0.2	0.5XVDDQ+0.2	V	2

Notes:

1. *VID is the magnitude of the difference between the input level on CK and the input on $\overline{CK}$.*
2. *The value of VIX is expected to equal 0.5*V DDQ of the transmitting device and must track variations in the DC level of the same.*
3. *These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relation to VREF relation to a VREF envelope that has been bandwidth limited 20MHZ.*

IDD SPECIFICATIONS AND TEST CONDITIONS

(Recommended operating conditions, TA = 0 to 70C, VDDQ = 2.5V +\-0.2V, VDD = 2.5V +\-0.2V)

Parameter	Symbol	Conditions	DDR266@CL=2, 2.5 Max	DDR200@CL=2 Max	Units
Operating Current	IDD0	One device bank; Active = Precharge; TRC=TRC (MIN); TCK=TCK (MIN); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two cycles.	1957	1900	mA
Operating Current	IDD1	One device bank; Active-Read-Precharge; Burst = 2; TRC=TRC (MIN); TCK=TCK (MIN); Iout = 0mA; Address and control inputs changing once per clock cycle.	2632	2450	mA
Precharge Power-Down	IDD2P	All device banks idle; Power- down	135	125	mA
Standby Current		mode; TCK=TCK (MIN); CKE=(low)			
dle Standby Current	IDD2F	CS# = High; All device banks idle; TCK=TCK (MIN); CKE = high; Address and other control inputs changing once per clock cycle. Vin = Vref for DQ, DQS and DM.	810	750	mA
Active Power-Down Standby Current	IDD3P	One device bank active; Power-down mode; TCK (MIN); CKE=(low)	405	385	mA
Active Standby Current	IDD3N	CS# = High; CKE = High; One device bank; Active-Precharge; TRC=TRAS (MAX); TCK=TCK (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle.	790	700	mA
Operating Current	IDD4R	Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; TCK=TCK (MIN); Iout = 0mA.	3375	2970	mA
Operating Current	IDD4W	Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; TCK=TCK (MIN); DQ, DM and DQS inputs changing twice per clock cycle.	3375	3250	mA
Auto Refresh Current	IDD5	TRC=TRC (MIN)	4455	4300	mA
Self Refresh Current	IDD6	CKE £ 0.2V	121	115	mA
Operating Current	IDD7A	Four bank interleaving Reads (BL=4) with auto precharge with TRC=TRC (MIN); TCK=TCK (MIN); Address and control inputs change only during Active Read or Write commands.	6682	6550	mA

Note: Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

AC TIMING PARAMETERS & SPECIFICATIONS

Parameter		Symbol	262JD3 (DDR266@CL=2) Min	262JD3 (DDR266@CL=2) Max	265JD3 (DDR266@CL=2.5) Min	265JD3 (DDR266@CL=2.5) Max	202JD3 (DDR200@CL=2) Min	202JD3 (DDR200@CL=2) Max	Unit	Note
Row cycle time		tRC	65		65		70		ns	
Refresh row cycle time		tRFC	75		75		80		ns	
Row active time		tRAS	40	120K	40	120K	48	120K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD	20		20		20		ns	
Row precharge time		tRP	20		20		20		ns	
Row active to Row active delay		tRRD	15		15		15		ns	
Write recovery time		tWR	15		15		15		ns	
Last data in to Read command		tWTR	1		1		1		tCK	
Col. address to Col. address delay		tCCD	1		1		1		tCK	
Clock cycle time	CL=2.0	tCK	10	13			10	13	ns	5
	CL=2.5				7.5	13			ns	5
Clock high level width		tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
Clock low level width		tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
DQS-out access time from CK/$\overline{CK}$		tDQSCK	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
Output data access time from CK/$\overline{CK}$		tAC	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
Data strobe edge to output data edge		tDQSQ	0.5		0.5		0.6		ns	5
Read Preamble		tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Read Postamble		tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
CK to valid DQS-in		tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
DQS-in setup time		tWPRES	0		0		0		ns	2
DQS-in hold time		tWPRE	0.25		0.25		0.25		tCK	
DQS falling edge to CK rising-setup time		tDSS	0.2		0.2		0.2		tCK	
DQS falling edge from CK rising-hold time		tDSH	0.2		0.2		0.2		tCK	
DQS-in high level width		tDQSH	0.35		0.35		0.35		tCK	
DQS-in low level width		tDQSL	0.35		0.35		0.35		tCK	
DQS-in cycle time		tDSC	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Address and Control Input setup time (fast)		tIS	0.9		0.9		1.1		ns	i,6
Address and Control Input hold time (fast)		tIH	0.9		0.9		1.1		ns	i,6
Address and Control Input setup time (slow)		tIS	1.0		1.0		1.1		ns	i, 6
Address and Control Input hold time (slow)		tIH	1.0		1.0		1.1		ns	i, 6
Data-out high impedance time from CK/$\overline{CK}$		tHZ	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
Data-out low impedance time from CK/$\overline{CK}$		tLZ	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
Input Slew Rate (for input only pins)		tSL(I)	0.5		0.5		0.5		V/ns	6
Input Slew Rate (for I/O pins)		tSL(IO)	0.5		0.5		0.5		V/ns	7
Output Slew Rate (x4,x8)		tSL(O)	1.0	4.5	1.0	4.5	1.0	4.5	V/ns	10
Output Slew Rate Matching Ratio (rise to fall)		tSLMR	0.67	1.5	0.67	1.5	0.67	1.5		

SYSTEM CHARACTERISTICS FOR DDR SDRAM

The following specification parameters are required in systems using DDR266 & DDR200 devices to ensure proper system performance. These characteristics are for system simulation purposes and are guaranteed by design.

Parameter	Symbol	262JD3 (DDR266@CL=2)		265JD3 (DDR266@CL=2.5)		202JD3 (DDR200@CL=2)		Unit	Note
		Min	Max	Min	Max	Min	Max		
Mode register set cycle time	t_{MRD}	15		15		16		ns	
DQ & DM setup time to DQS	t_{DS}	0.5		0.5		0.6		ns	j, k
DQ & DM hold time to DQS	t_{DH}	0.5		0.5		0.6		ns	j, k
Control & Address input pulse width	t_{IPW}	2.2		2.2		2.5		ns	8
DQ & DM unput pulse width	t_{DIPW}	1.75		1.75		2		ns	8
Power down exit time	t_{PDEX}	7.5		7.5		10		ns	
Exit self refresh to non-Read command	t_{XSNR}	75		75		80		ns	
Exit self refresh to read command	t_{XSRD}	200		200		200		tCK	
Refresh interval time	t_{REFI}	7.8		7.8		7.8		us	4
Output DQS valid window	t_{QH}	t_{HP} - t_{QHS}	-	t_{HP} - t_{QHS}	-	t_{HP} - t_{QHS}	-	ns	11
Clock half period	t_{HP}	t_{CL}min or t_{CH}min	- -	t_{CL}min or t_{CH}min	- -	t_{CL}min or t_{CH}min	-	ns	10, 11
Data hold skew factor	t_{QHS}		0.75		0.75		0.8	ns	11
DQS write postamble time	t_{QPST}	0.4	0.6	0.4	0.6	0.4	0.6	tCK	2
Active to Read with Auto precharge command	t_{RAP}	20		20		20			
Auto precharge write revovery + Precharge time	t_{DAL}	(t_{WR}/t_{CK}) +		(t_{WR}/t_{CK}) +		(t_{WR}/t_{CK}) +		tCK	

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to VSS	V_{IN}, Vout	-0.5 ~ 3.6	V
Voltage on VDD supply relative to VSS	VDD, VDDQ	-1.0 ~ 3.6	V
Storage Temperature	TSTG	-55 ~ +150	°C
Power Dissipation	PD	27	W
Short Circuit Current	IOS	50	mA

Notes:
Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

CAPACITANCE (TA = 25°C, F = 1MHz, VDD = 2.5V)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-A13)	CIN1	-	12	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	CIN2	-	12	pF
Input Capacitance (CKE0)	CIN3	-	12	pF
Input Capacitance (CK0, $\overline{CK0}$)	CIN4	-	12	pF
Input Capacitance ($\overline{CS0}$)	CIN5	-	11	pF
Input Capacitance (DQM0-DQM8)	CIN6	-	11	pF
Input Capacitance (BA0-BA1)	CIN7	-	12	pF
Data input/output capacitance (DQ0-DQ63) (DQS)	Cout	-	11	pF
Data input/output capacitance (CB0-CB7)	Cout	-	11	pF

COMMAND TRUTH TABLE

(V = Valid, X = Don't Care, H = Logic High, L = Logic Low)

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0,1	A10/AP	A0~A9 A11, A13	Note
Register	Extended MRS		H	X	L	L	L	L	OP Code			1,2
Register	Mode register Set		H	X	L	L	L	L	OP Code			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X			3
	Self Refresh	Entry		L								3
		Exit	L	H	L	H	H	H	X			3
					H	X	X	X				3
Bank Active & Row Addr.			H	X	L	L	L	L	V	Row Address (A0~A9, A11,A13)		
Read & Column Address	Auto Precharge		H	X	L	H	L	H	V	L	Column Address	4
	Disable									H		4
Write & Column Address	Auto Precharge Enable		H	X	L	H	L	L	V	L	Column Address	4
	Auto Precharge Disable									H		4.6
Burst Stop	Auto Precharge Enable		H	X	L	H	H	L	X			7
Precharge			H	X	L	L	H	L	V	L	X	
	Bank Selection								X	H		5
Active Power Down	All Banks	Entry	H	L	H	X	X	X	X			
					L	V	V	V				
		Exit	L	H	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X			
					L	H	H	H				
		Exit	L	H	H	X	X	X				
					L	V	V	V				
DM			H			X			X			8
Non Operation (NOP):Not Defined			H	X	H	X	X	X	X			9
					L	H	H	H				9

Notes:

1. *OP Code: Operand Code. A_0~A_{13} & BA_0 ~ BA_1: Program keys (@EMRS/MRS)*
2. *EMRS/MRS can be issued only at all blanks precharge state.*
   A new command can be issued 2 clock cycles after EMRS or MRS.
3. *Auto refresh functions are same as the CBR refresh of DRAM.*
   The automatic precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. *BA_0 ~ BA_1: Bank select addresses.*
   If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank B is selected.
   If BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank C is selected.
   If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
5. *If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 are ignored and all blanks are selected.*
6. *During burst write with auto precharge, new read/write command can not be issued.*
   Another bank read/write command can be issued at tRP after the end of the burst.
7. *Burst stop command is valid at every burst length.*
8. *DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).*
9. *This combination is not defined for any function, which means "No Operation (NOP)" in DDR SDRAM.*

DETAILED TEST CONDITIONS FOR DDR SDRAM IDD1 & IDD7A

IDD1:OPERATING CURRENT:ONE BANK

1. Typical Case : Vdd = 2.5V, T = 25'C
2. Worst Case : Vdd = 2.7V, T = 10'C
3. Only one bank is accessed with tRC (min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle.
   Iout = 0mA
4. Timing patterns
   - 202JD3, DDR200 (100MHz, CL = 2) : tCK = 10ns, CL2, BL = 4, tRCD = 2*tCK, tRAS = 5*tCK
     Read : A0 N R0 N N P0 N A0 N - repeat the same timing with random address changing
     *50% of data changing at every burst

   - 265JD3, DDR266 (133MHz, CL = 2.5) : tCK = 7.5ns, CL = 2.5, BL = 4, tRCD = 3*tCK, tRC = 9*tCK, tRAS = 5*tCK
     Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
     *50% of data changing at every burst

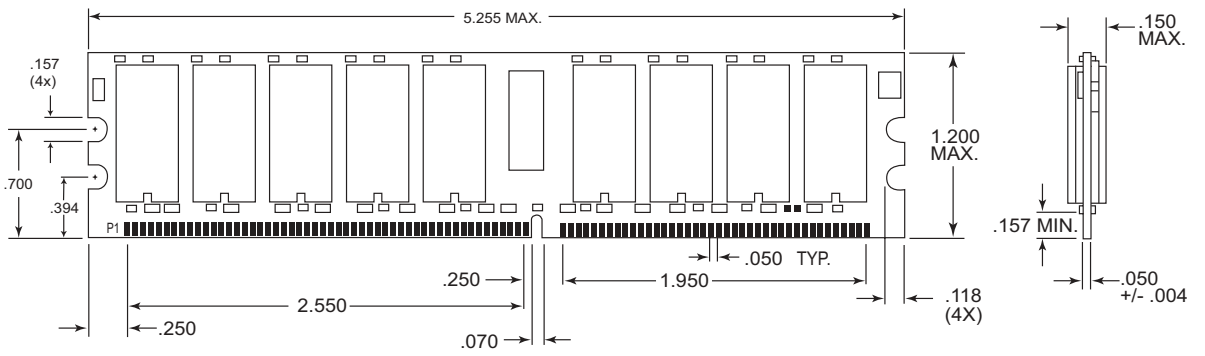
   - 262JD3, DDR266 (133MHz, CL = 2) : tCK = 7.5ns, CL = 2, BL = 4, tRCD = 3*tCK, tRC = 9*tCK, tRAS = 5*tCK
     Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
     *50% of data changing at every burst

ORDERING INFORMATION

Part Number	Density	Speed	Organization	Height
WED3EG72256S202JD3-M	2GB	100MHz/CL=2	256M x 72	1.2 in
WED3EG72256S262JD3-M	2GB	133MHz/CL=2	256M x 72	1.2 in
WED3EG72256S265JD3-M	2GB	133MHz/CL=2.5	256M x 72	1.2 in

M = Micron® Die

PACKAGE DIMENSIONS



All dimensions are in inches.

Document Title

2GB- 256Mx72, ECC, DDR SDRAM DIMM Registered Module

Revision History

Rev #	History	Release Date	Status
Rev 0	Initial Release	January 2004	Advanced