Quad 2-Input Positive OR Gate

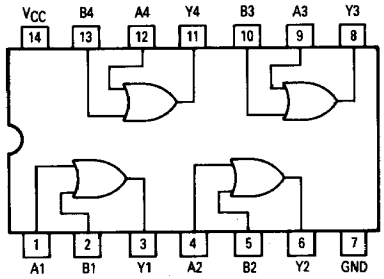
ELECTRICALLY TESTED PER:
MPG54ALS32

AVAILABLE AS:

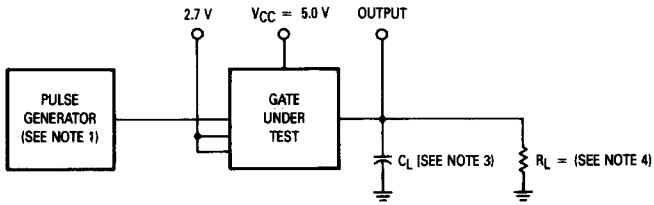
1) JAN: N/A
2) SMD: N/A
3) 883C: 54ALS32/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2

LOGIC DIAGRAM

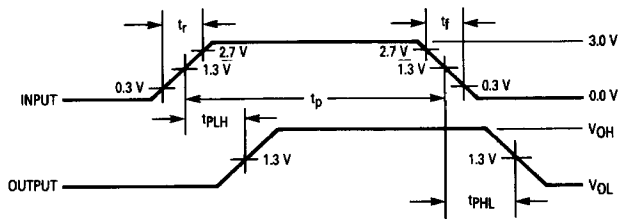


AC TEST CIRCUIT



NOTES:
1. Input pulse has the following characteristics: $t_r = t_f = 6.0 \pm 1.5$ ns, PRR = 1.0 MHz, $Z_{out} \approx 50\ \Omega$.
2. Terminal condition (pins not designated may be high ≥ 2.0 V, low ≤ 0.8 V, or open).
3. $C_L = 50$ pF ± 10%, including scope probe, wiring and jig capacitance, without package in test fixture.
4. $R_L = 499\ \Omega \pm 1.0\%$.
5. Voltage measurements are to be made with respect to network ground terminal.
6. Each gate tested separately.

WAVEFORMS



PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
A1	1	1	2	V_{CC}
B1	2	2	3	V_{CC}
Y1	3	3	4	V_{CC}
A2	4	4	6	V_{CC}
B2	5	5	8	V_{CC}
Y2	6	6	9	V_{CC}
GND	7	7	10	GND
Y3	8	8	12	V_{CC}
A3	9	9	13	V_{CC}
B3	10	10	14	V_{CC}
Y4	11	11	16	V_{CC}
A4	12	12	18	V_{CC}
B4	13	13	19	V_{CC}
V_{CC}	14	14	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

TRUTH TABLE		
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −0.4 mA, V_{IH} = 2.0 V, other input = 0.8 V.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IL} = 0.8 V on both inputs.
V_{IC}	Input Clamping Voltage		−1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other input is open.
I_{IHH}	Logical "1" Input Current		100		100		100	μA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V, other input is open.
I_{IL}	Logical "0" Input Current	0	−100	0	−100	0	−100	μA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other input = 5.5 V.
I_{OS}	Output Short Circuit Current	−30	−112	−30	−112	−30	−112	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (both inputs), V_{OUT} = 2.25 V.
I_{CCH}	Power Supply Current		4.0		4.0		4.0	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V (all inputs).
I_{CCL}	Power Supply Current		4.9		4.9		4.9	mA	V_{CC} = 5.5 V, V_{IN} = GND (all inputs).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
		Subgroup 7		Subgroup 8A		Subgroup 8B			
	Functional Tests								per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Switching Parameters	Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL}	Propagation Delay /Data-Output Output High-Low	3.0	12	3.0	13	3.0	13	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH}	Propagation Delay /Data-Output Output Low-High	3.0	14	3.0	16	3.0	16	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.