REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added case outlines M, N, 4, and 5.	96-10-15	K. A. Cottongim
B	Figure 1; For the case outlines 4 and 5 changed dimension D3 min and max from 1.030 and 1.040 inches to 1.020 and 1.060 inches. Changed dimension A min from .156 inches to .135 inches. Changed dimension L min from .145 inches to .132 inches. -sld	98-07-08	K. A. Cottongim

REV																				
SHEET																				
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31			

REV STATUS OF SHEETS																		
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14				

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Gary Zahn

CHECKED BY
Michael C. Jones

APPROVED BY
Kendall A. Cottongim

DRAWING APPROVAL DATE
95-01-31

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

MICROCIRCUIT, HYBRID, DIGITAL, FLASH, ERASABLE/PROGRAMMABLE READ ONLY MEMORY, 128K x 32-BIT

SIZE	CAGE CODE	
A	**67268**	**5962-94610**

SHEET 1 OF 31

DSCC FORM 2233
APR 97

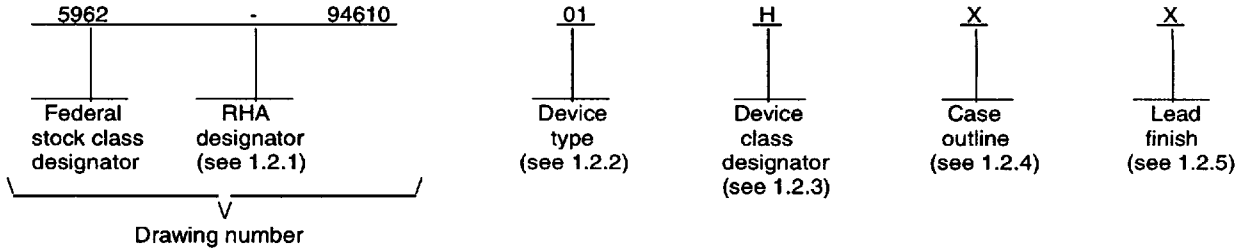
5962-E375-98

9004708 0037963 T69

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes, class D (lowest reliability), class E, (exceptions), class G (lowest high reliability), class H (high reliability), and class K, (highest reliability) and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access Time
01	WF128K32-200HQ	FLASH EPROM, 128K X 32-bit	200 ns
02	WF128K32-150HQ	FLASH EPROM, 128K X 32-bit	150 ns
03	WF128K32-120HQ	FLASH EPROM, 128K X 32-bit	120 ns

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device performance documentation
D, E, G, H or K	Certification and qualification to MIL-PRF-38534

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
M	See figure 1	68	Ceramic, dual cavity, quad pack, lead formed
N	See figure 1	68	Ceramic, single cavity, quad flat pack
W	See figure 1	66	Hex-in-line, single cavity, with standoffs
X	See figure 1	66	Hex-in-line, single cavity, without standoffs
Y	See figure 1	66	Hex-in-line, single cavity, with standoffs
Z	See figure 1	66	Hex-in-line, single cavity, without standoffs
4	See figure 1	66	1.075", hex-in-line, single cavity, with standoffs
5	See figure 1	66	1.075", hex-in-line, single cavity, with standoffs

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) 2/	-2.0 V dc to +7.0 V dc
Signal Voltage range (any pin except A9) 2/	-2.0 V dc to +7.0 V dc
Power dissipation (P_D)	2.2 W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300 °C
Thermal resistance junction-to-case (θ_{JC}):	
Case outlines W, X, Y, Z, 4, and 5	7.8°C/W
Case outline M	11.3°C/W
Case outline N	1.7°C/W
Data retention	10 years minimum
Endurance (write/erase cycles)	10,000 cycles minimum
V_{PP} supply voltage (with respect to ground) 3/	-2.0 V dc to +14.0 V dc

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input low voltage range (V_{IL})	-0.5 V dc to +0.8 V dc
Input high voltage range (V_{IH})	+2.0 V dc to V_{CC} + 0.3 V dc
V_{PP} high voltage (V_{PPH})	+11.4 V dc to +12.6 V dc
V_{PP} low voltage (V_{PPL})	0 V dc to 6.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbook. The following specification, standards, and handbook form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Minimum DC voltage on input or I/O pins is -0.5 V dc. During voltage transitions, inputs may undershoot GND to -2.0 V dc for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V dc. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V dc for periods up to 20 ns.

3/ Minimum DC input voltage on A9 pin is -0.5 V dc. During voltage transitions, A9 may undershoot GND to -2.0 V dc for periods up to 20 ns. Maximum DC input voltage on A9 is +13.5 V dc which may overshoot to +14.0 V dc for periods up to 20 ns.

HANDBOOK

DEPARTMENT OF DEFENSE

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbook are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. Therefore, the tests and inspections herein may not be performed for the applicable device class (see MIL-PRF-38534). Futhermore, the manufacturers may take exceptions or use alternate methods to the tests and inspections herein and not perform them. However, the performance requirements as defined in MIL-PRF-38534 shall be met for the appilcable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Timing diagram(s). The timing diagram(s) shall be as specified on figure 4, 5, and 6.

3.2.5 Block diagram. The block diagram shall be as specified on figure 7.

3.2.6 Output load circuit. The output load circuit shall be as specified on figure 8.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Programming procedure. The programming procedure shall be as specified by the manufacturer and shall be available on request.

3.6 Marking of Device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked as listed in QML-38534.

3.7 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.8 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.9 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

3.10 Endurance. A reprogrammability test shall be completed as part of the vendors's reliability monitors. The reprogrammability test shall be done for the initial characterization and after any design process changes whichmay affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase endurance cycles listed in section 1.3 herein over the full military temperature range. The vendors procedure shall be kept under document control and shall be made available upon request of the acquiring of preparing activity.

3.11 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DC parameters							
Supply current, static	I_{CCS}	$\overline{CS} = V_{IH}$, $\overline{OE} = V_{IH}$, V_{CC} = 5.5 V dc	1,2,3	All		1.0	mA
Supply current, 32-bit mode	I_{CC32}	$\overline{CS} = V_{IL}$, $\overline{OE} = V_{IH}$, V_{CC} = 5.5 V dc, f = 5 MHz	1,2,3	All		120	mA
Standby current	I_{SB}	$\overline{CS} = V_{IH}$, $\overline{OE} = V_{IH}$, V_{CC} = 5.5 V dc, f = 5 MHz	1,2,3	All		6.5	mA
Input leakage current	I_{LI}	V_{IN} = GND or V_{CC}, V_{CC} = 5.5 V dc	1,2,3	All		10	µA
Output leakage current	I_{LO}	$\overline{CS} = V_{IH}$, $\overline{OE} = V_{IH}$, V_{OUT} = GND or V_{CC}, V_{CC} = 5.5 V dc	1,2,3	All		10	µA
Output low voltage	V_{OL}	V_{CC} = 4.5 V dc, I_{OL} = 2.1 mA	1,2,3	All		0.45	V
Output high voltage	V_{OH}	V_{CC} = 4.5 V dc I_{OH} = -2.5 mA	1,2,3	All	2.4		V
V_{CC} program current	I_{CC2}	$V_{PP} = V_{PPH}$ = 12.6 V	1,2,3	All		120	mA
V_{CC} erase current	I_{CC3}	$V_{PP} = V_{PPH}$ = 12.6 V	1,2,3	All		120	mA
V_{PP} program current	I_{PP2}	$V_{PP} = V_{PPH}$ = 12.6 V	1,2,3	All		120	mA
V_{PP} erase current	I_{PP3}	$V_{PP} = V_{PPH}$ = 12.6 V	1,2,3	All		120	mA
V_{PP} read current	I_{PPRx32}	$V_{PP} = V_{PPH}$ = 12.6 V	1,2,3	All		800	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic characteristics							
$\overline{OE}$ capacitance 2/	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz, T_A = +25°C	4	All		50	pF
A0-16 capacitance 2/	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz, T_A = +25°C	4	All		50	pF
$\overline{CS}$ 1-4 capacitance 2/	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz, T_A = +25°C	4	All		20	pF
$\overline{WE}$ capacitance 2/	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz, T_A = +25°C, case outline N only	4	All		50	pF
WE 1-4 capacitance 2/	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz, T_A = +25°C, case outlines M,W,X,Y,and Z	4	All		20	pF
I/O0-I/O31 capacitance 2/	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz T_A = +25°C	4	All		20	pF
Functional testing							
Functional tests		See 4.3.1c	7,8A,8B	All			
Read cycle AC timing characteristics							
Read cycle time 3/	t_{RC}	See figure 4	9,10,11	01 02 03	200 150 120		ns
Address access time	t_{ACC}	See figure 4	9,10,11	01 02 03		200 150 120	ns
Output hold from address change	t_{OH}	See figure 4	9,10,11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read cycle AC timing - Continued.							
Chip select access time	t_{CS}	See figure 4	9,10,11	01 02 03		200 150 120	ns
Output enable access time	t_{OE}	See figure 4	9,10,11	01 02 03		75 65 60	ns
Chip select to output in low impedance 3/	t_{LZ}	See figure 4	9,10,11	All	0		ns
Output enable to output in low impedence 3/	t_{OLZ}	See figure 4	9,10,11	All	0		ns
Output enable to output in high impedence 3/	t_{DF}	See figure 4	9,10,11	01 02 03		40 35 30	ns
Write cycle AC timing - Write/Erase/Program operations							
Write cycle time 3/	t_{WC}	See figures 5 and 6	9,10,11	01 02 03	200 150 120		ns
Chip select setup time	t_{CS}	See figures 5 and 6	9,10,11	All	20		ns
Chip select hold time	t_{CH}	See figures 5 and 6	9,10,11	All	0		ns
Data setup time	t_{DS}	See figures 5 and 6	9,10,11	All	50		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write cycle AC timing - Write/Erase/Program operations - Continued.							
Address setup time	t_{AS}	See figures 5 and 6	9,10,11	All	0		ns
Write pulse width	t_{WP}	See figures 5 and 6	9,10,11	All	80		ns
Write enable pulse width high	t_{WPH}	See figures 5 and 6	9,10,11	All	20		ns
Address hold time	t_{AH}	See figures 5 and 6	9,10,11	01	75		ns
				02,03	60		
Write recovery before read	t_{WHGL}	See figures 5 and 6 3/	9,10,11	All	6		µs
Data hold time	t_{DH}	See figures 5 and 6	9,10,11	01	15		ns
				02,03	10		

1/ Unless otherwise specified, $4.5 V \le V_{CC} \le 5.5 V$ and $V_{SS} = 0 V$.
2/ Unless otherwise specified, the DC test conditions are as follows:
Input pulse levels: $V_{IH} = V_{CC} - 0.3 V$ and $V_{IL} = 0.3 V$.
Unless otherwise specified, the AC test conditions are as follows:
Input pulse Levels: $V_{IL} = 0 V$ and $V_{IH} = 3.0 V$.
Input rise and fall times: 5 nanoseconds.
Input and output timing reference levels: 1.5 V.
3/ Guaranteed by design, but not tested.

Case outline M.

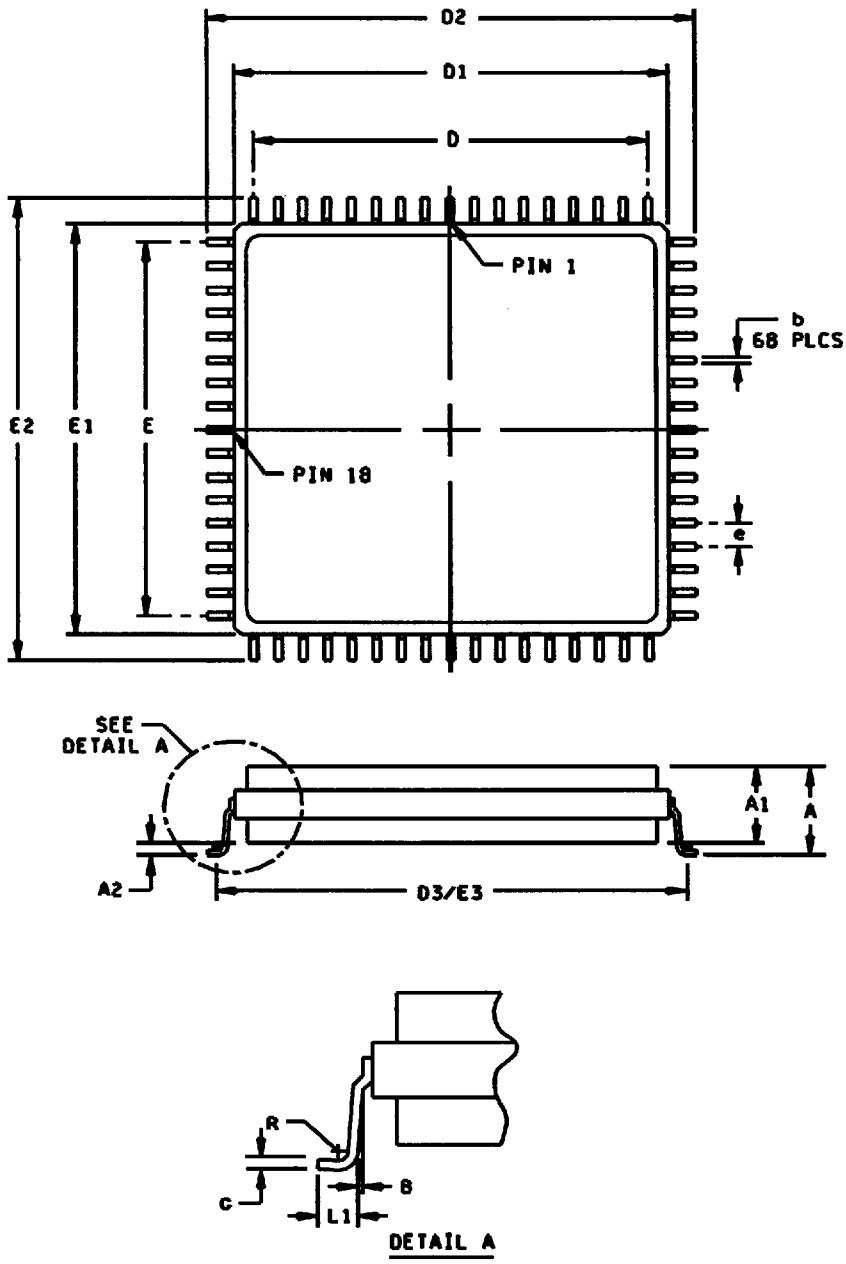


FIGURE 1. Case outline(s).

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-94610
		REVISION LEVEL B	SHEET 10

DSCC FORM 2234
APR 97

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	4.01	5.10	0.158	0.200
A1	3.91	4.72	0.154	0.186
A2	0.24	0.38	0.005	0.015
b	0.33	0.43	0.013	0.017
B	0.25 REF		.010 REF	
C	0.23	0.31	0.009	0.012
D/E	20.3 BSC		0.800 BSC	
D1/E1	22.10	22.65	0.870	0.890
D2/E2	24.89	25.35	0.980	1.000
D3/E3	23.75	24.28	0.936	0.956
e	1.27 BSC		0.050 BSC	
R	0.13		0.005	
L1	0.89	1.14	0.035	0.045

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.
3. Case outline M is a dual cavity package.

FIGURE 1. Case outline(s) - Continued.

Case outline N.

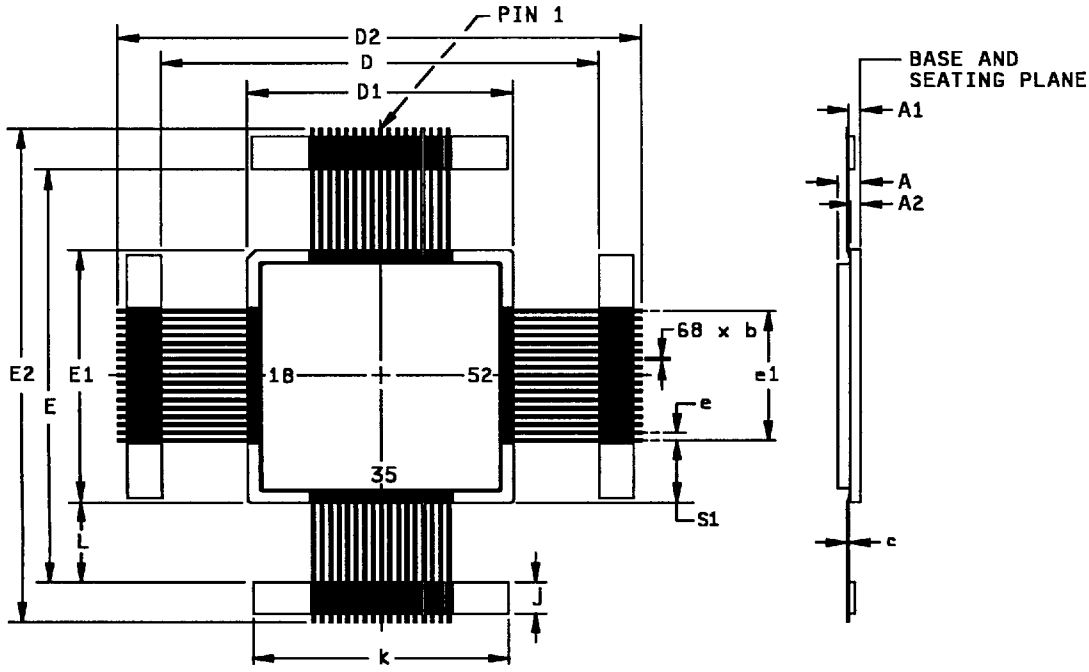


FIGURE 1. Case outline(s) - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE **A**		**5962-94610**
		REVISION LEVEL **B**	SHEET **12**

DSCC FORM 2234
APR 97

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	4.46	5.10	0.175	0.200
A1	1.40	1.65	0.055	0.065
A2	1.14	1.40	0.045	0.055
b	0.30	0.46	0.012	0.018
C	0.23	0.31	0.009	0.012
D/E	63.63	66.42	2.505	2.615
D1/E1	39.24	40.01	1.545	1.575
D2/E2	73.28	84.20	2.885	3.315
e	1.14	1.40	0.045	0.055
e1	20.19	20.45	0.795	0.805
j	4.83	5.33	0.190	0.210
k	37.72	38.48	1.485	1.515
L	12.19	13.21	0.480	0.520
S1	9.45	9.86	0.372	0.388

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

Case outlines W,Y,4,5.

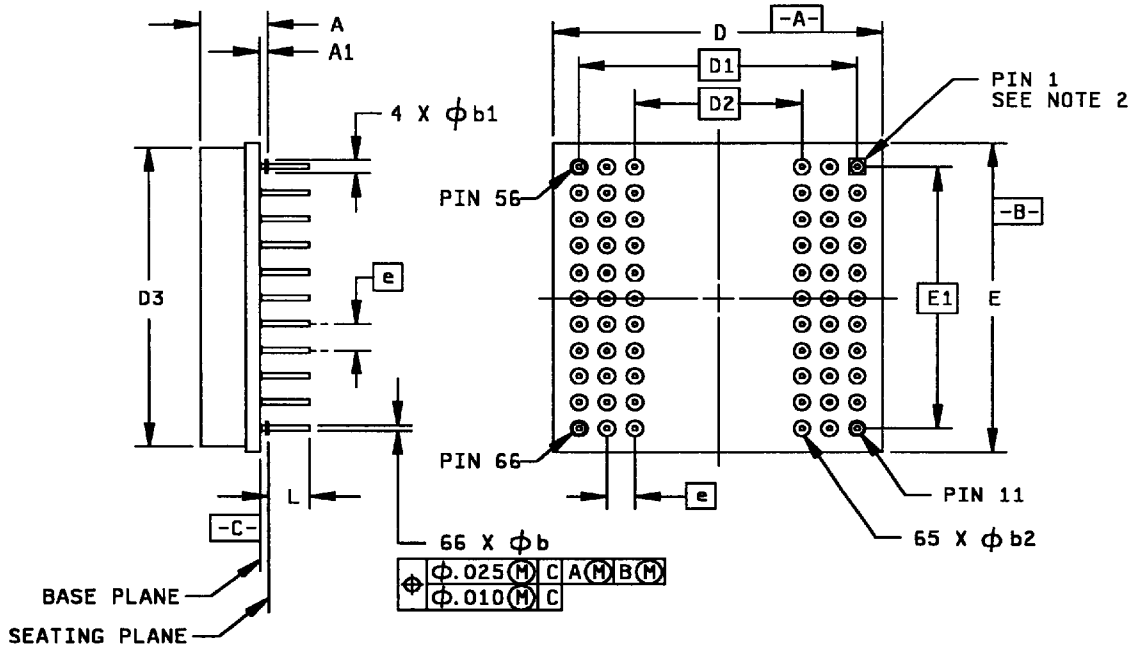


FIGURE 1. Case outline(s) - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE **A**		**5962-94610**
		REVISION LEVEL **B**	SHEET **14**

DSCC FORM 2234
APR 97

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	5.08	6.22	0.200	0.245
A1	0.64	0.89	0.025	0.035
øb	0.41	0.51	0.016	0.020
øb1	1.14	1.40	0.045	0.055
øb2	1.65	1.91	0.065	0.075
D/E	29.72	30.48	1.170	1.200
D1/E1	25.40 BSC		1.000 BSC	
D2	15.24 BSC		0.600 BSC	
D3	28.96	29.21	1.140	1.150
e	2.54 BSC		0.100 BSC	
L	3.68	3.94	0.145	0.155

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin 1 is identified by 0.070 square pad.
3. Pin numbers are for reference only.

FIGURE 1. Case outlines(s) - Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.43	4.34	0.135	0.181
A1	0.64	0.89	0.025	0.035
øb	0.41	0.51	0.016	0.020
øb1	1.14	1.40	0.045	0.055
øb2	1.65	1.91	0.065	0.075
D/E	27.05	27.56	1.065	1.085
D1/E1	25.40 BSC		1.000 BSC	
D2	15.24 BSC		0.600 BSC	
D3	25.91	26.92	1.020	1.060
e	2.54 BSC		0.100 BSC	
L	3.35	3.94	0.132	0.155

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin 1 is identified by 0.070 square pad.
3. Pin numbers are for reference only.

FIGURE 1. Case outlines(s) - Continued.

Case outlines X,Z.

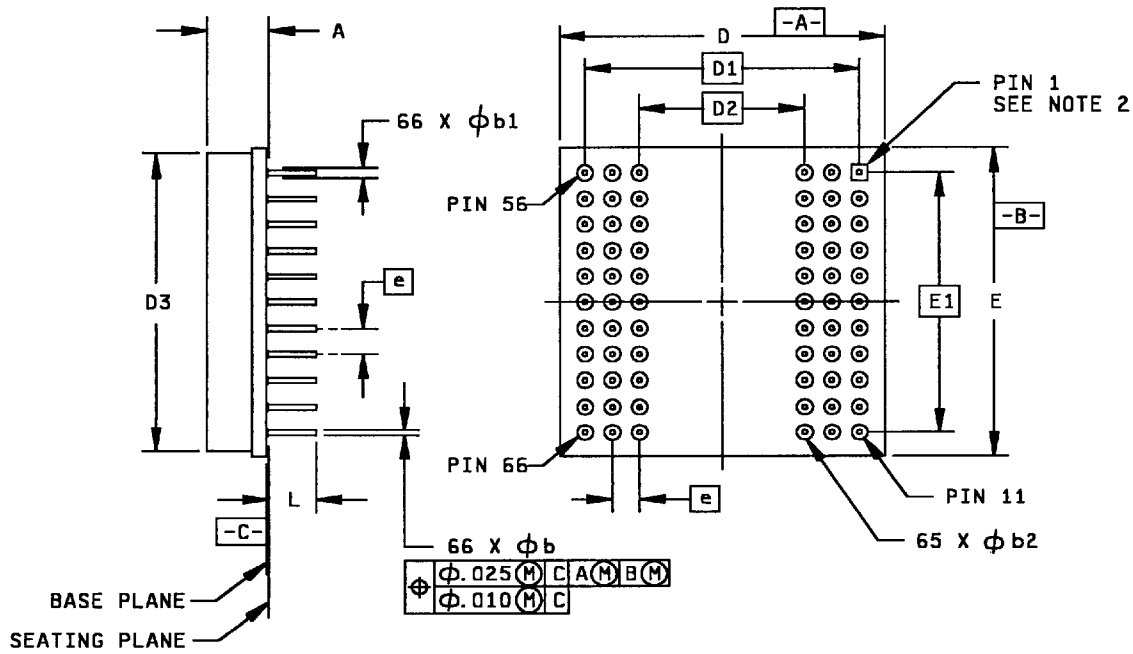


FIGURE 1. Case outline(s) - Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	4.69	5.84	0.185	0.230
øb	0.41	0.51	0.016	0.020
øb1	0.76 Ref.		0.030 Ref.	
øb2	1.65	1.91	0.065	0.075
D/E	29.72	30.48	1.170	1.200
D1/E1	25.40 BSC		1.000 BSC	
D2	15.24 BSC		0.600 BSC	
D3	28.96	29.21	1.140	1.150
e	2.54 BSC		0.100 BSC	
L	4.19	4.69	0.165	0.185

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin 1 is identified by 0.070 square pad.
3. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

Device types	All	Device types	All	Device types	All	Device types	All
Case outlines	M	Case outlines	M	Case outlines	M	Case outlines	M
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CS3}$	19	I/O8	36	$\overline{CS2}$	53	I/O23
3	A5	20	I/O9	37	NC	54	I/O22
4	A4	21	I/O10	38	$\overline{WE2}$	55	I/O21
5	A3	22	I/O11	39	$\overline{WE3}$	56	I/O20
6	A2	23	I/O12	40	$\overline{WE4}$	57	I/O19
7	A1	24	I/O13	41	NC	58	I/O18
8	A0	25	I/O14	42	NC	59	I/O17
9	NC	26	I/O15	43	V_{PP}	60	I/O16
10	I/O0	27	V_{CC}	44	I/O31	61	V_{CC}
11	I/O1	28	A11	45	I/O30	62	A10
12	I/O2	29	A12	46	I/O29	63	A9
13	I/O3	30	A13	47	I/O28	64	A8
14	I/O4	31	A14	48	I/O27	65	A7
15	I/O5	32	A15	49	I/O26	66	A6
16	I/O6	33	A16	50	I/O25	67	$\overline{WE1}$
17	I/O7	34	$\overline{CS1}$	51	I/O24	68	$\overline{CS4}$

FIGURE 2. Terminal connections.

Device types	All	Device types	All	Device types	All	Device types	All
Case outline	N	Case outline	N	Case outline	N	Case outline	N
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CS1}$	19	I/O8	36	$\overline{CS4}$	53	I/O23
3	A5	20	I/O9	37	NC	54	I/O22
4	A4	21	I/O10	38	NC	55	I/O21
5	A3	22	I/O11	39	NC	56	I/O20
6	A2	23	I/O12	40	NC	57	I/O19
7	A1	24	I/O13	41	NC	58	I/O18
8	A0	25	I/O14	42	NC	59	I/O17
9	NC	26	I/O15	43	V_{PP}	60	I/O16
10	I/O0	27	V_{CC}	44	I/O31	61	V_{CC}
11	I/O1	28	A11	45	I/O30	62	A10
12	I/O2	29	A12	46	I/O29	63	A9
13	I/O3	3	A13	47	I/O28	64	A8
14	I/O4	31	A14	48	I/O27	65	A7
15	I/O5	32	A15	49	I/O26	66	A6
16	I/O6	33	A16	50	I/O25	67	$\overline{WE}$
17	I/O7	34	$\overline{CS2}$	51	I/O24	68	$\overline{CS3}$

FIGURE 2. Terminal connections - Continued.

Device type	All	Device type	All	Device type	All	Device type	All
Case outlines	W,X,4	Case outlines	W,X,4	Case outlines	W,X,4	Case outlines	W,X,4
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	I/O8	18	A15	35	I/O25	52	$\overline{WE3}$
2	I/O9	19	V_{CC}	36	I/O26	53	$\overline{CS3}$
3	I/O10	20	$\overline{CS1}$	37	A7	54	GND
4	A14	21	NC	38	A12	55	I/O19
5	A16	22	I/03	39	V_{PP}	56	I/O31
6	A11	23	I/015	40	A13	57	I/O30
7	A0	24	I/O14	41	A8	58	I/O29
8	NC	25	I/O13	42	I/O16	59	I/O28
9	I/O0	26	I/O12	43	I/O17	60	A1
10	I/O1	27	$\overline{OE}$	44	I/O18	61	A2
11	I/O2	28	NC	45	V_{CC}	62	A3
12	$\overline{WE2}$	29	$\overline{WE1}$	46	$\overline{CS4}$	63	I/O23
13	$\overline{CS2}$	30	I/O7	47	$\overline{WE4}$	64	I/O22
14	GND	31	I/O6	48	I/O27	65	I/O21
15	I/O11	32	I/O5	49	A4	66	I/O20
16	A10	33	I/O4	50	A5		
17	A9	34	I/O24	51	A6		

FIGURE 2. Terminal connections (industrial pin-outs) - Continued.

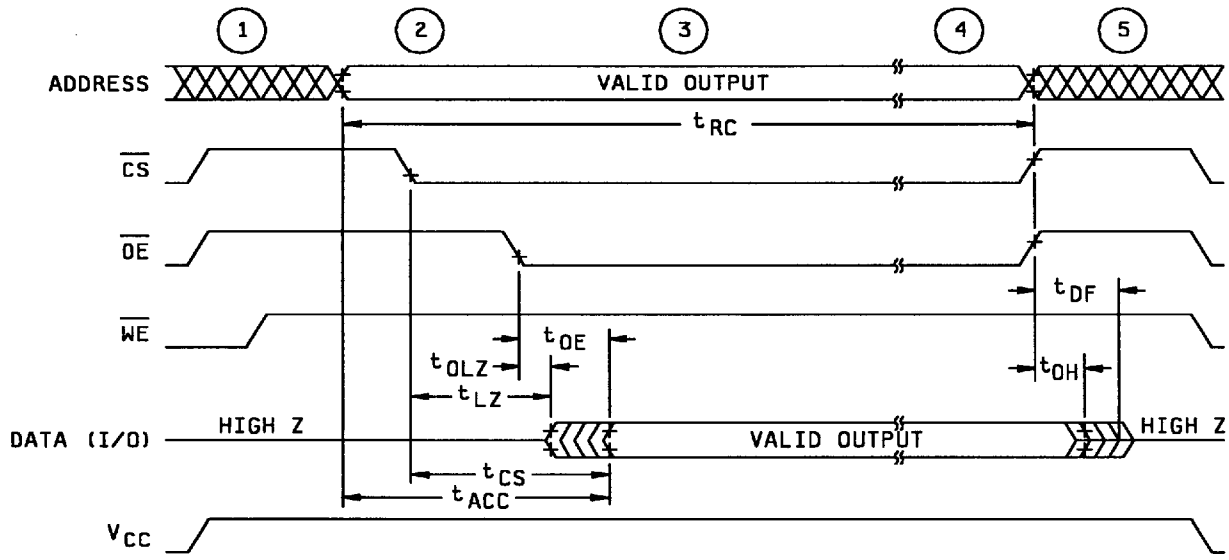
Device type	All	Device type	All	Device type	All	Device type	All
Case outlines	Y,Z,5	Case outlines	Y,Z,5	Case outlines	Y,Z,5	Case outlines	Y,Z,5
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	I/O8	18	A12	35	I/O25	52	$\overline{WE3}$
2	I/O9	19	V_{CC}	36	I/O26	53	$\overline{CS3}$
3	I/O10	20	$\overline{CS1}$	37	A6	54	GND
4	A13	21	NC	38	A7	55	I/O19
5	A14	22	I/03	39	V_{PP}	56	I/O31
6	A15	23	I/015	40	A8	57	I/O30
7	A16	24	I/O14	41	A9	58	I/O29
8	NC	25	I/O13	42	I/O16	59	I/O28
9	I/O0	26	I/O12	43	I/O17	60	A0
10	I/O1	27	$\overline{OE}$	44	I/O18	61	A1
11	I/O2	28	NC	45	V_{CC}	62	A2
12	$\overline{WE2}$	29	$\overline{WE1}$	46	$\overline{CS4}$	63	I/O23
13	$\overline{CS2}$	30	I/O7	47	$\overline{WE4}$	64	I/O22
14	GND	31	I/O6	48	I/O27	65	I/O21
15	I/O11	32	I/O5	49	A3	66	I/O20
16	A10	33	I/O4	50	A4		
17	A11	34	I/O24	51	A5		

FIGURE 2. Terminal connections (alternative pin-outs) - Continued.

Operation	Pins	V_{PP} 1/	A0	A9	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ0-DQ7
Read-only	Read	V_{PPL}	A0	A9	V_{IL}	V_{IL}	V_{IH}	Data Out
	Output Disable	V_{PPL}	X	X	V_{IL}	V_{IH}	V_{IH}	High Z
	Standby	V_{PPL}	X	X	V_{IH}	X	X	High Z
Read/Write	Read	V_{PPH}	A0	A9	V_{IL}	V_{IL}	V_{IH}	Data 2/ Out
	Output Disable	V_{PPH}	X	X	V_{IL}	V_{IH}	V_{IH}	High Z
	Standby 3/	V_{PPH}	X	X	V_{IH}	X	X	High Z
	Write	V_{PPH}	A0	A9	V_{IL}	V_{IH}	V_{IL}	Data In

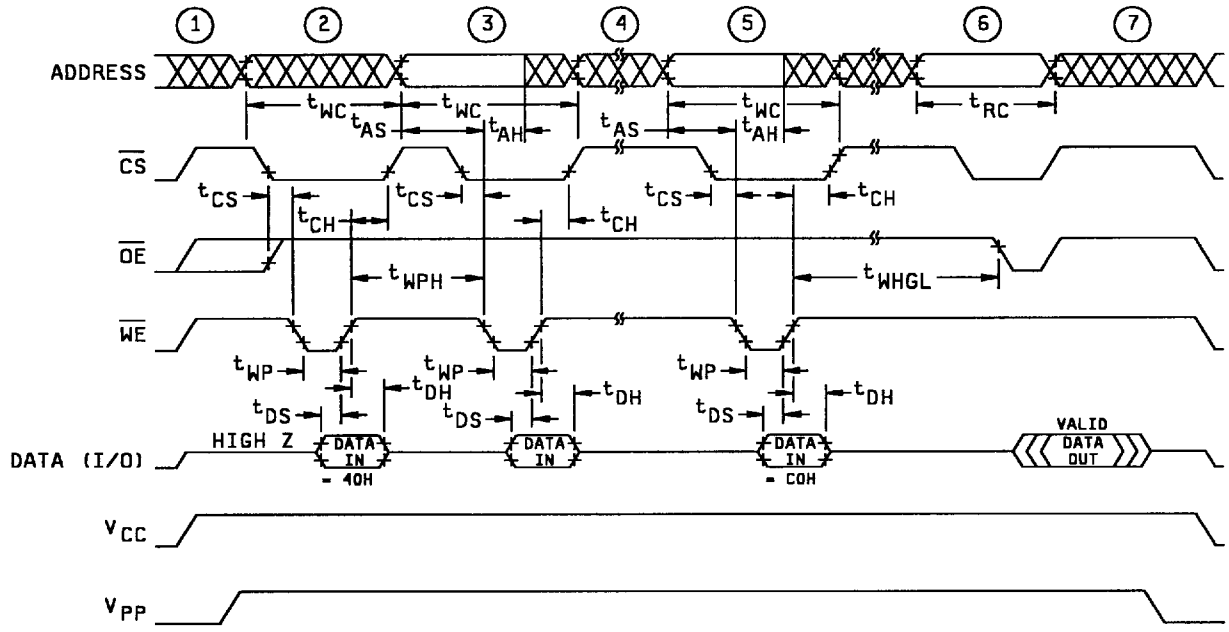
NOTES:
1. Refer to DC characteristics. When $V_{PP} = V_{PPL}$ memory contents can be read but not written or erased.
2. Read operations with $V_{PP} = V_{PPH}$ may access array data.
3. With V_{PP} at high voltage, the standby current equals $I_{CC} + I_{PP}$ (standby).
4. X can be V_{IL} or V_{IH}.

FIGURE 3. Truth table.



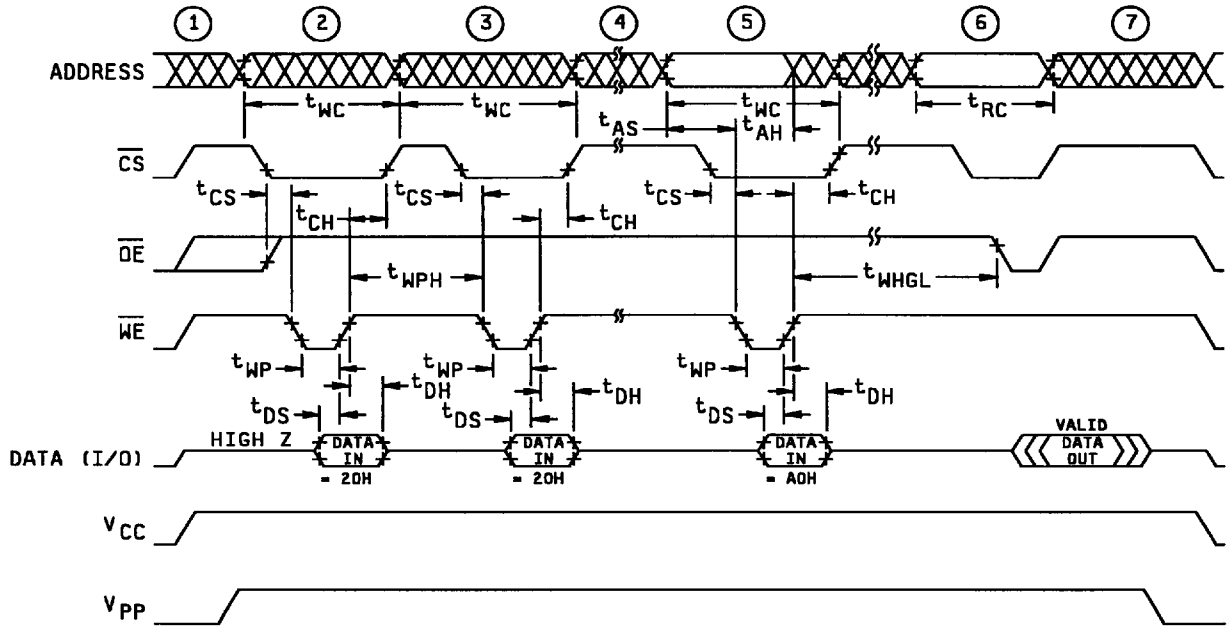
NOTES:
1. V_{CC} power-up and standby.
2. Device and address selection.
3. Outpus enabled.
4. Data valid.
5. Standby / V_{CC} power-down

FIGURE 4. AC waveforms for read operations.



NOTES:
1. V_{CC} power-up and standby.
2. Set-up erase command.
3. Program command latch address and data.
4. Programming.
5. Program verify command.
6. Program verification.
7. Standby / V_{CC} power-down

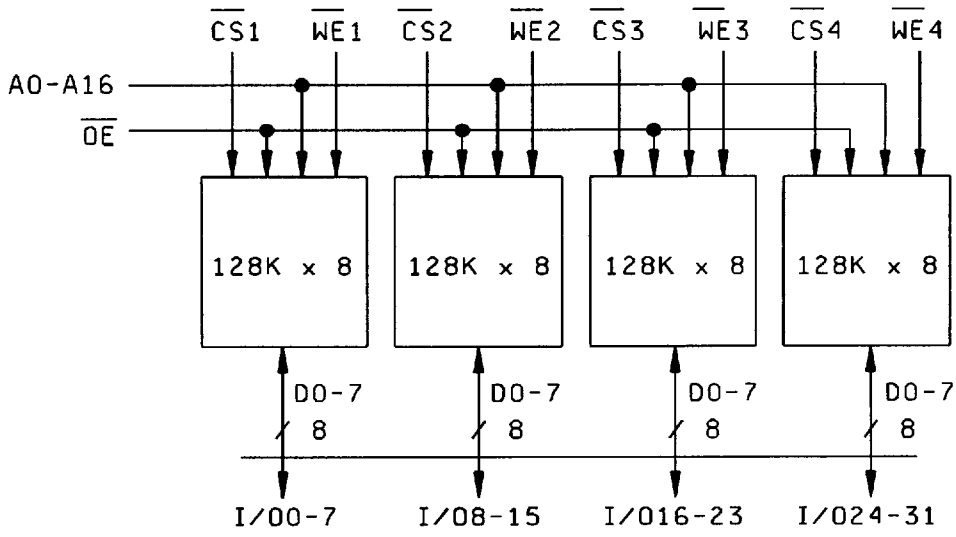
FIGURE 5. Program operations.



NOTES:
1. V_{CC} power-up and standby.
2. Set-up erase command.
3. Erase command.
4. Erasing.
5. Erase verify command.
6. Erase verification.
7. Standby / V_{CC} power-down

FIGURE 6. Erase operations.

Case outlines M, W, X, Y, Z, 4, and 5.



Case outline N.

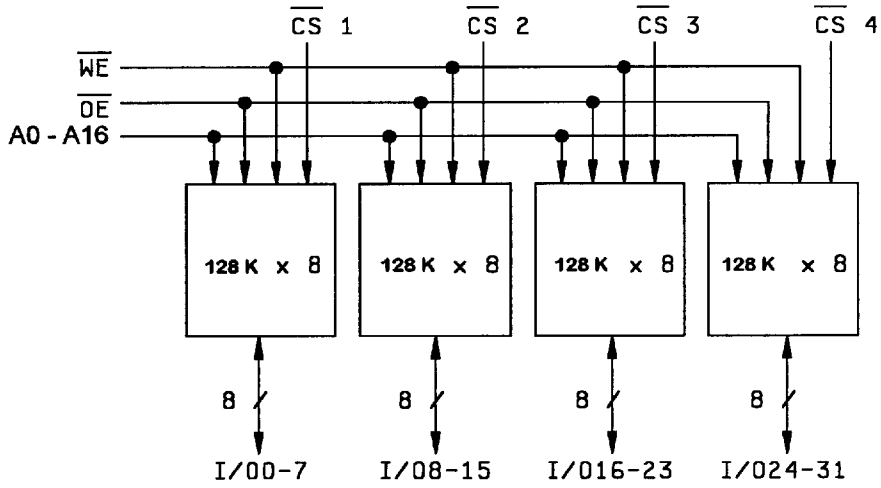
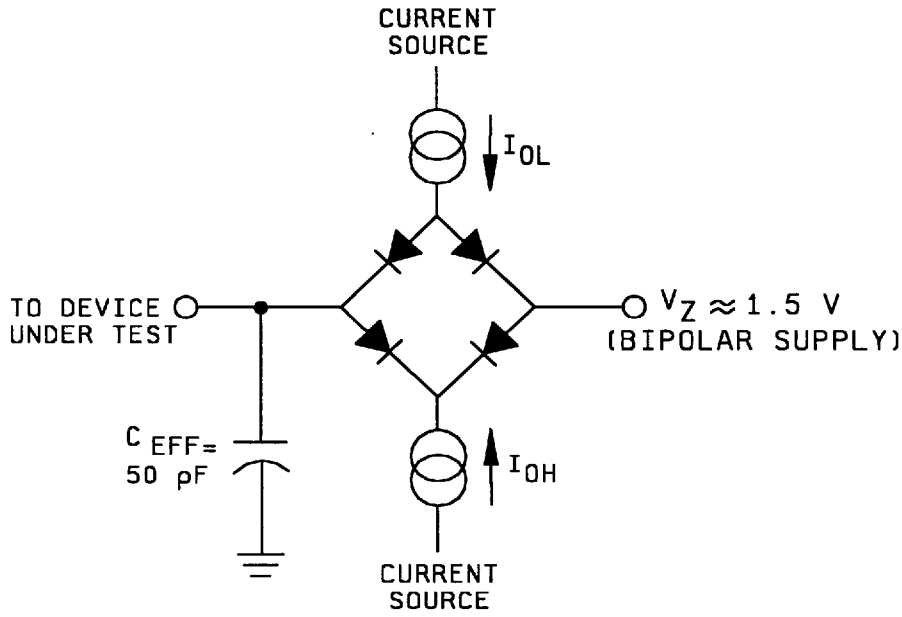


FIGURE 7. Block diagram(s).



NOTES:

1. V_Z is programmable from -2 V to +7 V.
2. I_{OL} & I_{OH} are programmable from 0 to 16 mA.
3. Tester impedance (Z0) = 75 ohms.
4. V_Z is typically the midpoint of V_{OH} and V_{OL}.
5. I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
6. ATE tester includes jig capacitance.

FIGURE 8. Output test circuit.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534,group A test table)
Interim electrical parameters	1,4,7,9
Final electrical test parameters	1*,2,3,4,7,8A,8B,9,10,11
Group A test requirements	1,2,3,4,7,8A,8B,9,10,11
Group C end-point electrical parameters	1,2,3,4,7,8A,8B,9,10,11
MIL-STD-883, group E end-point electrical parameters for RHA devices	Subgroups ** (in accordance with method 5005, group A test table)

* PDA applies to subgroup 1.
** When applicable to this standard microcircuit drawing, the subgroups shall be defined.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 shall be omitted.

c. Subgroups 7, 8A, and 8B shall include verification of the truth table.

d. The following data patterns shall be verified during subgroups 7, 8A, and 8B:

(1) 0's to all memory cell locations.

(2) Checkerboard pattern to entire memory array.

(3) Checkerboard compliment to entire memory array.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

(4) The checkerboard data pattern shall be verified after burn-in as part of end-point electrical testing.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels shall be M, D, R, and H. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for levels M, D, R, and H shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table II herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.

d. The devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38534 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

f. For device classes H and K, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0526.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0512.

6.6 Sources of supply. Sources of supply are listed in QML-38534. The vendors listed in QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 98-07-08

Approved sources of supply for SMD 5962-94610 are listed below for immediate acquisition only and shall be added to QML-38534 during the next revision. QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38534.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9461001HMA	54230	WF128K32-200G2Q
5962-9461001HMC	54230	WF128K32-200G2Q
5962-9461001HNC	54230	WF128K32-200G4Q
5962-9461001HWA	54230	WF128K32N-200HQ
5962-9461001HWC	54230	WF128K32N-200HQ
5962-9461001HXA	54230	WF128K32N-200HSQ
5962-9461001HXC	54230	WF128K32N-200HSQ
5962-9461001HYA	54230	WF128K32NA-200HQ
5962-9461001HYC	54230	WF128K32NA-200HQ
5962-9461001HZA	54230	WF128K32NA-200HSQ
5962-9461001HZC	54230	WF128K32NA-200HSQ
5962-9461001H4A	54230	WF128K32N-200H1Q
5962-9461001H4C	54230	WF128K32N-200H1Q
5962-9461001H5A	54230	WF128K32NA-200H1Q
5962-9461001H5C	54230	WF128K32NA-200H1Q
5962-9461002HMA	54230	WF128K32-150G2Q
5962-9461002HMC	54230	WF128K32-150G2Q
5962-9461002HNC	54230	WF128K32-150G4Q
5962-9461002HWA	54230	WF128K32N-150HQ
5962-9461002HWC	54230	WF128K32N-150HQ
5962-9461002HXA	54230	WF128K32N-150HSQ
5962-9461002HXC	54230	WF128K32N-150HSQ
5962-9461002HYA	54230	WF128K32NA-150HQ
5962-9461002HYC	54230	WF128K32NA-150HQ
5962-9461002HZA	54230	WF128K32NA-150HSQ
5962-9461002HZC	54230	WF128K32NA-150HSQ
5962-9461002H4A	54230	WF128K32N-150H1Q
5962-9461002H4C	54230	WF128K32N-150H1Q
5962-9461002H5A	54230	WF128K32NA-150H1Q
5962-9461002H5C	54230	WF128K32NA-150H1Q

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9461003HMA	54230	WF128K32-120G2Q
5962-9461003HMC	54230	WF128K32-120G2Q
5962-9461003HNC	54230	WF128K32-120G4Q
5962-9461003HWA	54230	WF128K32N-120HQ
5962-9461003HWC	54230	WF128K32N-120HQ
5962-9461003HXA	54230	WF128K32N-120HSQ
5962-9461003HXC	54230	WF128K32N-120HSQ
5962-9461003HYA	54230	WF128K32NA-120HQ
5962-9461003HYC	54230	WF128K32NA-120HQ
5962-9461003HZA	54230	WF128K32NA-120HSQ
5962-9461003HZC	54230	WF128K32NA-120HSQ
5962-9461003H4A	54230	WF128K32N-120H1Q
5962-9461003H4C	54230	WF128K32N-120H1Q
5962-9461003H5A	54230	WF128K32NA-120H1Q
5962-9461003H5C	54230	WF128K32NA-120H1Q

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availibility.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
54230	White Microelectronics 3601 East University Drive Phoenix, AZ 85034

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.