

74HC3G07; 74HCT3G07

Triple buffer with open-drain outputs

Rev. 02 — 12 May 2009

Product data sheet

1. General description

The 74HC3G07 and 74HCT3G07 are high-speed Si-gate CMOS devices. They provide three buffers with open-drain outputs.

The outputs of the 74HC3G07 and 74HCT3G07 devices are open drains and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions. For digital operation this device must have a pull-up resistor to establish a logic HIGH-level.

The HC device has CMOS input switching levels and supply voltage range 2 V to 6 V.

The HCT device has TTL input switching levels and supply voltage range 4.5 V to 5.5 V.

2. Features

- Wide supply voltage range from 2.0 V to 6.0 V
- High noise immunity
- Low power dissipation
- Multiple package options
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC3G07DP 74HCT3G07DP	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74HC3G07DC 74HCT3G07DC	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74HC3G07GD 74HCT3G07GD	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	XSON8U	plastic extremely thin small outline package; no leads; 8 terminals; UTLP based; body $3 \times 2 \times 0.5$ mm	SOT996-2

4. Marking

Table 2. Marking code

Type number	Marking code
74HC3G07DP	H07
74HCT3G07DP	T07
74HC3G07DC	H07
74HCT3G07DC	T07
74HC3G07GD	H07
74HCT3G07GD	T07

5. Functional diagram

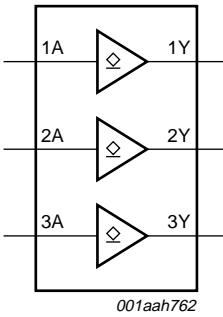


Fig 1. Logic symbol

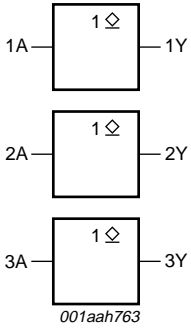


Fig 2. IEC logic symbol

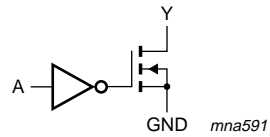


Fig 3. Logic diagram (one buffer)

6. Pinning information

6.1 Pinning

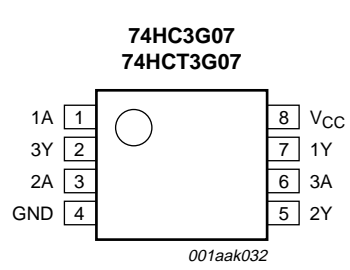


Fig 4. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)

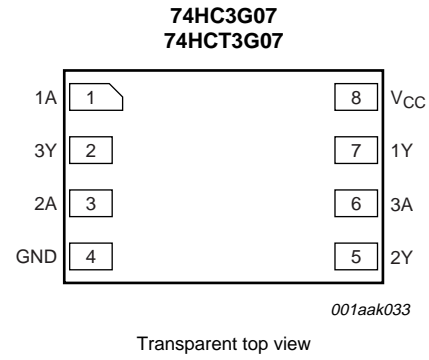


Fig 5. Pin configuration SOT996-2 (XSON8U)

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A, 3A	1, 3, 6	data input
GND	4	ground (0 V)
1Y, 2Y, 3Y	7, 5, 2	data output
V _{CC}	8	supply voltage

7. Functional description

Table 4. Function table^[1]

Input nA	Output nY
L	L
H	Z

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	7.0	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	[1] -	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V	[1] -20	-	mA
V _O	output voltage	active mode	[1] -0.5	V _{CC} + 0.5	V
		high-impedance mode	[1] -0.5	7.0	V
I _O	output current	V _O = -0.5 V to 7.0 V	[1] -25	-	mA
I _{CC}	supply current		[1] -	50	mA
I _{GND}	ground current		[1] -50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _D	dynamic power dissipation	T _{amb} = -40 °C to +125 °C	[2] -	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.
 For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K.
 For XSON8U package: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC3G07			74HCT3G07			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	6.0	0	-	5.5	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V). All typical values are measured at T_{amb} = 25 °C.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
74HC3G07								
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1.0	μA
I _{LO}	output leakage current	V _I = V _{IH} ; V _O = V _{CC} or GND	-	-	±5.0	-	±10	μA
I _{CC}	supply current	per input pin; V _{CC} = 6.0 V; V _I = V _{CC} or GND; I _O = 0 A;	-	-	10	-	20	μA
C _I	input capacitance		-	1.5	-	-	-	pF

Table 7. Static characteristics ...continued

Voltages are referenced to GND (ground = 0 V). All typical values are measured at $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
74HCT3G07								
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	2.0	1.6	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	1.2	0.8	-	0.8	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 4.5\text{ V}$	-	0	0.1	-	0.1	V
		$I_O = 4.0\text{ mA}; V_{CC} = 4.5\text{ V}$	-	0.15	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5\text{ V}$	-	-	± 1.0	-	± 1.0	μA
I_{LO}	output leakage current	$V_I = V_{IH}; V_O = V_{CC}$ or GND	-	-	± 5.0	-	± 10	μA
I_{CC}	supply current	per input pin; $V_{CC} = 5.5\text{ V}; V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$;	-	-	10	-	20	μA
ΔI_{CC}	additional supply current	per input; $V_{CC} = 4.5\text{ V to }5.5\text{ V}; V_I = V_{CC} - 2.1\text{ V}; I_O = 0\text{ A}$	-	-	375	-	410	μA
C_I	input capacitance		-	1.5	-	-	-	pF

[1] Typical values are measured at $T_{amb} = 25\text{ }^{\circ}\text{C}$.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); all typical values are measured at $T_{amb} = 25\text{ }^{\circ}\text{C}$; for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HC3G07								
t_{PZL}	OFF-state to LOW propagation delay	nA to nY; see Figure 6						
		$V_{CC} = 2.0\text{ V}$	-	25	95	-	125	ns
		$V_{CC} = 4.5\text{ V}$	-	9	19	-	25	ns
		$V_{CC} = 6.0\text{ V}$	-	7	16	-	20	ns
t_{PLZ}	LOW to OFF-state propagation delay	nA to nY; see Figure 6						
		$V_{CC} = 2.0\text{ V}$	-	25	95	-	125	ns
		$V_{CC} = 4.5\text{ V}$	-	11	23	-	30	ns
		$V_{CC} = 6.0\text{ V}$	-	10	23	-	26	ns
t_{THL}	HIGH to LOW output transition time	nY; see Figure 6						
		$V_{CC} = 2.0\text{ V}$	-	18	95	-	125	ns
		$V_{CC} = 4.5\text{ V}$	-	6	19	-	25	ns
		$V_{CC} = 6.0\text{ V}$	-	5	16	-	20	ns
C_{PD}	power dissipation capacitance	$V_I = \text{GND to } V_{CC}$	^[1]	4	-	-	-	pF

Table 8. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); all typical values are measured at $T_{amb} = 25\text{ }^\circ\text{C}$; for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HCT3G07								
t_{PZL}	OFF-state to LOW propagation delay	nA to nY; see Figure 6 $V_{CC} = 4.5\text{ V}$	-	11	27	-	32	ns
t_{PLZ}	LOW to OFF-state propagation delay	nA to nY; see Figure 6 $V_{CC} = 4.5\text{ V}$	-	10	26	-	31	ns
t_{THL}	HIGH to LOW output transition time	$V_{CC} = 4.5\text{ V}$; see Figure 6	-	6	19	-	22	ns
C_{PD}	power dissipation capacitance	$V_I = \text{GND to } V_{CC} - 1.5\text{ V}$ [1]	-	4	-	-	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

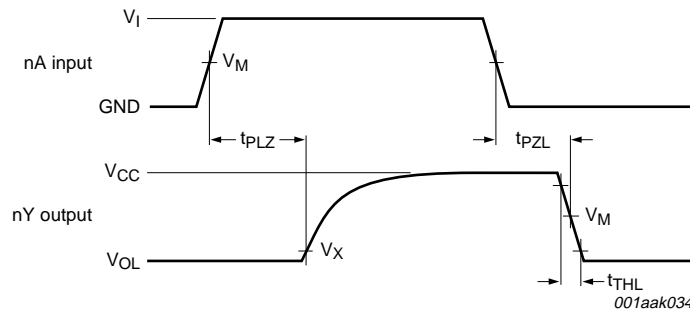
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

12. Waveforms



Measurement points are given in [Table 9](#).

V_{OL} is the typical output voltage level that occurs with the output load.

Fig 6. The input (nA) to output (nY) propagation delays

Table 9. Measurement points

Type	Input	Output	
	V_M	V_M	V_X
74HC3G07	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$0.1 \times V_{CC}$
74HCT3G07	1.3 V	1.3 V	$0.1 \times V_{CC}$



Test data is given in [Table 10](#).

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig 7. Test circuit for measuring switching times

Table 10. Test data

Type	Input		Load			S1 position
	V_I	t_r, t_f	C_L	R_L	t_{pZL}, t_{PLZ}	
74HC3G07	GND to V_{CC}	≤ 6 ns	50 pF	1 k Ω	V_{CC}	
74HCT3G07	GND to 3 V	≤ 6 ns	50 pF	1 k Ω	V_{CC}	

13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

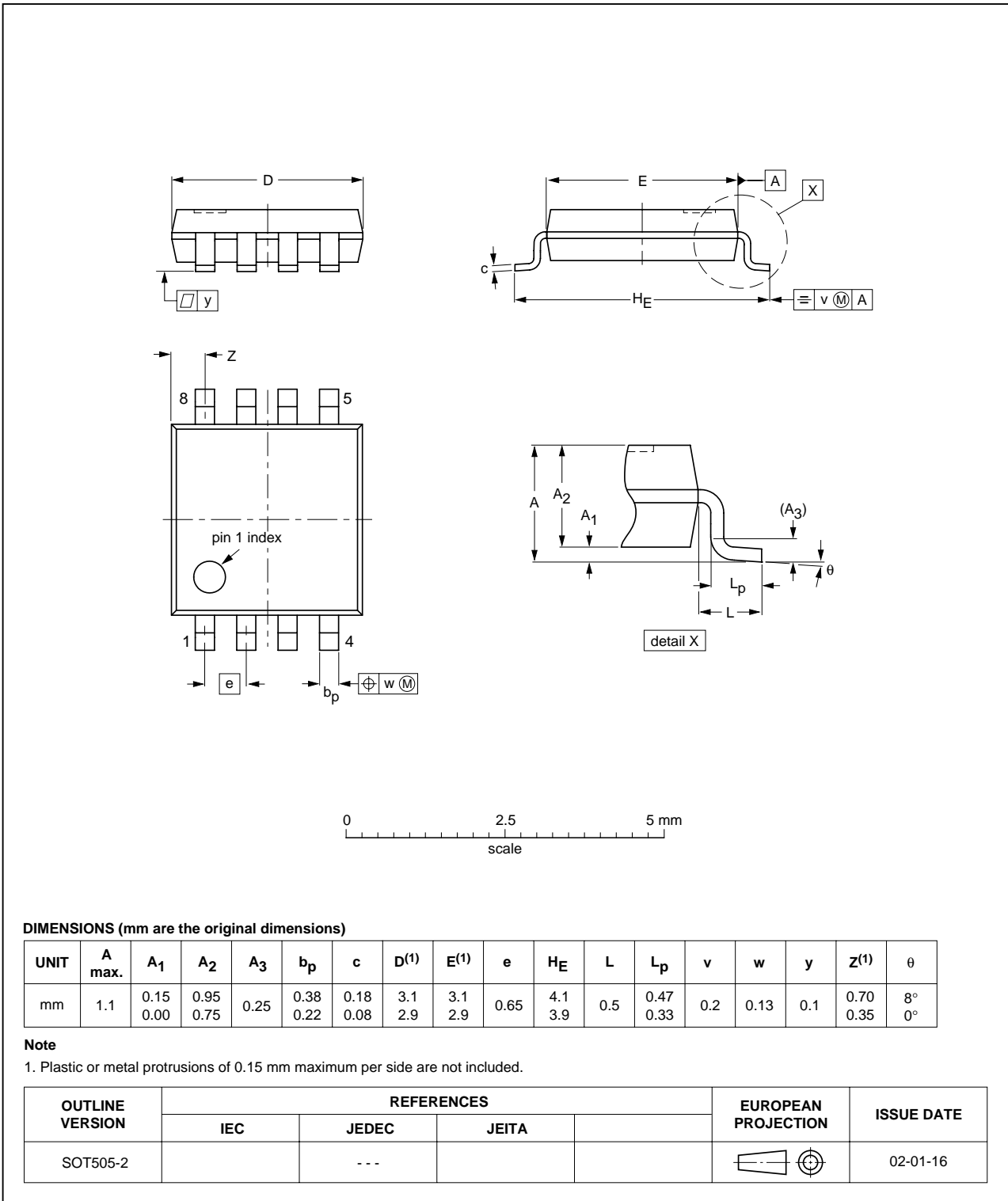


Fig 8. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

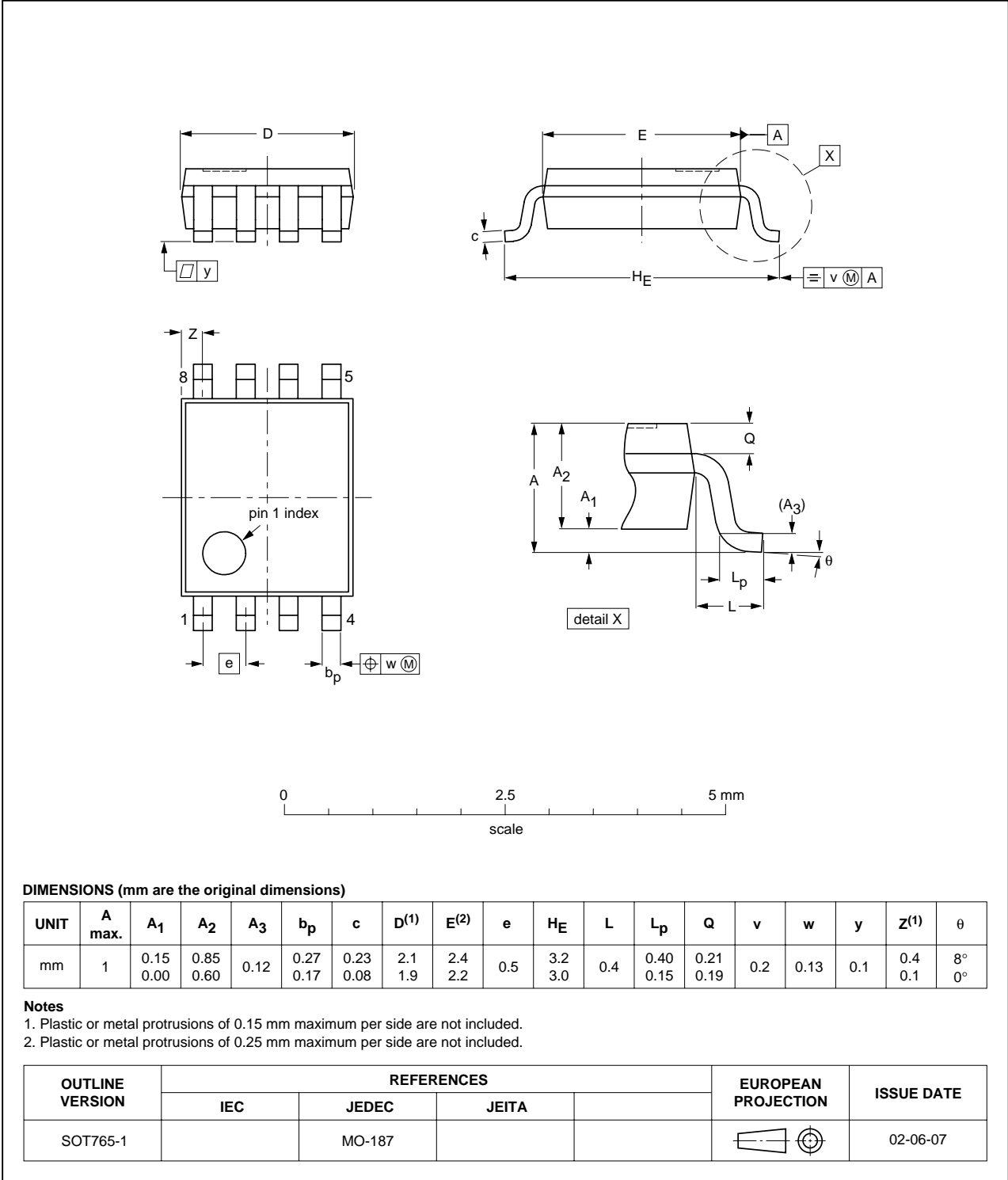


Fig 9. Package outline SOT765-1 (VSSOP8)

XSON8U: plastic extremely thin small outline package; no leads;
8 terminals; UTLP based; body 3 x 2 x 0.5 mm

SOT996-2



Fig 10. Package outline SOT996-2 (XSON8U)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT3G07_2	20090512	Product data sheet	-	74HC_HCT3G07_1
Modifications:		<ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.Legal texts have been adapted to the new company name where appropriate.Added type number 74HC3G07GD and 74HCT3G07GD (XSON8U package)		
74HC_HCT3G07_1	20031015	Product specification	-	-

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16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
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[2] The term 'short data sheet' is explained in section "Definitions".

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18. Contents

1	General description	1
2	Features	1
3	Ordering information	1
4	Marking	2
5	Functional diagram	2
6	Pinning information	2
6.1	Pinning	2
6.2	Pin description	3
7	Functional description	3
8	Limiting values	3
9	Recommended operating conditions	4
10	Static characteristics	4
11	Dynamic characteristics	5
12	Waveforms	6
13	Package outline	8
14	Abbreviations	11
15	Revision history	11
16	Legal information	12
16.1	Data sheet status	12
16.2	Definitions	12
16.3	Disclaimers	12
16.4	Trademarks	12
17	Contact information	12
18	Contents	13

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