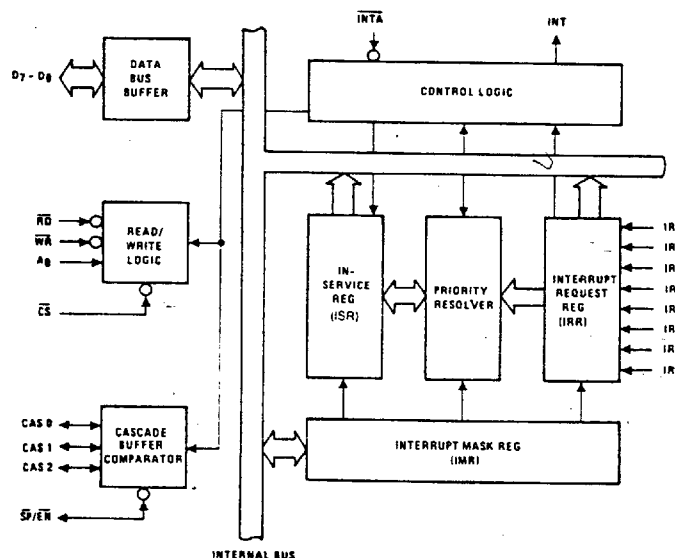


Radiation Hardened 82C59ARP

CMOS Priority
Interrupt Controller

For Space Applications

SEI's 82C59ARP (RP for RAD-PAK®) high speed CMOS microcircuit features a minimum 100 kilorad (Si) total dose tolerance. Using SEI's radiation hardened RAD-PAK® packaging technology, the 82C59ARP is fully equivalent to the commercial 82C59A from Harris Semiconductor. This device is a high performance CMOS Priority Interrupt Controller which is manufactured using a self-aligned silicon gate CMOS process. The 82C59ARP is design to relieve the system CPU from the task of polling in a multi-level priority interrupt system. It can handle up to eight vectored priority interrupting sources and is cascadable to 64 without additional circuitry. Individual interrupting sources can be masked or prioritized to allow custom system configuration. The high density advanced CMOS technology ensures low operating power capabilities. Capable of surviving space environments, the 82C59ARP is ideal for satellite, spacecraft, and space probe missions. SEI's RAD-PAK® advanced technology incorporates radiation shielding in the microcircuit package. It eliminates box shielding while providing lifetime in orbit. This device provides a total dose survivability of greater than 100 krad(Si). It is available in Class S packaging and screening.



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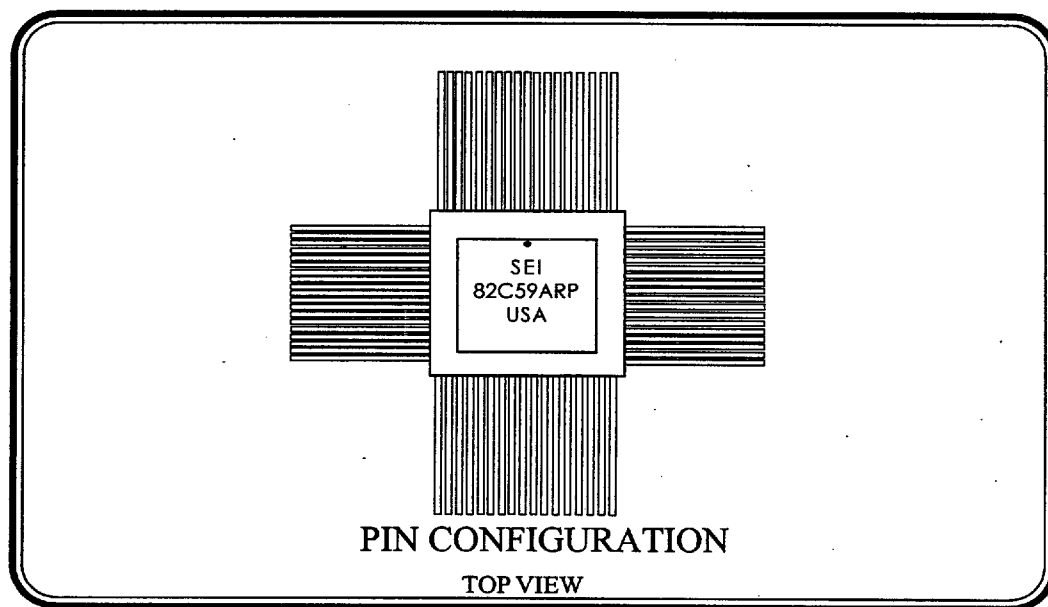
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SEI 82C59ARP RADIATION HARDENED CMOS

Radiation Hardened 82C59ARP

CMOS Priority
Interrupt Controller



Features

- ▲ Pin Compatible with Harris Semiconductor 8259A, 82C59A
- ▲ RAD-PAK® Radiation Hardened Against Natural Space Radiation
- ▲ Total Dose Hardness >100 krad (Si)
- ▲ Package:
 - 28 Pin RAD-PAK® quad flat pack (1.15 in. x 1.15 in.)
 - Weight – 4.8 grams
- ▲ High Speed: 5 MHz clock rate
- ▲ Low Power CMOS Technology
 - Standby Power <10uA
- ▲ Eight Level Priority Controller, Expandable to 64 Level
- ▲ Fully TTL Compatible
- ▲ High Speed, No "Wait State" Operation with 8MHz, 80C86 and 80C88
- ▲ Programmable Interrupt Modes
- ▲ 8080/8085 and 8086/80C86/80C88 Compatible Operation
- ▲ Fully Static Design
- ▲ Scaled SAJI IV CMOS Process
- ▲ Single 5V Power Supply
- ▲ Class S Screening per TM 5004
- ▲ QCI per TM5005 Available
- ▲ NASA Flight Qualified

Specifications and design are subject to change without notice.



June 1995

For Further Information Contact:

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82C59ARP CAPACITANCE

PARAMETER	SYMBOL	TYPICAL	UNIT
Input Capacitance	C_{IN}	5	pF
Output Capacitance	C_{OUT}	15	pF
I/O Capacitance	C_{IO}	20	pF

82C59ARP TIMING REQUIREMENTS

PARAMETER	SYMBOL	MIN	MAX	UNIT
AO/CS\ Setup to RDVINTA\	T_{AHRL}			ns
AO/CS\ Hold after RDVINTA\	T_{RHAX}			ns
RDVINTA\ Pulse Width	T_{RLRH}			ns
AO/CS\ Setup to WR\	T_{AHWL}			ns
AO/CS\ Hold after WR\	T_{WHAX}			ns
WR\ Pulse Width	T_{WLWH}			ns
Data Setup to WR\	T_{DYWH}			ns
Data Hold after WR\	T_{WHDX}			ns
Interrupt Request Width (Low)	T_{JLJH}			ns
Cascade Setup to Second or Third INTA\ (Slave Only)	T_{CVIAL}			ns
End of RD\ to next RD\; End of INTA\ to next INTA\ within an INTA\ sequence only	T_{RHRL}			ns
End of WR\ to next WR\	T_{WHWL}			ns
End of Command to next Command (Not same command type) End of INTA\ sequence to next INTA\ sequence	T_{CHCL}			ns



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82C59ARP ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V_{SS}		8	V
Input, Output, or I/O Voltage Applied		GND-0.5	$V_{CC}+0.5$	V
Storage Temperature Range	T_s			
Power Dissipation	P_D		1	W

82C59ARP DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Logical One Input Voltage	V_{IH}	2.0 2.2		V V
Logical Zero Input Voltage	V_{IL}		0.8	V
Output High Voltage $I_{OH}=-2.5mA$ $I_{OH}=-100uA$	V_{OH}	3.0 $V_{CC}-0.4$		V V
Output Low Voltage $V_{OL}=+2.5mA$	V_{OL}		0.4	V
Input Leakage Current $V_{IN}=GND$ or V_{CC}	I_I	-1.0	+1.0	μA
I/O Leakage Current $V_O=GND$ or V_{CC}	I_{IO}	-10.0	+10.0	μA
IR Input Load Current $V_{IN}=0$ $V_{IN}=V_{CC}$:All temperature ranges	I_{LIR}		-500 10	μA μA
Standby Power Supply Current $V_{CC}=5.5V$ $V_{IN}=V_{CC}$ or GND ¹ Outputs Open	I_{CCSB}		10	μA
Operating Power Supply Current $T_A=+25^{\circ}C$, $V_{CC}=5V$, Typical ²	I_{CCOP}		1	μA



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82C59ARP TIMING RESPONSES

PARAMETER	SYMBOL	MIN	MAX	UNIT
Data Valid from RD\INTA\	T _{RLDV}			ns
Data Float after RD\INTA\	T _{RHDZ}			ns
Interrupt Output Delay	T _{JHIH}			ns
Cascade Valid from First INTA\ (Master Only)	T _{JALCV}			ns
Enable Active from RD\ or INTA\	T _{RLEL}			ns
Enable Inactive from RD\ or INTA\	T _{RHEH}			ns
Data Valid from Stable Address	T _{AHDV}			ns
Cascade Valid to Valid Data	T _{CVDV}			ns

82C59ARP Package Ordering Guide

Package Style	Case Outline	1/	Description
Q	Q-28		28 Pin Quad Flat Package

Note:

1/ For outline information, see Appendix A (Package Information - Outline Dimension)



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