

32K x 8 Very High Speed CMOS Static RAM

Features

- Fast access times: 8 and 10 ns
- Fast output enable (t_{DOE}) for cache applications
- Low active power: 400 mW (Typical)
- Low standby power
- Fully static operation, no clock or refresh required
- TTL-compatible inputs and outputs
- Single +5V $\pm 10\%$ power supply
- Commercial and industrial temperature range

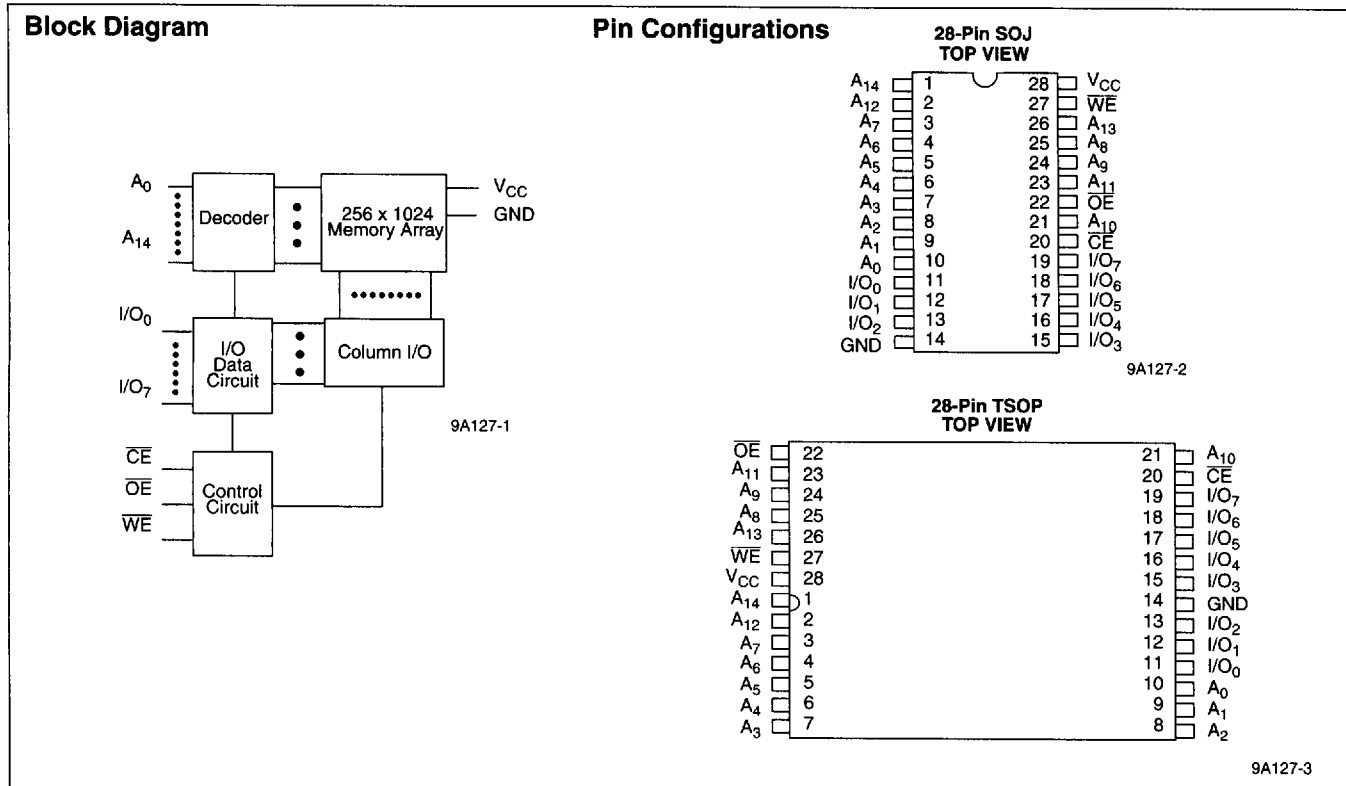
Functional Description

The Aptos AP9A127 is a very high speed, low power, 32,768-word by 8-bit CMOS static RAM. It is fabricated using Aptos' high-performance CMOS, double metal technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 8ns (Max).

When Chip Enable ($\overline{CE}$) is HIGH, the device assumes a standby mode at which the power dissipation can be reduced down to 10 μ W (typical) at CMOS input levels.

Easy memory expansion is provided by using asserted LOW $\overline{CE}$ and asserted LOW output enable inputs ($\overline{OE}$). The asserted LOW write enable ($\overline{WE}$) controls both writing and reading of the memory.

The AP9A127 is pin-compatible with the Aptos AP9A128 and other 32K x 8 SRAMs in the SOJ, and TSOP packages.



Selection Guide

	AP9A127-8	AP9A127-10
Maximum Access Time (ns)	8	10
Maximum Operating Current (mA)	125	115
Maximum Standby Current (mA)	10	10

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature..... -65°C to +150°C

Ambient Temperature

with Power Applied..... -55°C to +125°C

V_{CC} Supply Relative to GND..... -1.0 V to +7.0 V

Voltage on Any Pin Relative to GND..... -0.5 V to V_{CC} +0.5 V

Short Circuit Output Current¹..... ±50 mA

Power Dissipation..... 1.0 W

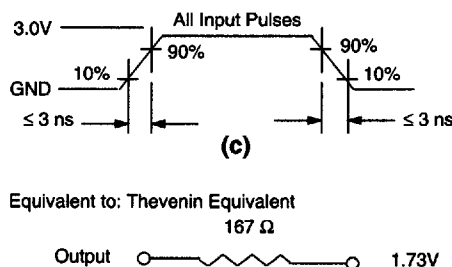
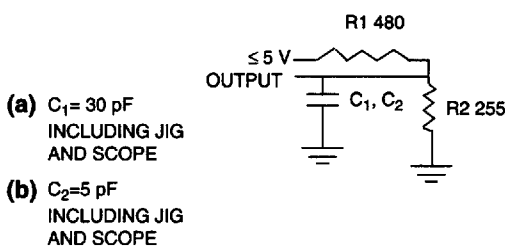
Electrical Characteristics Over the Operating Range (0 °C ≤ T_A ≤ 70 °C, V_{CC} = 5V ±10%) -Commercial

Symbol	Parameter	Test Conditions	9A127-8		9A127-10		Unit
			Min.	Max.	Min.	Max.	
I _{CC1}	Dynamic Operating Current	V _{CC} = Max., I _{OUT} = 0 mA, $\overline{CE} = V_{IL}$, f = fmax.		125		115	mA
I _{CC2}	Operating Current	V _{CC} = Max., I _{OUT} = 0 mA, $\overline{CE} = V_{IL}$, f = 0		80		80	mA
I _{SB1}	TTL Standby Current -TTL Inputs	V _{CC} = Max., V _{IN} = V _{IH} or V _{IL} , $\overline{CE} \geq V_{IH}$, f=fmax.		35		35	mA
I _{SB2}	CMOS Standby Current-CMOS Inputs	V _{CC} = Max., $\overline{CE} \geq V_{CC}$ -0.2V, V _{IN} ≥ V _{CC} -0.2V or V _{IN} ≤ 0.2 V, f = 0		10		10	mA
I _{LI}	Input Leakage Current	GND ≤ V _{IN} ≤ V _{CC}	-1	1	-1	1	μA
I _{LO}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , Output Disabled	-1	1	-1	1	μA
V _{OH}	Output High Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		2.4		V
V _{OL}	Output Low Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input High Voltage		2.2	V _{CC} +0.5	2.2	V _{CC} +0.5	V
V _{IL}	Input Low Voltage		-0.5	0.8	-0.5	0.8	V

Capacitance

Symbol	Description	Max.	Unit
C _{IN}	Input Capacitance	5	pF
C _{IO}	I/O Capacitance	5	pF

AC Test Loads and Waveforms



Notes:

1. No more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

2. Tested initially and after any design or process changes that may effect these parameters.

3. V_{IL} = -3.0 V for pulse width less than 3 ns.

Electrical Characteristics Over the Operating Range ($-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, $V_{CC} = 5V \pm 10\%$) -Industrial

Symbol	Parameter	Test Conditions	9A127-10		Unit
			Min.	Max.	
I_{CC1}	Dynamic Operating Current	$V_{CC} = \text{Max.}, I_{OUT} = 0\text{ mA}, \overline{CE} = V_{IL}, f = f_{\text{max.}}$		135	mA
I_{CC2}	Operating Current	$V_{CC} = \text{Max.}, I_{OUT} = 0\text{ mA}, \overline{CE} = V_{IL}, f = 0$		100	mA
I_{SB1}	TTL Standby Current -TTL Inputs	$V_{CC} = \text{Max.}, V_{IN} = V_{IH} \text{ or } V_{IL}, \overline{CE} \geq V_{IH}, f = \text{Max.}$		55	mA
I_{SB2}	CMOS Standby Current -CMOS Inputs	$V_{CC} = \text{Max.}, \overline{CE} \geq V_{CC} - 0.2V, V_{IN} \geq V_{CC} - 0.2V \text{ or } V_{IN} \leq 0.2V, f = 0$		25	mA
I_{LI}	Input Leakage Current	$GND \leq V_{IN} \leq V_{CC}$	-1	1	μA
I_{LO}	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC},$ Output Disabled	-1	1	μA
V_{OH}	Output High Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0\text{ mA}$	2.4		V
V_{OL}	Output Low Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0\text{ mA}$		0.4	V
V_{IH}	Input High Voltage		2.2	$V_{CC} + 0.5$	V
V_{IL}	Input Low Voltage		-0.5	0.8	V

Switching Characteristics Over the Operating Range ¹

Parameter	Description	9A127-8		9A127-10		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t _{RC}	Read Cycle Time	8		10		ns
t _{AA}	Address Access Time		8		10	ns
t _{OHA}	Output Hold Time	3		3		ns
t _{ACE}	$\overline{CE}$ Access Time		8		10	ns
t _{DOE}	$\overline{OE}$ Access Time		4		5	ns
t _{LZOE}	$\overline{OE}$ to Low-Z Output	0		0		ns
t _{HZOE} ²	$\overline{OE}$ to High-Z Output		4		5	ns
t _{LZCE}	$\overline{CE}$ to Low-Z Output	3		3		ns
t _{HZCE}	$\overline{CE}$ to High-Z Output		4		5	ns
t _{PU}	$\overline{CE}$ to Power Up	0		0		ns
t _{PD}	$\overline{CE}$ to Power Down		8		10	ns
Write Cycle ³						
t _{WC}	Write Cycle Time	8		10		ns
t _{SCE}	$\overline{CE}$ to Write End	7		7		ns
t _{AW}	Address to Set-up Time to Write End	7		7		ns
t _{HA}	Address Hold to Write End	0		0		ns
t _{SA}	Address Set-up Time	0		0		ns
t _{PWE1} ⁴	$\overline{WE}$ Pulse Width ($\overline{OE}$ =HIGH)	7		7		ns
t _{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ =LOW)	8		10		ns
t _{SD}	Data Set-up to Write End	5		6		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{HZWE} ²	$\overline{WE}$ LOW to High-Z Output		4		5	ns
t _{LZWE}	$\overline{WE}$ HIGH to Low-Z Output	2		2		ns

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 - 3.0 V and output loading specified in AC Test Loads and Waveforms *Figure (a)*.
2. Tested with the load in AC Test Loads and Waveforms *Figure (b)*. Transition is measured ± 500 mV from steady state voltage.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but

either can be deasserted to terminate the Write. The Data Input Set-up and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

4. Tested with $\overline{OE}$ High.
5. $\overline{WE}$ is HIGH for a Read Cycle.
6. The device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
7. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.
8. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

Pin Descriptions

A₀ - A₁₄: Address Inputs

These 15 address inputs select one of the 32,768 8-bit words in the RAM.

$\overline{\text{CE}}$: Chip Enable Input

$\overline{\text{CE}}$ is asserted LOW. The Chip Enable is asserted LOW to read from or write to the device. If Chip Enable is deasserted, the device is deselected and is in a standby power mode. The I/O pins will be in the high-impedance state when the device is deselected.

$\overline{\text{OE}}$: Output Enable Input

The Output Enable input is asserted LOW. If the Output

Enable is asserted LOW while $\overline{\text{CE}}$ is asserted (LOW) and $\overline{\text{WE}}$ is deasserted (HIGH), data from the SRAM will be present on the I/O pins. The I/O pins will be in the high-impedance state when $\overline{\text{OE}}$ is deasserted.

$\overline{\text{WE}}$: Write Enable Input

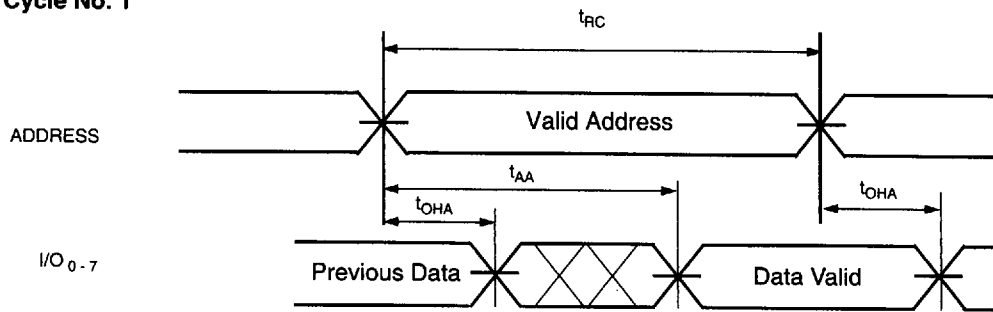
The Write Enable input is asserted LOW and controls read and write operations. When $\overline{\text{CE}}$ and $\overline{\text{WE}}$ are both asserted (LOW) input data present on the I/O pins will be written into the selected memory location.

I/O₀ - I/O₇: Common Input/Output Pins

GND: Ground

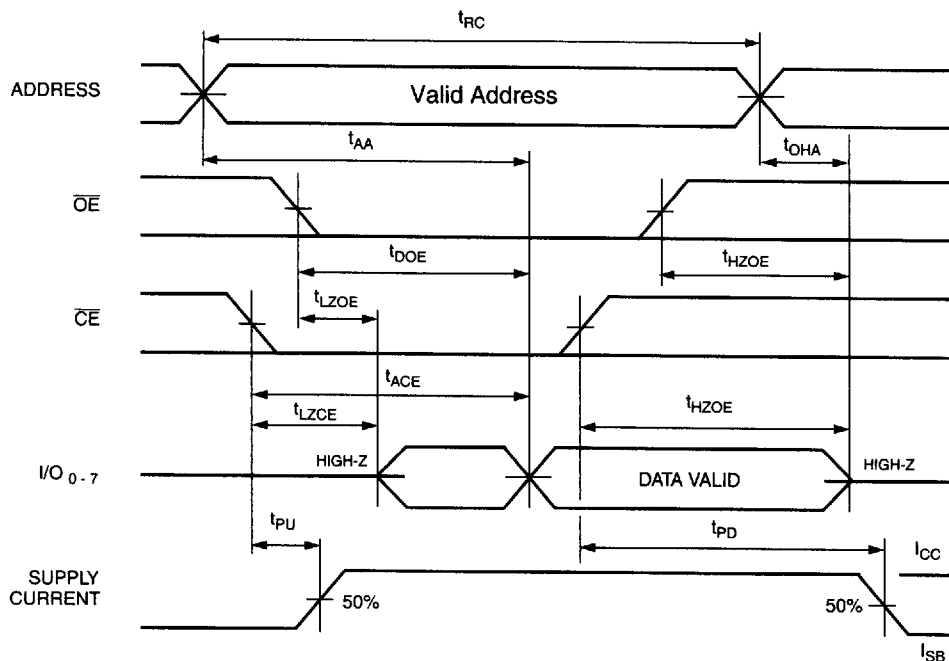
Switching Waveforms

Read Cycle No. 1



9A127-4

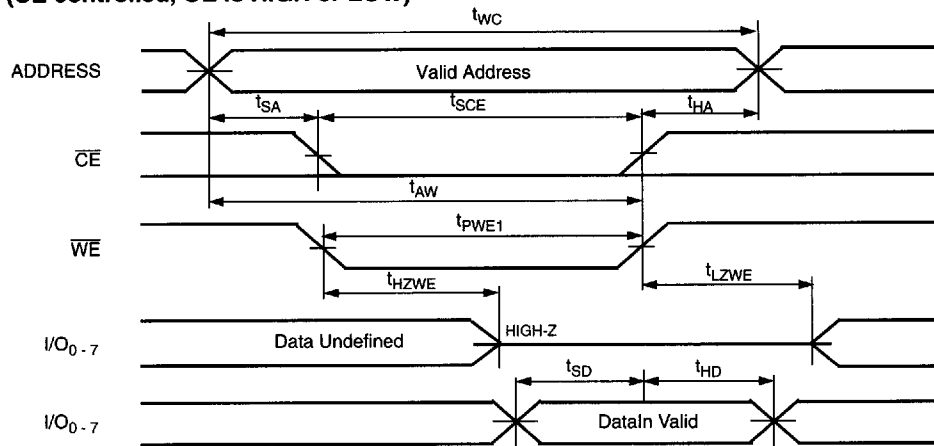
Read Cycle No. 2



9A127-5

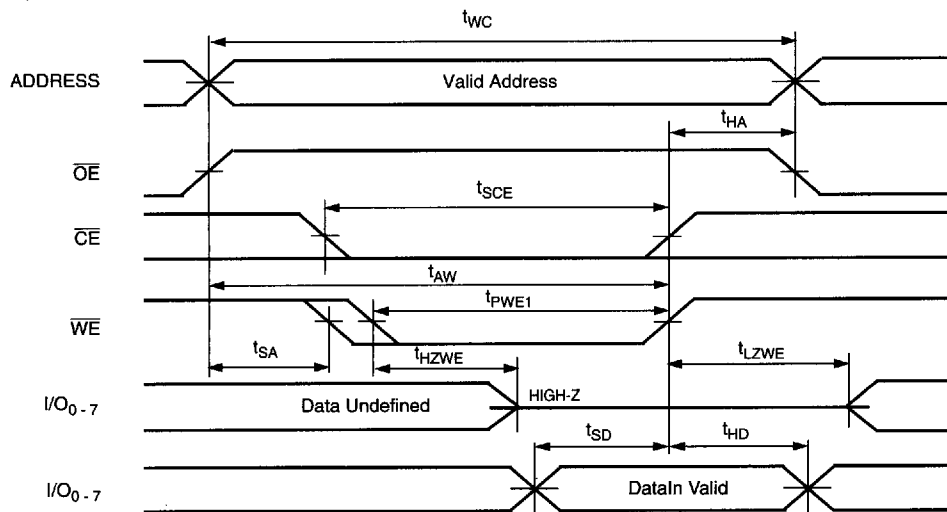
Switching Waveforms (continued)

Write Cycle No.1 ($\overline{\text{CE}}$ controlled, $\overline{\text{OE}}$ is HIGH or LOW)



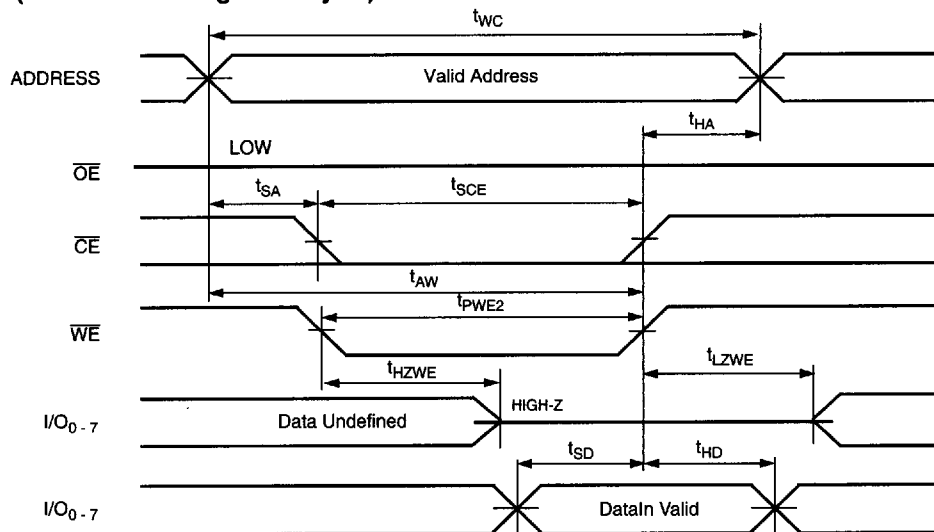
9A127-6

Write Cycle No.2 ($\overline{\text{OE}}$ is HIGH During Write Cycle)



9A127-7

Write Cycle No.3 ($\overline{\text{OE}}$ is LOW During Write Cycle)



9A127-8

Truth Table

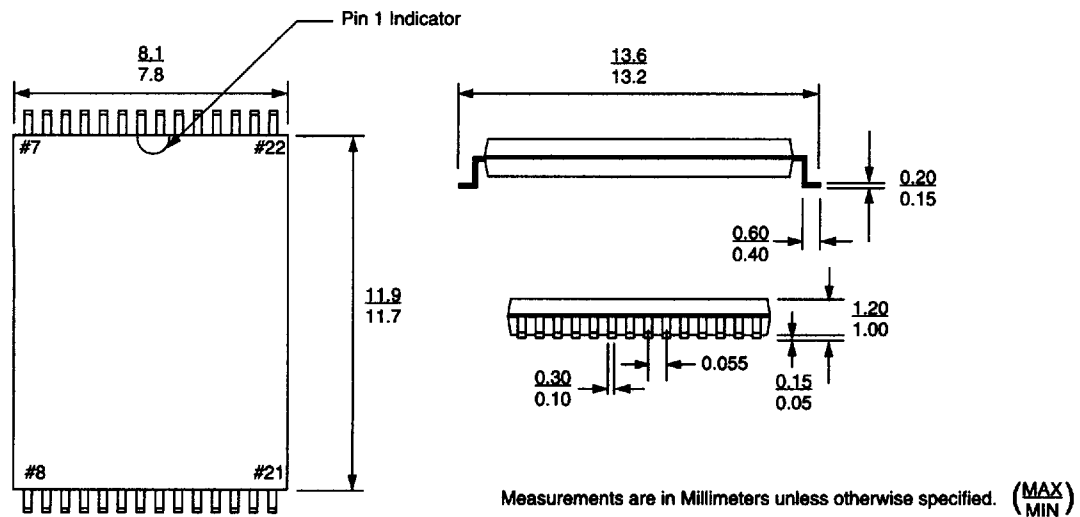
Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O	I_{CC}
Not Selected (Power Down)	X	H	X	High-Z	I_{SB1} , I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC1} , I_{CC2}
Read	H	L	L	D_{OUT}	I_{CC1} , I_{CC2}
Write	L	L	X	D_{IN}	I_{CC1} , I_{CC2}

Ordering Information

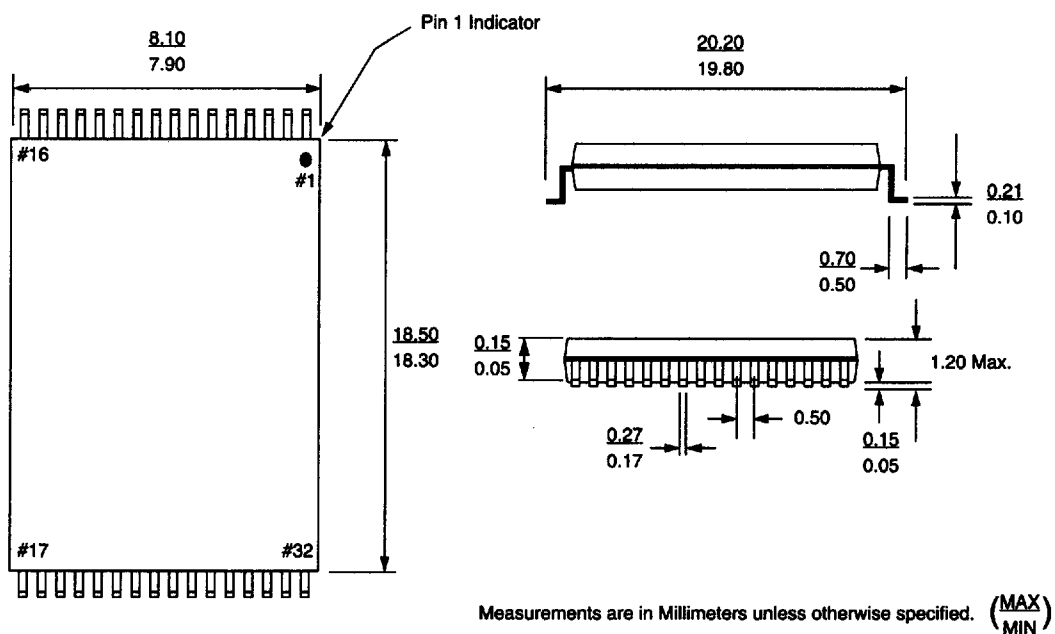
Speed	Part Number	Package Name	Package Type	Temperature Range
8	AP9A127-8VC	V28.1	28-Pin Small Outline J-Bend	Commercial
10	AP9A127-10VC	V28.1	28-Pin Small Outline J-Bend	Commercial
	AP9A127-10VI	V28.1	28-Pin Small Outline J-Bend	Industrial
	AP9A127-10TC	T28.1	28-Pin Thin Small Outline Package	Commercial

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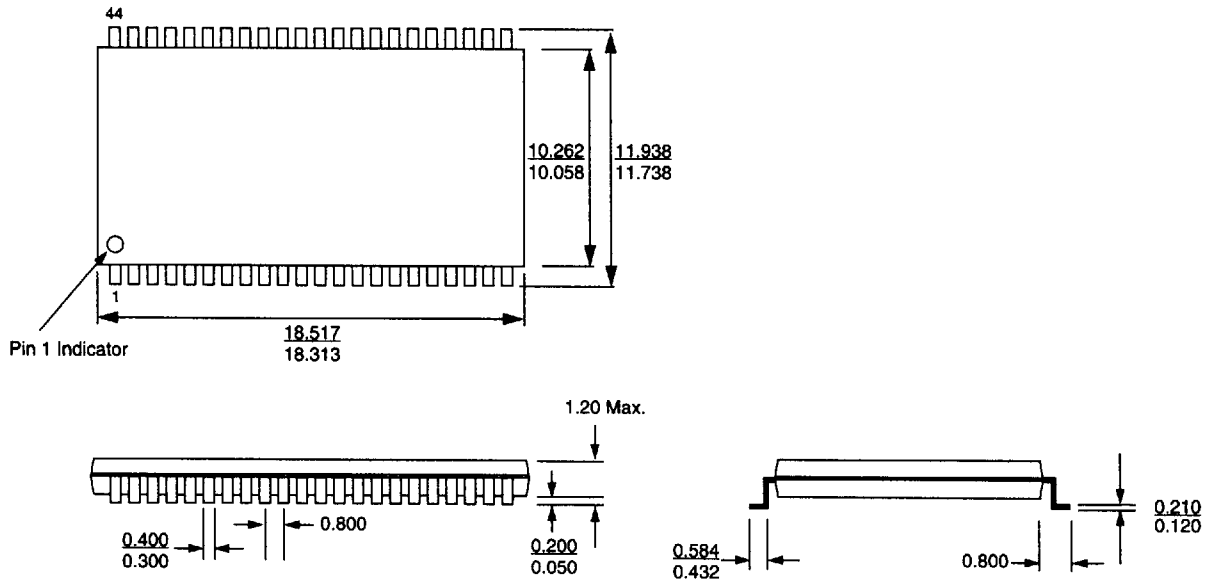
T28.1 - 28-Pin Thin Small Outline Package (TSOP)



T32.1 - 32-Pin Thin Small Outline Package (TSOP)

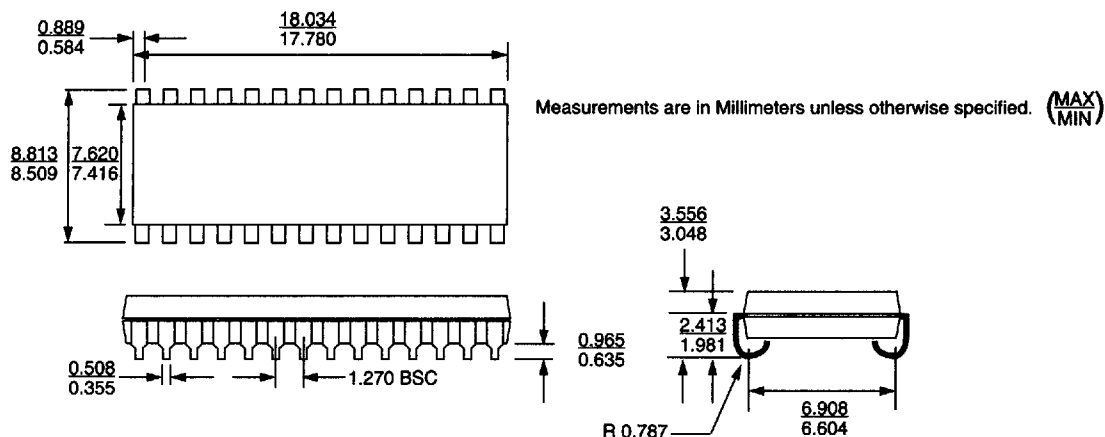


T44.1 - 44-Pin (400-Mil) Thin Small Outline Package (TSOP)

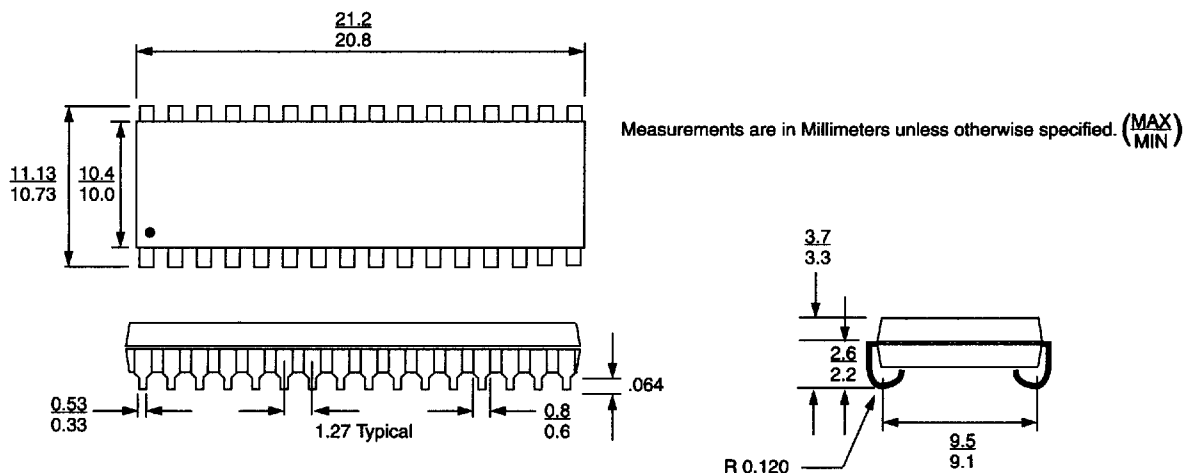


Measurements are in Millimeters unless otherwise specified. (MAX)
(MIN)

V28.1 - 28-Pin (300-Mil) Small Outline J-Bend (SOJ)



V32.1 - 32-Pin (400-Mil) Small Outline J-Bend (SOJ)



V44.1 - 44-Pin (400-Mil) Small Outline J-Bend (SOJ)

