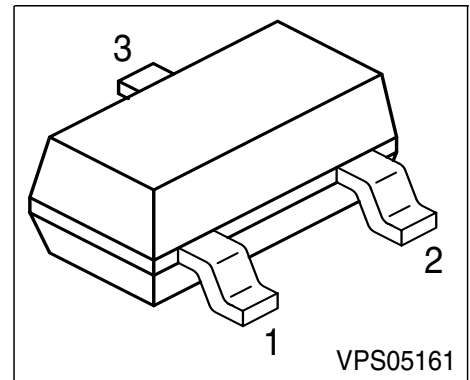
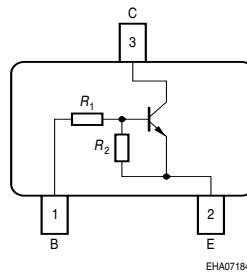


NPN Silicon Digital Transistor

- Switching circuit, inverter, interface circuit, driver circuit
- Built in bias resistor ($R_1=4.7k\Omega$, $R_2=47k\Omega$)



Type	Marking	Pin Configuration			Package
BCR 116	WG5	1 = B	2 = E	3 = C	SOT-23

Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CEO}	50	V
Collector-base voltage	V_{CBO}	50	
Emitter-base voltage	V_{EBO}	5	
Input on Voltage	$V_{i(on)}$	15	
DC collector current	I_C	100	mA
Total power dissipation, $T_S = 102\text{ °C}$	P_{tot}	200	mW
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	-65 ... 150	

Thermal Resistance

Junction ambient ¹⁾	R_{thJA}	≤ 350	K/W
Junction - soldering point	R_{thJS}	≤ 240	

1) Package mounted on pcb 40mm x 40mm x 1.5mm / 6cm ²Cu

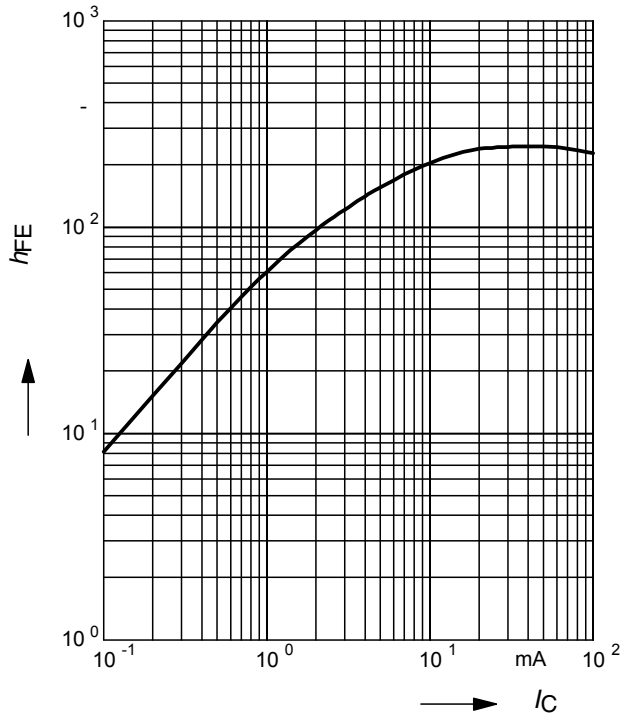
Electrical Characteristics at $T_A=25^{\circ}\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Collector-emitter breakdown voltage $I_C = 100\text{ }\mu\text{A}$, $I_B = 0$	$V_{(BR)CEO}$	50	-	-	V
Collector-base breakdown voltage $I_C = 10\text{ }\mu\text{A}$, $I_B = 0$	$V_{(BR)CBO}$	50	-	-	
Collector cutoff current $V_{CB} = 40\text{ V}$, $I_E = 0$	I_{CBO}	-	-	100	nA
Emitter cutoff current $V_{EB} = 5\text{ V}$, $I_C = 0$	I_{EBO}	-	-	155	μA
DC current gain 1) $I_C = 5\text{ mA}$, $V_{CE} = 5\text{ V}$	h_{FE}	70	-	-	-
Collector-emitter saturation voltage1) $I_C = 10\text{ mA}$, $I_B = 0.5\text{ mA}$	V_{CEsat}	-	-	0.3	V
Input off voltage $I_C = 100\text{ }\mu\text{A}$, $V_{CE} = 5\text{ V}$	$V_{i(off)}$	0.4	-	0.8	V
Input on Voltage $I_C = 2\text{ mA}$, $V_{CE} = 0.3\text{ V}$	$V_{i(on)}$	0.5	-	1.4	
Input resistor	R_1	3.2	4.7	6.2	k Ω
Resistor ratio	R_1/R_2	0.09	0.1	0.11	-
AC Characteristics					
Transition frequency $I_C = 10\text{ mA}$, $V_{CE} = 5\text{ V}$, $f = 100\text{ MHz}$	f_T	-	160	-	MHz
Collector-base capacitance $V_{CB} = 10\text{ V}$, $f = 1\text{ MHz}$	C_{cb}	-	3	-	pF

1) Pulse test: $t < 300\mu\text{s}$; $D < 2\%$

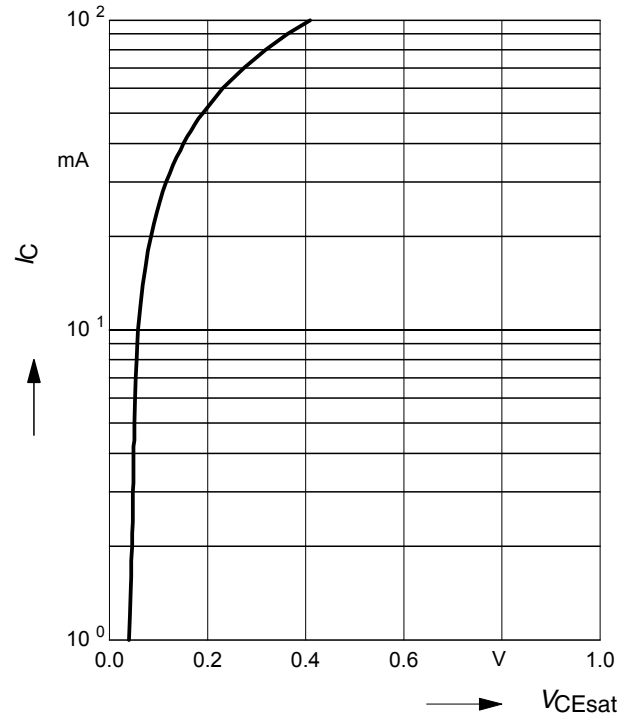
DC Current Gain $h_{FE} = f(I_C)$

$V_{CE} = 5V$ (common emitter configuration)



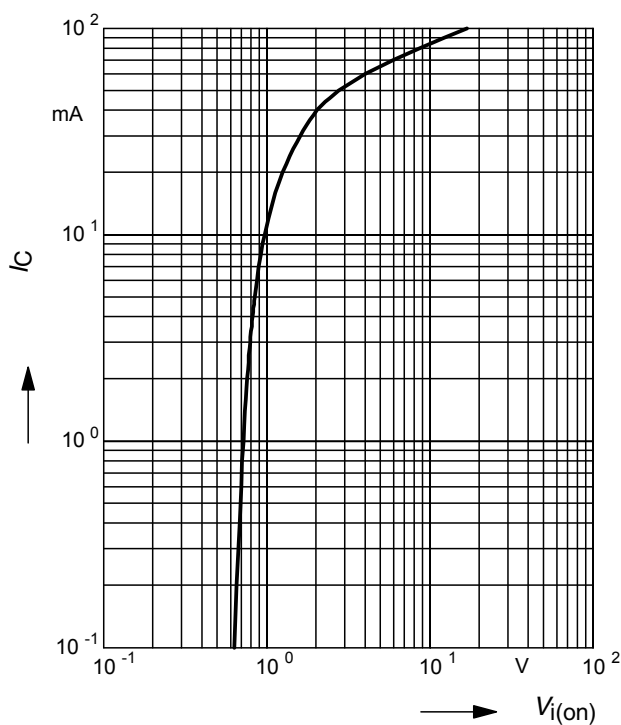
Collector-Emitter Saturation Voltage

$V_{CEsat} = f(I_C), h_{FE} = 20$



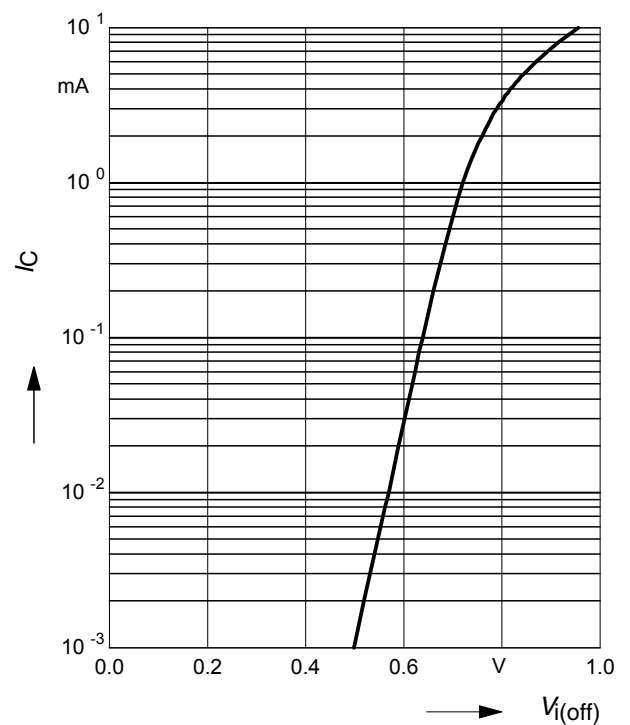
Input on Voltage $V_{i(on)} = f(I_C)$

$V_{CE} = 0.3V$ (common emitter configuration)



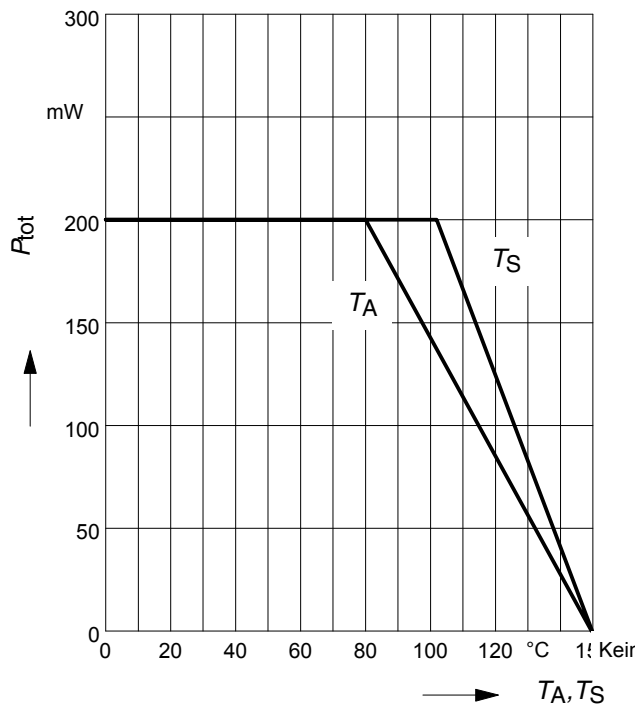
Input off voltage $V_{i(off)} = f(I_C)$

$V_{CE} = 5V$ (common emitter configuration)

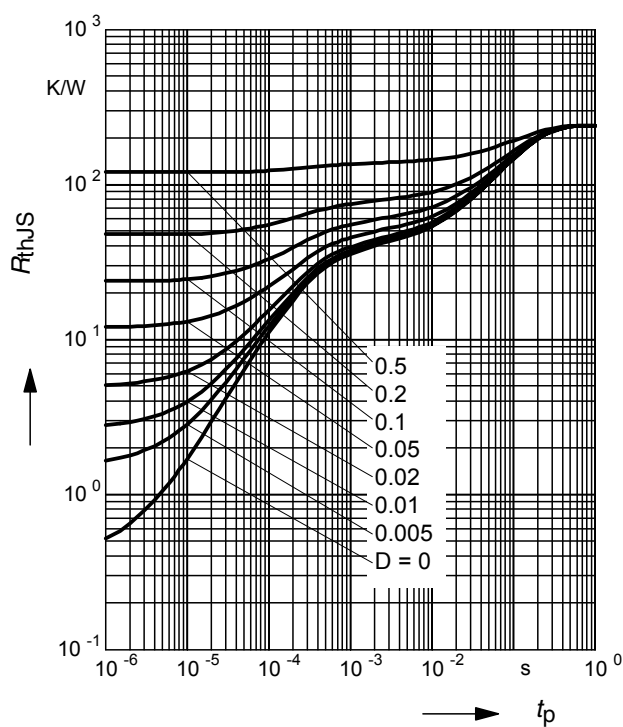


Total power dissipation $P_{\text{tot}} = f(T_A^*; T_S)$

* Package mounted on epoxy



Permissible Pulse Load $R_{\text{thJS}} = f(t_p)$



Permissible Pulse Load

$P_{\text{totmax}} / P_{\text{totDC}} = f(t_p)$

