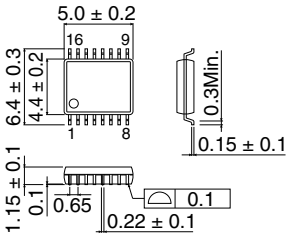
Clock generator for digital still camera

BU2382FV

●Description

BU2382FV is a high-performance 2-channel PLL IC. PLL circuit generates necessary clocks by inputting standard clocks of crystal oscillator from outside. Changing a connection of wire can generate any clocks required for any applications of users. Jitter and S/N characteristic has achieved almost the same high-quality sound and vision as oscillating module because of optimization of PLL. Frequency can be changed by the internal dividing control.

●Dimension (Units : mm)



SSOP-B16

●Features

1) Generate clocks for CDS, USB with standard clock input
2) No external elements required
3) Standard clocks apply to two kinds of NTSC/PAL
4) Power down control in each 2-channel PLL
5) Single power supply of 3.3V operating
6) SSOP-B16 small package

● Applications

Digital still camera

● Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Limits	Unit
Applied voltage	V_{DD}	–0.5 ~ +7.0	V
Input voltage	VIN	–0.5 ~ V_{DD}+0.5	V
Storage temperature range	Tstg	–30 ~ +125	℃
Power dissipation	PD	450	mW

*IC destruction is not occurred, however, operation can not be guaranteed.
*Derating : 4.5mW/℃ for operation above Ta=25℃
*This product is not designed for protection against radioactive rays.
*Power dissipation is the rate when the IC is mounted on the board.

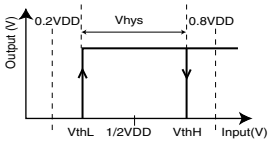
● Recommended Operating Conditions (Ta=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	3.0	–	3.6	V
Input H voltage range	VIH	0.8V_{DD}	–	V_{DD}	V
Input L voltage range	VIL	0	–	0.2V_{DD}	V
Operating temperature	Topr	–5	–	70	℃
Output load	CL	–	–	15	pF

● Electrical Characteristics (Unless otherwise noted; Ta=25℃, Vcc=3.3V, Xtal frequency=14.318182MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output H voltage	VOH	2.4	–	–	V	IOH=–4.0mA
Output L voltage	VOL	–	–	0.4	V	IOL=4.0mA
Input thL *3	VthL	0.2V_{DD}	–	–	V	*1
Input thH *3	VthH	–	–	0.8V_{DD}	V	*1
Hysteresis width *3	Vhys	–	0.4	–	V	Vhys=VthH–VthL
Operating circuit current	IDD	–	30	45	mA	No load
CLK1	CLK1_LL	–	48.626786	–	MHz	XTAL 170/31/2 (XTAL=17.734475MHz)
	CLK1_LH		70.937900			XTAL 360/45/2 (XTAL=17.734475MHz)
	CLK1_HL		48.461539			XTAL 176/26/2 (XTAL=14.318182MHz)
	CLK1_HH		71.877274			XTAL 502/50/2 (XTAL=14.318182MHz)
CLK2	CLK2_L	–	47.998742	–	MHz	XTAL 249/46/2 (XTAL=17.734475MHz)
	CLK2_H		47.998451			XTAL 295/44/2 (XTAL=14.38182MHz)
Duty	Duty	45	50	55	%	1/2V_{DD} test
Jitter **σ**	JsSD	–	30	–	psec	1 **σ** short time jitter
Jitter Min.-Max.	JsABS	–	180	–	psec	Min.–Max.
Rise time	tr	–	2.5	–	nsec	20% ~ 80% time of V_{DD}
Fall time	tf	–	2.5	–	nsec	20% ~ 80% time of V_{DD}
Output Lock time	tlock	–	–	1	msec	*2

Note) Output frequency is determined by the operation expression (Frequency divide) input to XTAL IN.
Output at 27MHz input is shown above.
Jitter is value when using Time interval analyzer with 10000 sampling.
※1) Low and high limit voltage in the schmitt trigger input Pin having hysteresis features shown in ※3 diagram.
※2) Time that output takes to stabilize in the specific frequency range after the power supply reaches to 3.0V.
※3) Make reference to the diagram.



● Block Diagram