CAT27128A OTP

16,384 x 8-BIT ONE-TIME PROGRAMMABLE ROM

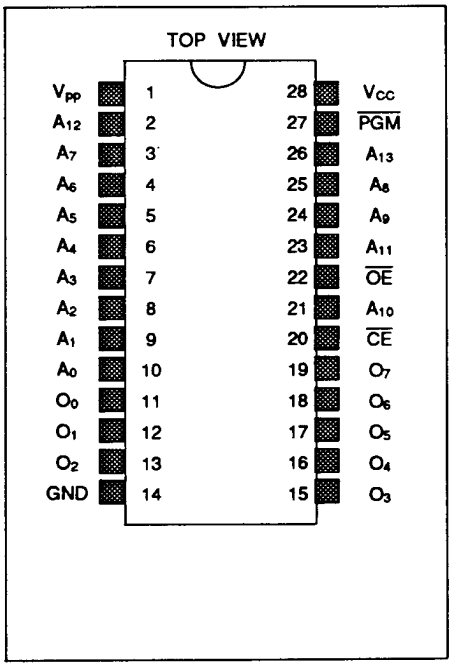
DESCRIPTION

The CAT27128A is a One Time Programmable Read Only Memory (OTPROM). It is offered in a plastic package, ideally suited for high volume production. The fast access time of the CAT27128A allows it to be used in systems that utilize high performance microprocessor systems. The CAT27128A is manufactured using N-channel dual-poly silicon gate MOS technology and supplied in a 28-pin JEDEC approved package.

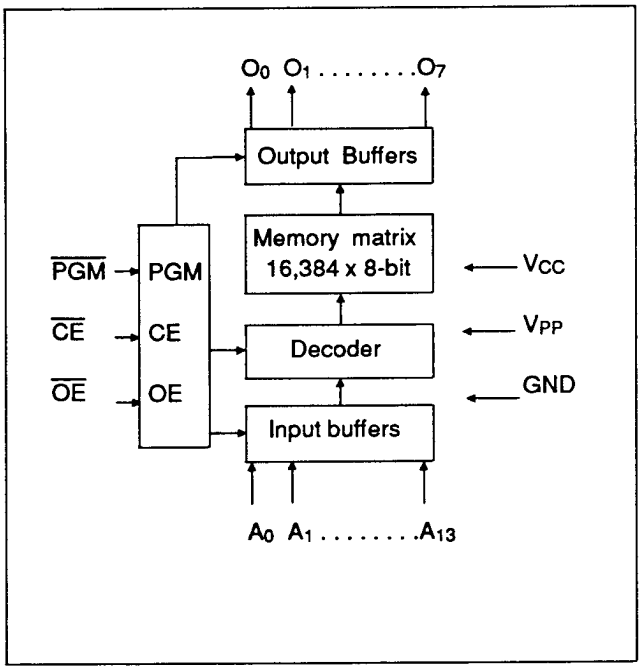
FEATURES

- 5V single power supply
- 16,384 words x 8-bit configuration
- Access time:
  - 150ns max (CAT27128A-15)
  - 200ns max (CAT27128A-20)
  - 250ns max (CAT27128A-25)
- Power consumption:
  - Active: 100mA
  - Standby: 35mA
- Fully static operation
- TTL compatible Input/Output (3-state output)

PIN CONFIGURATION



BLOCK DIAGRAM



FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5V	+5V	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{IH}	+5V	+5V	High impedance
Standby	V_{IH}	-	-	+5V	+5V	High impedance
Program	V_{IL}	V_{IH}	V_{IL}	+12.5V	+6V	D_{IN}
Program verify	V_{IL}	V_{IL}	V_{IH}	+12.5V	+6V	D_{OUT}
Program inhibit	V_{IH}	-	-	+12.5V	+6V	High impedance

The "-" means the value can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature under bias	0°C ~ 70°C
Storage temperature	- 55°C ~ 125°C
All input/output voltages	- 0.6 ~ 13.5V
V_{CC} supply voltage	- 0.6V ~ 7V
Program voltage	- 0.6 ~ 14V
Power assembly voltage	1.5W

(Voltages with respect to ground)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS <Read Operation>

(V_{CC} = 5V ± 5%, V_{PP} = V_{CC} voltages with respect to ground, T_A = 0°C to 70°C)

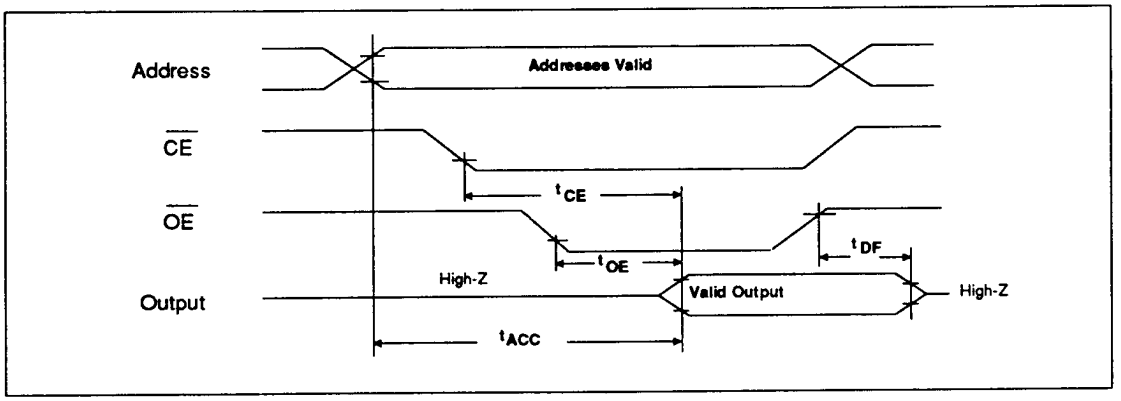
Symbol	Parameter	Conditions	Limits			Units
			Min.	Typ.	Max.	
I_{LI}	Input leakage current	V_{IN} = V_{IH} or V_{IL}	-	-	10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.25V	-	-	10	µA
I_{CC1}	V_{CC} power current (standby)	$\overline{CE}$ = V_{IH}, outputs unloaded	-	-	35	mA
I_{CC2}	V_{CC} power current (operation)	$\overline{CE}$ = V_{IL}, outputs unloaded	-	-	100	mA
I_{PP1}	Program power current	V_{PP} = V_{CC}	-	-	5	mA
V_{IH}	Input voltage "H" level	-	2.0	-	V_{CC}+1	V
V_{IL}	Input voltage "L" level	-	-0.1	-	0.8	V
V_{OH}	Output voltage "H" level	I_{OH} = -400µA	2.4	-	-	V
V_{OL}	Output voltage "L" level	I_{OL} = 2.1mA	-	-	0.45	V

AC CHARACTERISTICS <Read Operation>

(V_{CC} = 5V ± 5%, V_{PP} = V_{CC}, $\overline{PGM}$ = V_{IH}, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	27128A-15		27128A-20		27128A-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACC}	Address access time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	-	150	-	200	-	250	ns
t_{CE}	$\overline{CE}$ access time	$\overline{OE}$ = V_{IL}	-	150	-	200	-	250	ns
t_{OE}	$\overline{OE}$ access time	$\overline{CE}$ = V_{IL}	-	60	-	75	-	100	ns
t_{DF}	Output disable time	$\overline{CE}$ = V_{IL}	0	50	0	60	0	70	ns

TIMING <Read Operation>



DC CHARACTERISTICS <Programming Operation>

(V_{CC} = 5.75 - 6.5V, V_{PP} = 12.5V ± 0.5V, T_A = 25°C ± 5°C)

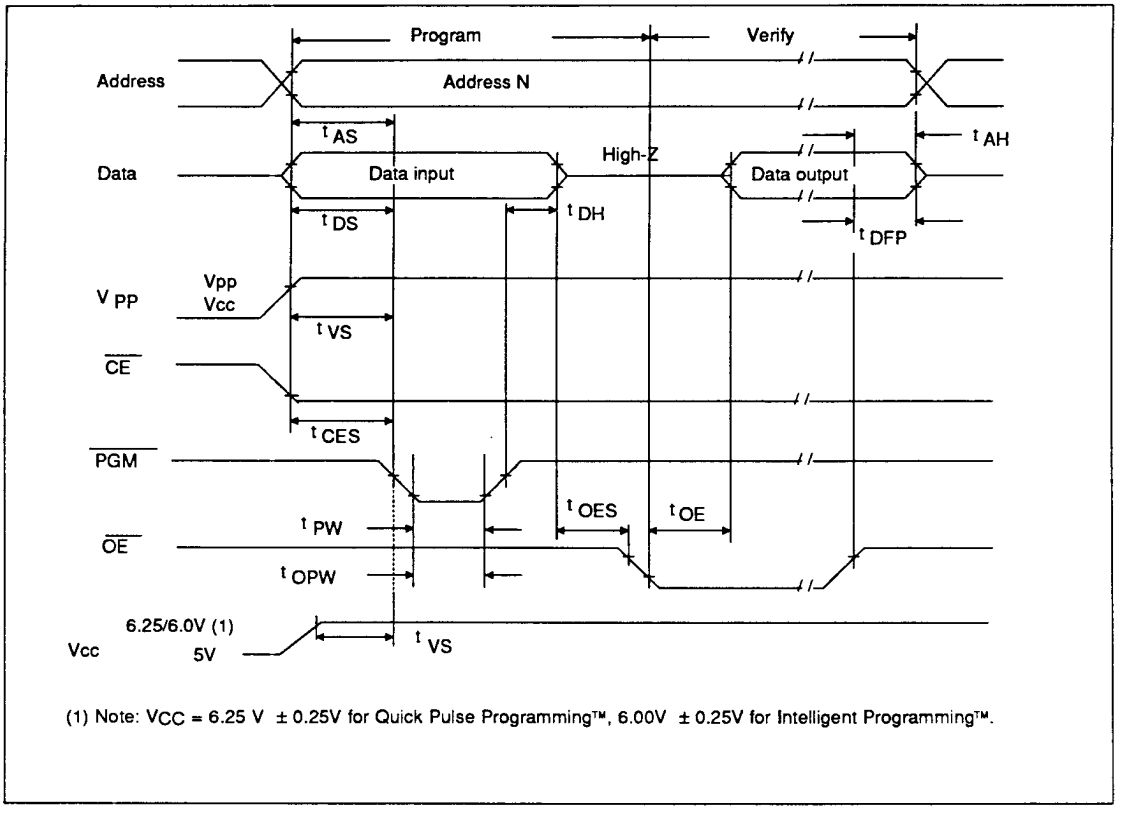
Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{LI}	Input leakage current	$V_{IN} = V_{IH}$ or V_{IL}	-	-	10	µA
I_{PP}	V_{PP} power current	$\overline{CE} = \overline{PGM} = V_{IL}$ All outputs unloaded	-	-	50	mA
I_{CC}	V_{CC} power current	All outputs unloaded	-	-	100	mA
V_{IH}	Input voltage "H" level	-	2.0	-	V_{CC}+1	V
V_{IL}	Input voltage "L" level	-	-0.1	-	0.8	V
V_{OH}	Output voltage "H" level	I_{OH} = -400µA	2.4	-	-	V
V_{OL}	Output voltage "L" level	I_{OL} = 2.1mA	-	-	0.45	V

AC CHARACTERISTICS <Programming Operation>

(V_{CC} = 5.75 - 6.5V, V_{PP} = 12.5V ± 0.5V, T_A = 25°C ± 5°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{AS}	Address set-up time	-	2	-	-	µs
t_{OES}	$\overline{OE}$ set-up time	-	2	-	-	µs
t_{DS}	Data set-up time	-	2	-	-	µs
t_{AH}	Address hold time	-	0	-	-	µs
t_{DH}	Data hold time	-	2	-	-	µs
t_{DFP}	Output enable to output float delay	-	0	-	130	ns
t_{VS}	V_{PP} and V_{CC} power set-up times	-	2	-	-	µs
t_{PW}	$\overline{PGM}$ initial program pulse width	V_{CC} = 6V ±0.25V	0.95	1.0	1.05	ms
t_{PW}	High-speed initial program pulse width	V_{CC} = 6.25V ±0.25V	95	100	105	µs
t_{OPW}	$\overline{PGM}$ overprogram pulse width	V_{CC} = 6V ±0.25V	2.85	-	78.75	ms
t_{CES}	$\overline{CE}$ set-up time	-	2	-	-	µs
t_{OE}	Data valid from $\overline{OE}$	-	-	-	150	ns

TIMING <Programming Operation>



(1) Note: V_{CC} = 6.25 V ± 0.25V for Quick Pulse Programming™, 6.00V ± 0.25V for Intelligent Programming™.

Programming Mode

As shipped, all bits of the OTPROM are in the logic one state. The device is programmed by selectively writing logic zeros into the desired bit locations. To enter the programming mode, V_{CC} and V_{PP} must be adjusted to their programming levels, the device must be selected ($\overline{CE}$ = V_{IL}), outputs are disabled ($\overline{OE}$ = V_{IH}), and a program write pulse must be applied to the $\overline{PGM}$ pin. After the program write pulse, the programmed data may be verified by enabling the outputs ($\overline{OE}$ = V_{IL}) and comparing the written data to the read data. This device is compatible with the Intelligent Programming ™ algorithm, and the Quick Pulse Programming ™ algorithm. Intelligent Programming and Quick Pulse Programming are registered trademarks of Intel Corp. [9/87]

Caution: Exceeding 14V on V_{PP} will permanently damage the device.