Cellular Radio Telephone DATA SAT LSI

Description

CXD1231Q-Z is a DATA SAT modulation / demodulation IC developed for cellular radio telephone.

Usage in conjunction with filter IC CXD1230M provides a modem.

Features

- Conforms with North American AMPS standards and British TACS standards.
- Uses the manchester code decoder with low error rate.
- SAT detection circuit produces few errors even with weak electric field.
- Low power consumption.

Functions

- Decoding of received data.
- Detection of received SAT.
- SAT output with same frequency and phase as received SAT.
- Transmitted DATA, ST encode.

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings

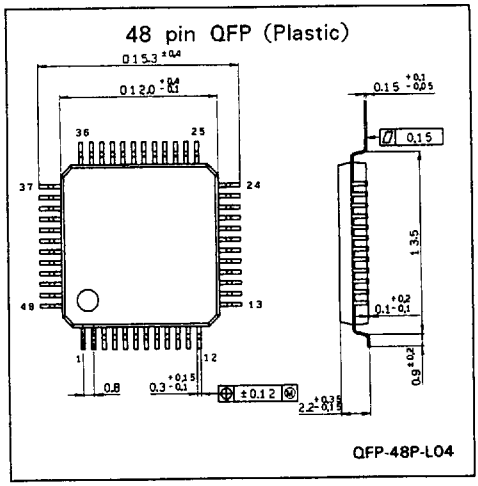
• Supply voltage	V_{DD}	−0.3 to +7.0	V
• Input voltage	V_{IN}	−0.3 to V_{DD}+0.3	V
• Output voltage	V_{OUT}	−0.3 to V_{DD}+0.3	V
• Operating temperature	Topr	−34 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.75 to 5.25	V
• Operating temperature	Topr	−34 to +75	°C

Package Outline

Unit : mm



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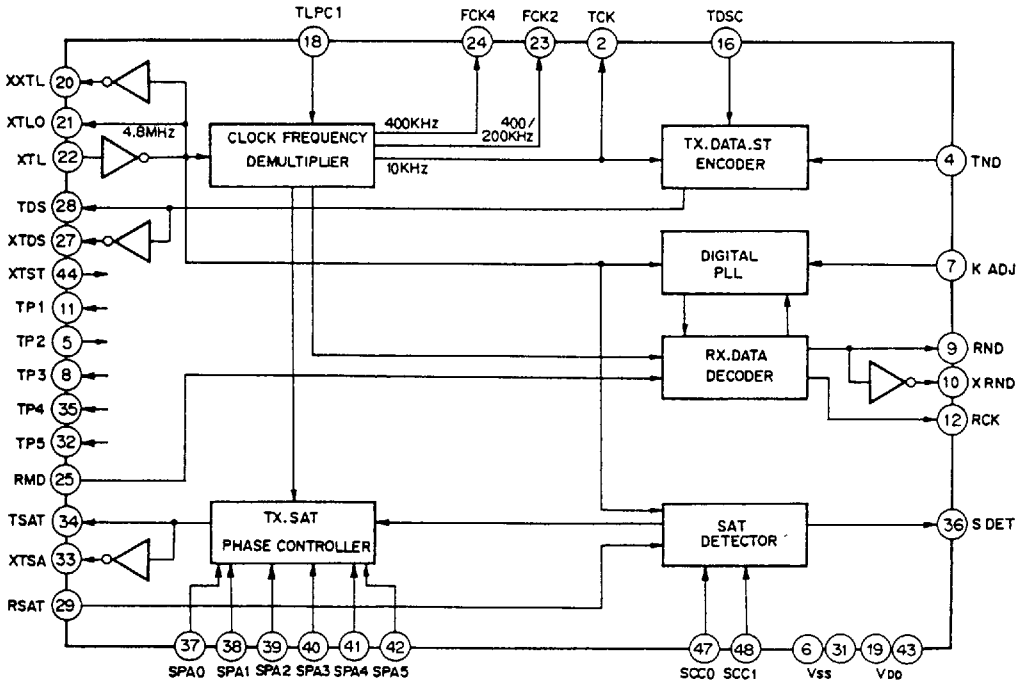
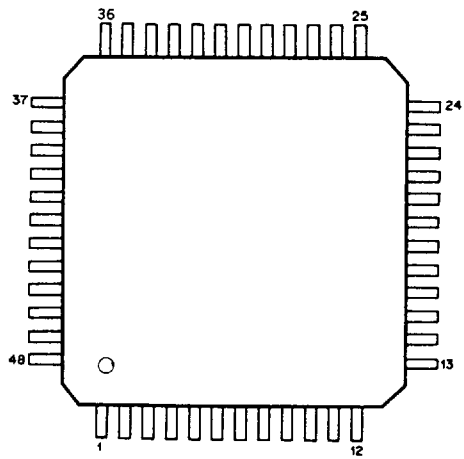
Block Diagram



Pin Configuration (Top View)

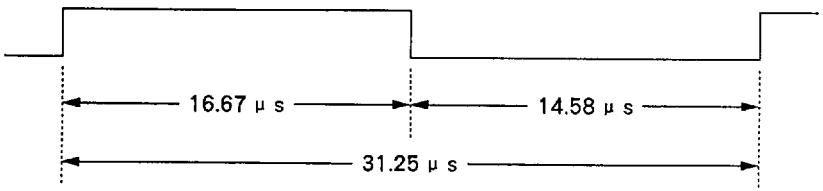


Pin Description

No.	Symbol	I/O	Description
1	NC	——	
2	TCK	O	Clock output of transmitted DATA, ST, 10kHz at AMPS mode and 8kHz at TACS mode.
3	AMPS	I	AMPS/TACS mode select input, AMPS mode at Open and TACS mode at L.
4	TND	I	Transmitted NRZ • DATA input.
5	TP2	I	Test input. Normally fixed at low level.
6	Vss	——	GND
7	KADJ	I	PLL lock range select input for received manchester Data decoder, ±78Hz at high level and ±19.5Hz at low level.
8	TP3	O	Test output.
9	RND	O	Received NRZ DATA output.
10	XRND	O	RND (pin 9) inverting output.
11	TP1	O	Test output.
12	RCK	O	Clock output (10kHz) extracted from received DATA, 10kHz at AMPS mode and 8kHz at TACS mode.
13		——	
14		——	
15	FCK3 *1	O	Clock output of switched capacitor filter, 400kHz at AMPS mode and 320kHz at TACS mode.
16	TDSC	I	ON/OFF control input of received manchester DATA, ST.
17	TLPC2 *2	I	Frequency select input 2 of FCK2 (pin 23).
18	TLPC1 *2	I	Frequency select input 1 of FCK2 (pin 23).
19	V_{DD}	——	+5V
20	XXTL	O	4.8MHz inverting output of XTLO (pin 21).
21	XTLO	I	4.8MHz output of crystal oscillator.
22	XTL	I	Crystal oscillator input or 4.8MHz clock input from the external circuit.
23	FCK2 *2	O	Clock output of switched capacitor filter.
24	FCK4	O	400kHz clock output of switched capacitor filter.
25	RMD	I	Received manchester DATA input.
26	TP6	O	Test output.
27	XTDS	O	TDS (pin 28) inverting output.
28	TDS	O	Transmitted manchester Data, ST output.
29	RSAT	I	Received SAT input.
30	ENBL	I	High impedance control input of TDS (pin 28) and XTDS (pin 27). Output at Open, High impedance at low level.
31	Vss	——	GND
32	TP5	O	Test output.

No.	Symbol	I/O	Description
33	XTSA	O	TSAT (pin 34) inverting output.
34	TSAT	O	Transmitted SAT output.
35	TP4	O	Test output
36	SDET	O	SAT detection output.
37	SPA0	I	Transmitted SAT phase compensation input 0.(LSB).
38	SPA1	I	Transmitted SAT phase compensation input 1.
39	SPA2	I	Transmitted SAT phase compensation input 2.
40	SPA3	I	Transmitted SAT phase compensation input 3.
41	SPA4	I	Transmitted SAT phase compensation input 4.
42	SPA5	I	Transmitted SAT phase compensation input 5.(MSB).
43	V_{DD}	—	+5V
44	XTST	I	Test input, normally fixed at high level.
45	NC	—	
46	NC	—	
47	SCC0	I	SAT color code lower bit input.
48	SCC1	I	SAT color code upper bit input.

*1 320kHz Clock Duty



*2 FCK2 Chart

AMPS	Open ("H")		"L"			
TLPC2	Don't care		Open		"L"	
TLPC1	"H"	"L"	"H"	"L"	"H"	"L"
FCK2	400kHz	200kHz	400kHz	200kHz	320kHz	160kHz

Electrical Characteristics

DC characteristics

V_{DD}=5V±5%, V_{SS}=0V
Topr=−34 to +75°C

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current		I_{DD}	Output no load		5		mA
		I_{DDS}	Static state $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$	0		0.1	mA
Output voltage	H level	V_{OH}	$I_{OH}=-0.4$mA	4.0		V_{DD}	V
	L level	V_{OL}	$I_{OL}=2$mA	V_{SS}		0.4	V
Input voltage	H level	V_{IH}		2.4			V
	L level	V_{IL}				0.8	V
Input leak current		I_{LI}		−10		10	μA

I/O capacitance

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			8	pF
Output pin	C_{OUT}			8	pF

Test conditions : $V_{DD}=V_I=0$V, $f_M=1$MHz

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Functions

CXD1231Q-Z is a DATA and SAT LSI designed for the US cellular radio telephone system. Combined with the switched capacitor filter CXD1230M it conforms with North American AMPS (Advanced Mobile Phone Service) and British TACS (Total Access Communication System) standards.

It features the following functions.

1) Decoding of the received DATA.
2) Detection of the received SAT.
3) SAT transmission in the same frequency and phase as for received.
4) Encoding of the transmitting DATA and ST.

The following is description of each function.

Decoding of the received DATA

With the cellular radio telephone system, DATA for selecting a channel is exchanged between land and mobile stations during cell movement after circuit connection. This DATA is called WIDE BAND DATA coded in the Manchester code. Transfer speed is 20kbaud for AMPS standards and 16kbaud for TACS standards. The following diagram shows the logical values "1" and "0" of the Manchester code.

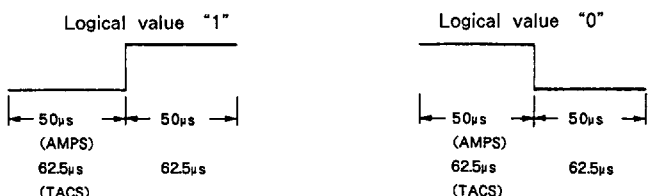

Fig. 1 Manchester code

To decode DATA input in this Manchester code, clock components are extracted by DPLL and the second half values of each bit are picked up using the clock. The decoded DATA is output as NRZ data from the output RND (Pin 9) and XRND (Pin 10) and its bit-clock is output from the output RCK (Pin 12).
Timing of RCK with RND or XRND is shown in Fig. 2.

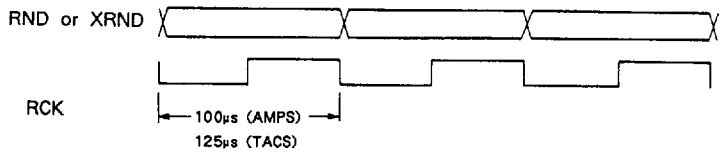

Fig. 2 Timing of RCK with RND or XRND

Detection of the received SAT

With the cellular radio telephone system, sinusoidal wave signals called SAT (Supervisory Audio Tone) are exchanged between land and mobile stations after radio link with either AMPS or TACS standards. SAT has three waves, 5.97kHz, 6.00kHz and 6.03kHz ; frequency is selected from those during cell movement. The selected one is notified in SAT color code to the mobile station by land station. During circuit connection, land and mobile stations confirm each other through reception of the designated SAT frequency.

When SAT signal with the frequency designated in SAT color code is detected, SDET (Pin 36) becomes "H".

SAT transmission with the same frequency and phase as for received

The land station confirms a mobile station through receiving SAT signal in the same frequency and phase as it has transmitted. The mobile station is required to transmit SAT signal in the same frequency and phase as received. For this purpose, the mobile station transmits the signal by phase-correcting DPLL output locked in the received SAT. Connecting the amount of phase depends on the transmitting circuit delay ; this is correctly executed by varying 64 stages in 3.6° steps (0° to 226.8°) and then further shifting the phase by 180° and selecting the output TSAT pin (Pin 34) and XTSA (inversion output of TSAT, Pin 33). Thus the phase can be compensated from 0° to 360° in 3.6° steps.

Table 1 shows the compensated value of the phase assuming that the TSAT output for (SPA5, SPA4, SPA3, SPA2, SPA1, SPA0) = (0, 0, 0, 0, 0, 0) is standard.

Table 1

SPA5	SPA4	SPA3	SPA2	SPA1	SPA0	Phase delay	
						TSAT	XTSA
0	0	0	0	0	0	0°	180°
0	0	0	0	0	1	3.6°	183.6°
0	0	0	0	1	0	7.2°	187.2°
⋮						⋮	⋮
1	1	0	0	0	0	172.8°	352.8°
1	1	0	0	0	1	176.4°	356.4°

Phase delay at pins TSAT and XTSA assuming that TSAT output for (SPA5, SPA4, SPA3, SPA2, SPA1, SPA0) = (0, 0, 0, 0, 0, 0) is standard.

Encoding of the transmitting DATA and ST

ST is a signal transmitted when conversation ends or when the bell is rang. The frequency is 10kHz for AMPS and 8kHz for TACS standards. It is output from TDS (Pin 28) and XTDS (Pin 27) with the DATA and ST (NRZ) input to TND (Pin 4), In synchronization with the clock output from TCK (Pin 2), and encoded in the Manchester code. However, it does not transmit the encoded data when the control input TDSC (Pin 16) is at "L" but fixes TDS to "H" and XTDS to "L".

Timing of TCK and TND is shown in Fig. 3.

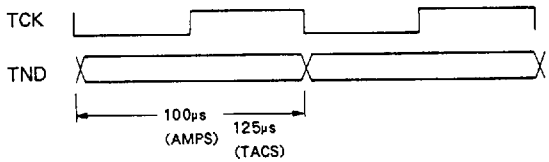

Fig. 3 Timing of TCK and TND

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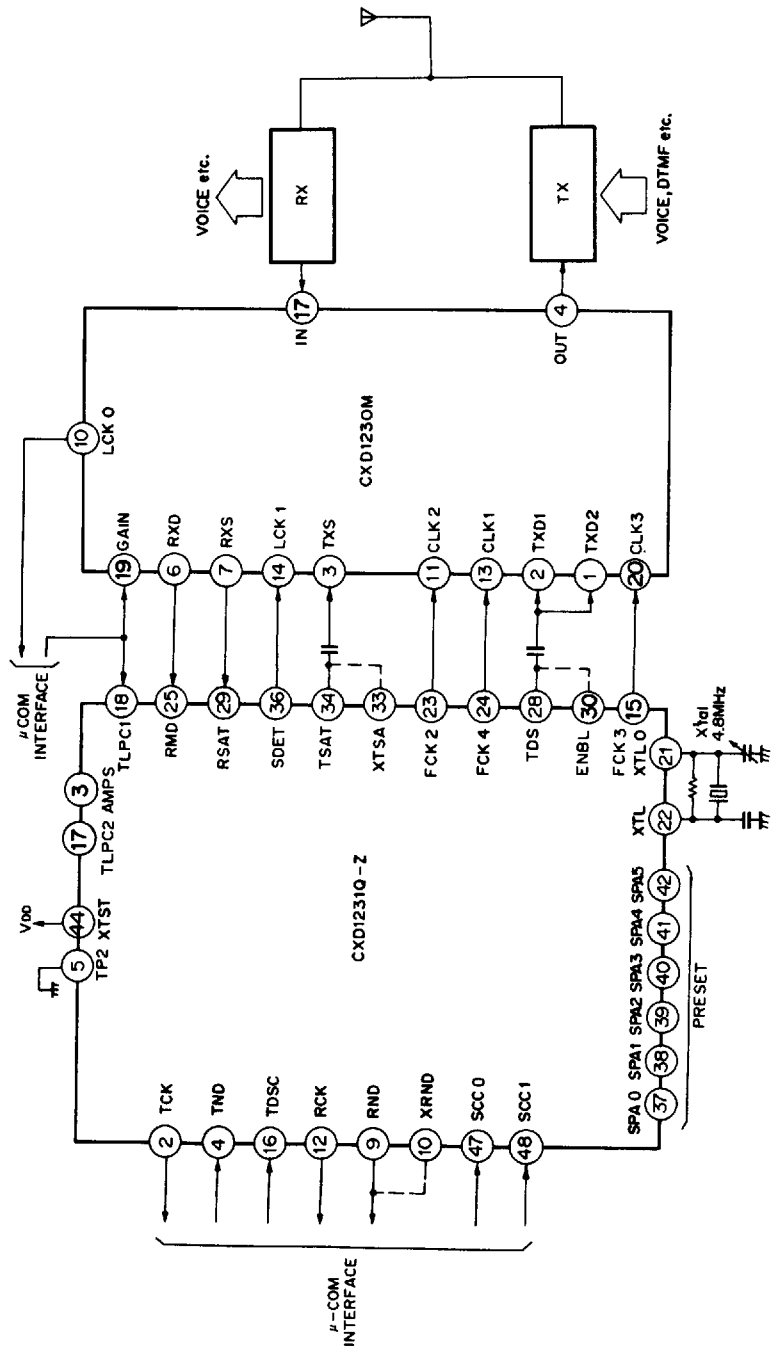
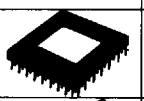
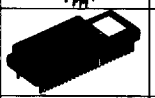
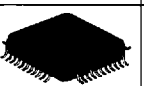
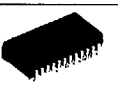
Application Circuit



Package Name

Type		Package name		Package	Features			
		Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction
Inserted	Standard	DIP	DUAL IN-LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		SIP	SINGLE IN LINE PACKAGE		P	2.54mm (100MIL)	Through Hole Lead	1-direction
		ZIP	ZIG ZAG IN-LINE PACKAGE		P	2.54mm (100MIL) Zig-Zag in-line	Through Hole Lead	1-direction
		PGA	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	Package under side
		PIGGY BACK	PIGGY BACK		C	2.54mm (100MIL)	Through Hole Lead	2-direction
	Shrink	SDIP	SHRINK DUAL IN-LINE PACKAGE		P	1.778mm (70MIL)	Through Hole Lead	2-direction
		SZIP	SHRINK ZIG-ZAG IN-LINE PACKAGE		P	1.778mm (70MIL) Zig-Zag in-line	Through Hole Lead	1-direction
Surface mounted	Standard flat package	QFP	QUAD FLAT L LEADED PACKAGE		P C	1.0mm 0.8mm 0.65mm	Gull-Wing	4-direction
		SOP	SMALL OUTLINE L-LEADED PACKAGE		P	1.27mm (50MIL)	Gull-Wing	2-direction
	Standard 2-direction chip carrier	SOJ	SMALL OUTLINE J-LEADED PACKAGE		P	1.27mm (50MIL)	J-Lead	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE		P	0.5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE		P	0.65mm	Gull-Wing	2-direction
		TSOP	THIN SMALL OUTLINE PACKAGE		P	0.5mm (0.55mm)	Gull-Wing	2-direction
	Standard chip carrier	QFJ	QUAD FLAT J-LEADED PACKAGE		P	1.27mm (50MIL)	J-Lead	4-direction
		QFN	QUAD FLAT NON-LEADED PACKAGE		C	1.27mm (50MIL)	Leadless	Package under side

*P·····Plastic, C···Ceramic

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