CYPRESS SEMICONDUCTOR

65,536 x 8 Reprogrammable Fast Column Access PROM

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **Unique fast column access**
  - **— t_{AA} = 20 ns (commercial)**
  - **— t_{AA} = 25 ns (military)**
- **WAIT signal**
- **User configurable chip select decoding (7C289)**
- **EPROM technology, 100% programmable**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Slim 300-mil package**
- **Capable of withstanding >2001V static discharge**

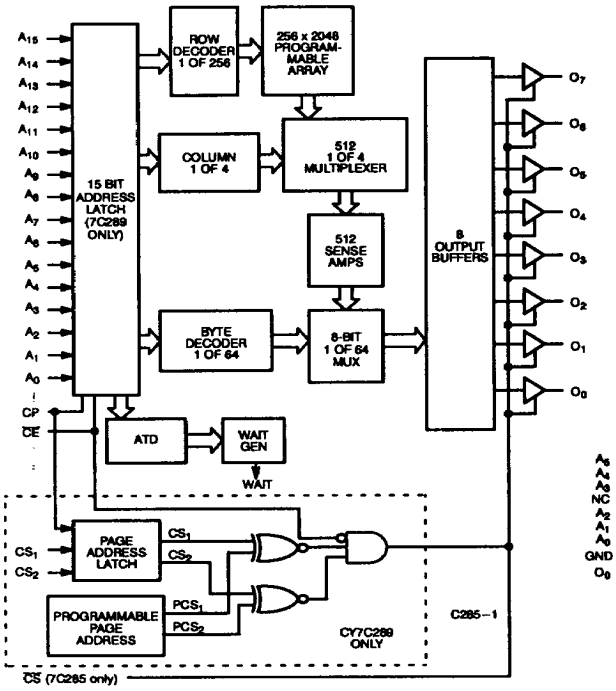
Functional Description

The CY7C285 and the CY7C289 are high-performance 65,536 by 8-bit CMOS PROMs. The CY7C285 is available in a 28-pin 300-mil package. It features a unique fast column access feature that allow access times as fast as 20 ns for each byte in a 64-byte page. There are 1024 pages in the device. The access time when changing pages will be 65 ns. In order to easily facilitate the use of the fast column access feature, a WAIT signal will be generated to advise the processor of a page change. The CY7C289 also incorporates the fast column access feature and through the use of the ALE option adds either synchronous address registers or asynchronous address latches. The CY7C289 is particularly well suited to support applications using the CY7C601 as well as other RISC or CISC microprocessors. It is available in a 32-pin 300-mil package.

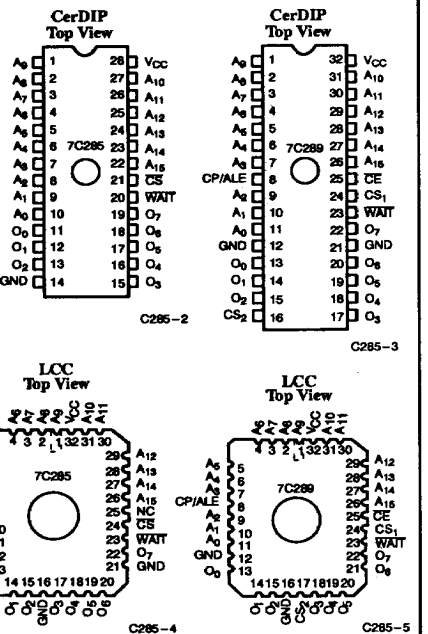
The CY7C285 and CY7C289 offer the advantage of low power, superior performance, and programming yield. The EPROM cell requires only 12.5V for the super voltage and low current requirements. The EPROM cells allow for each memory location to be 100% tested, with each location being written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

Reading the CY7C285 is accomplished by placing an active LOW signal on the $\overline{CS}$ pin. Reading the CY7C289 is accomplished by placing an active LOW signal on the $\overline{CE}$ pin and by placing active HIGH signals on the CS_1 or CS_2 pins as appropriate. The contents of the memory location addressed by the address lines (A_0 – A_{15}) will become available on the output lines (O_0 – O_7).

Logic Block Diagram



Pin Configurations



Selection Guide

	Description		7C285–65 7C289–65	7C285–75 7C289–75	7C285–85 7C289–85
Maximum Access Time (ns)	Page Access Time		65	75	85
	Column Access Time		20	25	35
Maximum Operating Current (mA)		Commercial	180	180	180
		Military		200	200

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential (CY7C285: Pin 28 to Pin 14) (CY7C289: Pin 32 to Pin 12, 21) ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

DC Program Voltage (CY7C285: Pin 22; CY7C289: Pin 26) 13.0V

UV Exposure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[1]	– 40°C to +85°C	5V ± 10%
Military[2]	– 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3, 4]

Parameters	Description	Test Conditions		7C285–65, 75, 85 7C289–65, 75, 85 Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 2.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA[5]			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8	V
V_{CD}	Input Diode Clamp Voltage			Note 4		V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		– 10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		– 40	+40	μA
I_{OS}	Output Short Circuit Current[6]	V_{CC} = Max., V_{OUT} = GND		– 20	– 90	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		180	mA
			Mil		200	mA

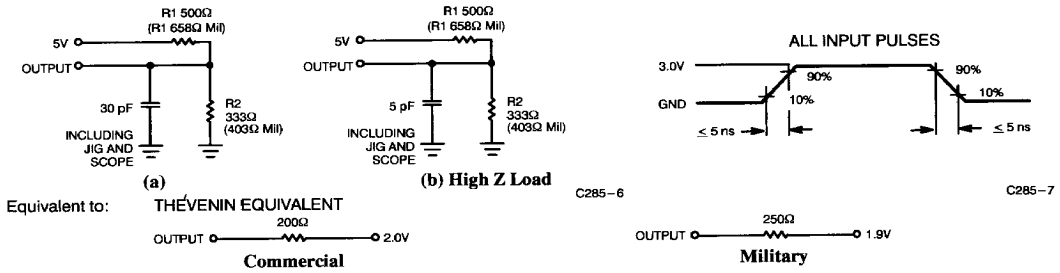
Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

1. Contact a Cypress representative for industrial temperature range specification.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See Introduction to CMOS PROMs in this Data Book for general information on testing.
5. I_{OL} = 6.0 mA for military 7C285, I_{OL} = 4.0 mA for commercial 7C289, and I_{OL} = 3.0 mA for military 7C289.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

AC Test Loads and Waveform[4, 7]



Notes:

7. Note that R1 and R2 for the 7C7C289 will be 961Ω and 510Ω for commercial (Thévenin equivalent is 333Ω to 1.73V) and 1250Ω and 588Ω for military (Thévenin equivalent is 400Ω to 1.6V).

7C285 Switching Characteristics Over the Operating Range[3, 4]

Parameters	Description	7C285–65		7C285–75		7C285–85		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RAC}	Slow Address Access Time (A_6 – A_{15})		65		75		85	ns
t_{CAA}	Fast Address Access Time (A_0 – A_5)		20		25		35	ns
t_{HZCS}	Output High Z from $\overline{CS}$		15		20		25	ns
t_{ACS}	Output Valid from $\overline{CS}$		15		20		25	ns
t_{WD}	Wait Delay from First Slow Address Change		20		25		35	ns
t_{DW}	Wait Hold from Data Valid	0		0		0		ns
t_{WW}	Wait Recovery from Last Address Change		90		110		120	ns
t_{PWD}	Wait Pulse Width	10		12		15		ns

7C289 Switching Characteristics Over the Operating Range[3, 4]

Parameters	Description	7C289–65		7C289–75		7C289–85		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RAC1}	Slow Address Access Time (A_6 – A_{15})		65		75		85	ns
t_{CAA1}	Fast Address Access Time (A_0 – A_5)		20		25		35	ns
t_{AR1}	Register Address Set-Up Time	2		4		8		ns
t_{RA1}	Register Address Hold Time	6		6		10		ns
t_{AR2}[8]	Register Address Set-Up	8		10		15		ns
t_{RA2}[8]	Register Address Hold Time	2		4		8		ns
t_{HZCS}	Output High Z from Clock HIGH		20		20		25	ns
t_{ACS}	Output Valid from Clock HIGH		20		20		25	ns
t_{PWC}	Clock Pulse Width	11		13		15		ns
t_{ADH}	Data Hold Time	5		5		5		ns
t_{SCE}	Chip Enable Set-Up	2		4		8		ns
t_{HCE}	Chip Enable Hold	6		6		10		ns

Notes:

8. Parameters for the 7C289 with t_{AS} option enabled.

Switching Characteristics for the 7C289 Over the Operating Range[3, 4] (continued)

Parameters	Description	7C289–65		7C289–75		7C289–85		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WD1}	Wait Delay from Clock LOW	0	19	0	25	0	30	ns
t_{WD3}[9]	Wait Delay from Clock HIGH	0	16	0	20	0	25	ns
t_{RAC2}[10]	Slow Address Access Time (A_6 – A_{15})		65		75		85	ns
t_{CAA2}[10]	Fast Address Access Time (A_0 – A_5)		22		30		35	ns
t_{ACE}[10]	Output Valid from $\overline{CE}$		20		25		30	ns
t_{HZCE}[10]	Output High Z from $\overline{CE}$		20		25		30	ns
t_{AL}[10]	Address Set-Up Time	5		8		12		ns
t_{LA}[10]	Address Hold Time	10		12		15		ns
t_{LL}[10]	ALE Pulse Width	10		12		15		ns
t_{PWD}[10]	Wait Pulse Width	10		12		15		ns
t_{WD2}[10]	Wait Delay from First Slow Address Change		21		25		30	ns
t_{DW2}[10]	Wait Hold from Data Valid	0		0		0		ns
t_{WW2}[10]	Wait Recovery from Last Address Change		90		110		120	ns
t_{CES}[10]	$\overline{CE}$ Set-Up Time for High Z Outputs	3		4		8		ns

Architecture Configuration Bits (7C289 only)

Architecture Bit	Architecture Verify D_0 – D_7		Function
TAS	D_1	0 = Erased	Address Set-Up < Address Hold
		1 = PGMED	Address Set-Up > Address Hold
ALE	D_2	0 = Erased	Input Registered (ADDR, $\overline{CE}$, CS_1, CS_2)
		1 = PGMED	Input Latched (ADDR, $\overline{CE}$, CS_1, CS_2)
ALEP	D_3	0 = Erased	ALE = LOW, Addresses Latched
		1 = PGMED	ALE = HIGH, Addresses Latched
WAITC	D_4	0 = Erased	WAIT Follows the Falling Edge of CP
		1 = PGMED	WAIT Follows the Rising Edge of CP
WAITP	D_5	0 = Erased	WAIT Signal Active LOW
		1 = PGMED	WAIT Signal Active HIGH
CS1E	D_6	0 = Erased	CS_1 (Pin 24) = LOW, Disables Outputs
		1 = PGMED	CS_1 (Pin 24) = HIGH, Disables Outputs
CS2E	D_7	0 = Erased	CS_2 (Pin 16) = LOW, Disables Outputs
		1 = PGMED	CS_2 (Pin 16) = HIGH, Disables Outputs

Bit Map

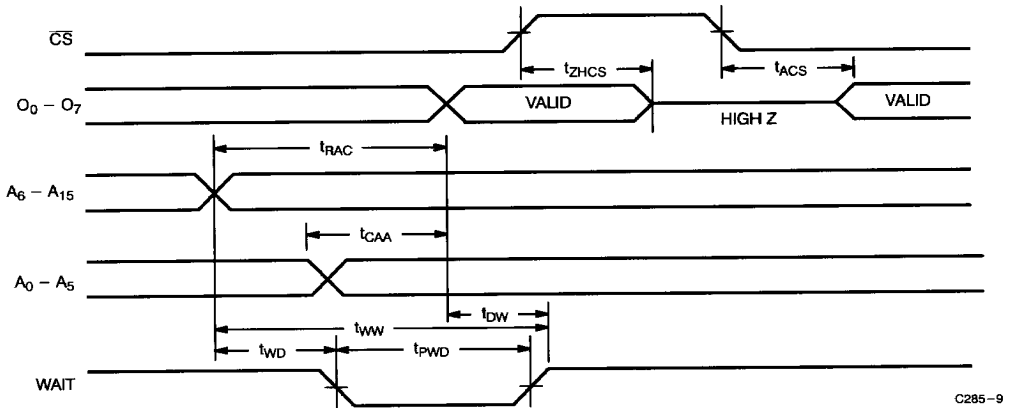
Programmer Address (Hex.)	RAM Data
0000	Data
.	.
.	.
FFFF	Data
10000	Control Byte

Architecture Byte (10000H)

D_7							D_0
C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0

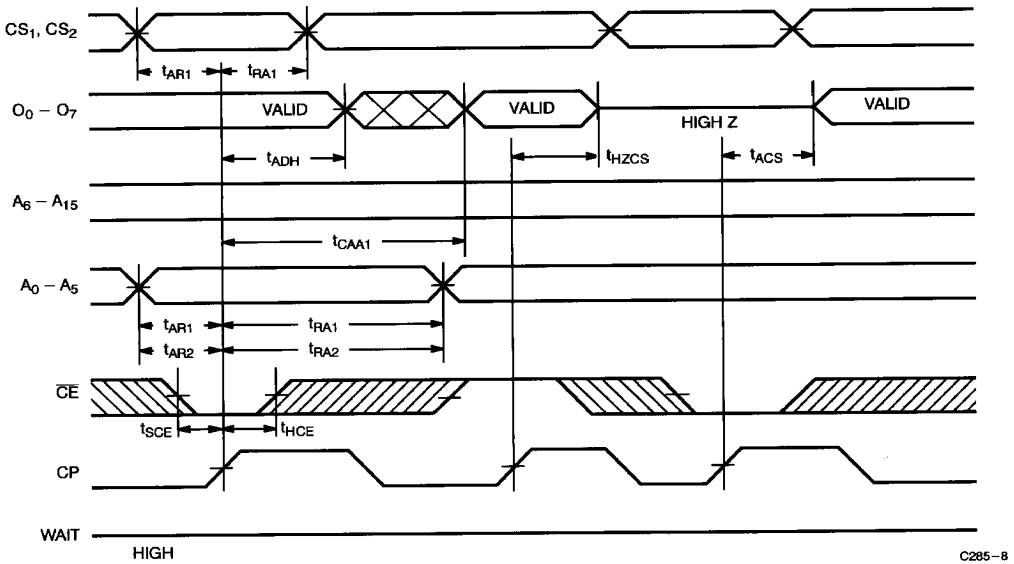
Notes:
9. Parameters for the 7C289 with WAITC option enabled.
10. Parameters for the 7C289 with ALE option enabled.

Switching Waveform for the 7C285



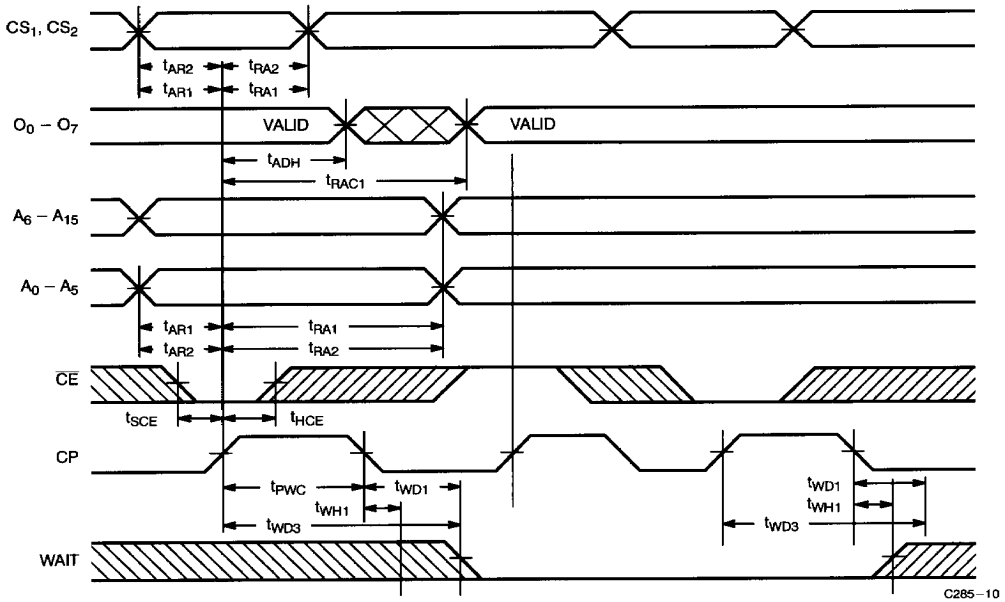
Switching Waveforms for the 7C289

Fast Column Access

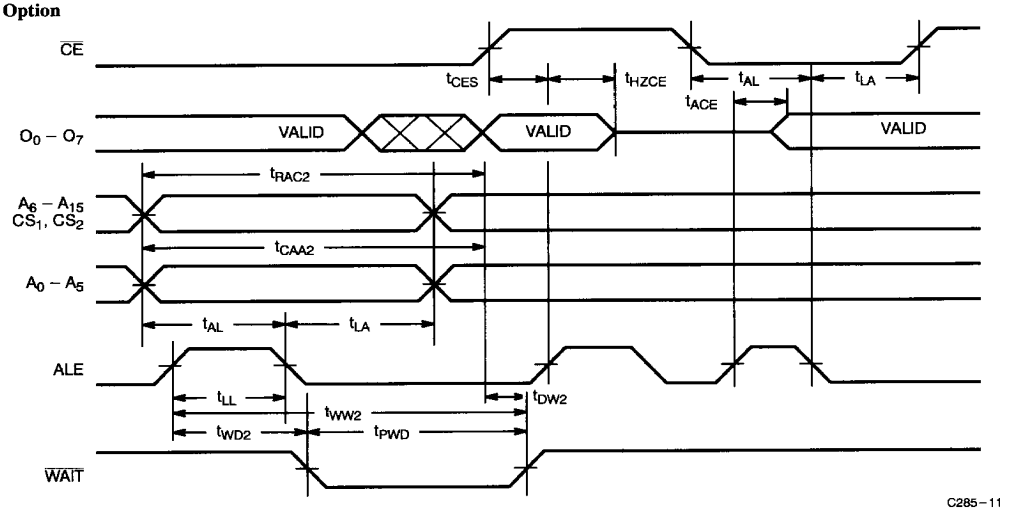


Switching Waveforms for the 7C289 (continued)

Using WAIT



ALE Option



CYPRESS SEMICONDUCTOR

Erasure Characteristics

Wavelengths of light less than 4000 angstroms begin to erase the 7C285 and 7C289 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 angstroms for a minimum dose (UV intensity multipled by exposure time) or 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The 7C285 or 7C289 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. CY7C285 Mode Selection

Mode		Pin Function				
	Read or Output Disable	A_{15}	A_{14}	$\overline{CS}$	$\overline{WAIT}$	$O_7 - O_0$
	Other	V_{PP}	LATCH	$\overline{PGM}$	$\overline{VFY}$	$D_7 - D_0$
Read (within a page: $A_6 - A_{15}$ stable)		A_{15}	A_{14}	V_{IL}	One	$O_7 - O_0$
Read (page break: $A_6 - A_{15}$ transition)		A_{15}	A_{14}	V_{IL}	Pulse LOW	$O_7 - O_0$
Output Disable		A_{15}	A_{14}	V_{IH}	Output	High Z
Program		V_{PP}	V_{ILP}	V_{ILP}	V_{IHP}	$D_7 - D_0$
Program Inhibit		V_{PP}	V_{ILP}	V_{IHP}	V_{IHP}	High Z
Program Verify		V_{PP}	V_{ILP}	V_{IHP}	V_{ILP}	$O_7 - O_0$
Blank Check		V_{PP}	V_{ILP}	V_{IHP}	V_{ILP}	Zeros

Table 2. CY7C289 Mode Selection

Mode		Pin Function[11]							
	Read or Output Disable	A_9	A_8	A_6	A_5	A_4	A_3	A_{15}	A_{14}
	Other	A_9	A_8	A_6	A_5	A_4	A_3	V_{PP}	LATCH
Registered Input Read (FCA)		A_9	A_8	A_6	A_5	A_4	A_3	A_{15}	A_{14}
Registered Input Read (page break)		A_9	A_8	A_6	A_5	A_4	A_3	A_{15}	A_{14}
Latched Input Read (FCA)		A_9	A_8	A_6	A_5	A_4	A_3	A_{15}	A_{14}
Latched Input Read (page break)		A_9	A_8	A_6	A_5	A_4	A_3	A_{15}	A_{14}
Output Disable		A_9	A_8	A_6	A_5	A_4	A_3	A_{15}	A_{14}
Output Disable (default architecture)		A_9	A_8	A_6	A_5	A_4	A_3	A_{15}	A_{14}
Output Disable (default architecture)		A_9	A_8	A_6	A_5	A_4	A_3	A_{15}	A_{14}
Program		A_9	A_8	A_6	A_5	A_4	A_3	V_{PP}	V_{ILP}
Program Inhibit		A_9	A_8	A_6	A_5	A_4	A_3	V_{PP}	V_{ILP}
Program Verify		A_9	A_8	A_6	A_5	A_4	A_3	V_{PP}	V_{IHP}
Blank Check		A_9	A_8	A_6	A_5	A_4	A_3	V_{PP}	V_{ILP}
Program Address Set-Up/Hold Option		V_{HH}	V_{IHP}	V_{ILP}	X	X	V_{ILP}	V_{PP}	V_{ILP}
Program Address/Latch Option		V_{HH}	V_{IHP}	V_{IHP}	X	X	V_{ILP}	V_{PP}	V_{ILP}
Program ALE Polarity Option		V_{HH}	V_{IHP}	V_{ILP}	X	X	V_{IHP}	V_{PP}	V_{ILP}
Program Edge Trigger for WAIT		V_{HH}	V_{ILP}	V_{IHP}	X	X	V_{ILP}	V_{PP}	V_{ILP}
Program WAIT Polarity		V_{HH}	V_{ILP}	V_{IHP}	X	X	V_{IHP}	V_{PP}	V_{ILP}
Program CS_1, CS_2 Polarity		V_{HH}	V_{IHP}	V_{IHP}	CS_2	CS_1	V_{IHP}	V_{PP}	V_{ILP}

Table 2. CY7C289 Mode Selection (continued)

Mode		Pin Function[11]					
	Read or Output Disable	CS_1	CS_2	$\overline{CE}$	CP/AL	$\overline{WAIT}$	$O_7 - O_0$
	Other	$\overline{PGM}$	GND	NC	NC	$\overline{VFY}$	$D_7 - D_0$
Registered Input Read (FCA)		V_{IL}	V_{IL}	V_{IL}	CLK	One	$O_7 - O_0$
Registered Input Read (page break)		V_{IL}	V_{IL}	V_{IL}	CLK	Zero	$O_7 - O_0$
Latched Input Read (FCA)		V_{IL}	V_{IL}	V_{IL}	LATCH	One	$O_7 - O_0$
Latched Input Read (page break)		V_{IL}	V_{IL}	V_{IL}	LATCH	Pulse LOW	$O_7 - O_0$
Output Disable		X	X	V_{IH}	X	Output	High Z
Output Disable (default architecture)		X	V_{IL}	X	X	Output	High Z
Output Disable (default architecture)		V_{IL}	X	X	X	Output	High Z
Program		V_{ILP}	V_{ILP}	X	X	V_{IHP}	$D_7 - D_1$
Program Inhibit		V_{IHP}	V_{ILP}	X	X	V_{IHP}	High Z
Program Verify		V_{IHP}	V_{ILP}	X	X	V_{ILP}	$O_7 - O_1$
Blank Check		V_{IHP}	V_{ILP}	X	X	V_{ILP}	Zeros
Program Address Set-Up/Hold Option		V_{ILP}	V_{ILP}	X	X	V_{IHP}	X
Program Address/Latch Option		V_{ILP}	V_{ILP}	X	X	V_{IHP}	X
Program ALE Polarity Option		V_{ILP}	V_{ILP}	X	X	V_{IHP}	X
Program Edge Trigger for WAIT		V_{ILP}	V_{ILP}	X	X	V_{IHP}	X
Program WAIT Polarity		V_{ILP}	V_{ILP}	X	X	V_{IHP}	X
Program CS_1, CS_2 Polarity		V_{ILP}	V_{ILP}	X	X	V_{IHP}	X

Note:
11. X = "don't care" but not to exceed $V_{CC} \pm 5\%$.

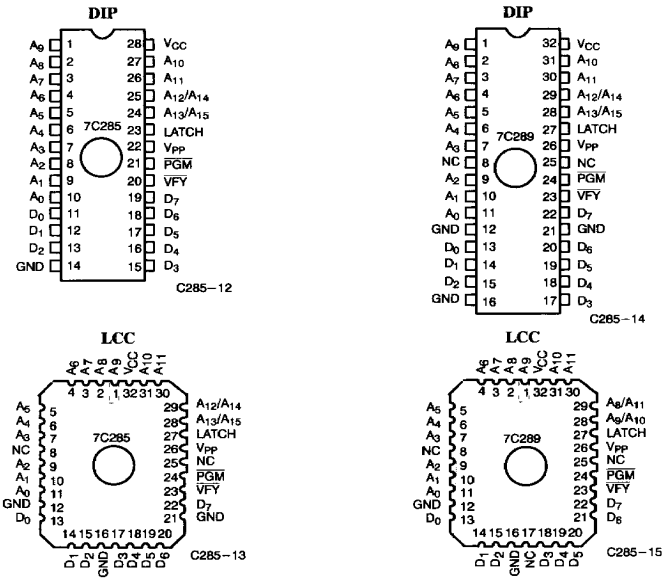


Figure 1. Programming Pinouts

Ordering Information[12]

Speed (ns)	Ordering Code	Package Type	Operating Range
65	CY7C285-65PC	P21	Commercial
	CY7C285-65WC	W22	
75	CY7C285-75PC	P21	Commercial
	CY7C285-75WC	W22	
	CY7C285-75DMB	D22	Military
	CY7C285-75LMB	L55	
	CY7C285-75QMB	Q55	
	CY7C285-75WMB	W22	
85	CY7C285-85PC	P21	Commercial
	CY7C285-85WC	W22	
	CY7C285-85DMB	D22	Military
	CY7C285-85LMB	L55	
	CY7C285-85QMB	Q55	
	CY7C285-85WMB	W22	

Speed (ns)	Ordering Code	Package Type	Operating Range
65	CY7C289-65WC	W32	Commercial
75	CY7C289-75WC	W32	Commercial
	CY7C289-75DMB	D32	Military
	CY7C289-75LMB	L55	
	CY7C289-75QMB	Q55	
	CY7C289-75WMB	W32	
85	CY7C289-85WC	W32	Commercial
	CY7C289-85DMB	D32	Military
	CY7C289-85LMB	L55	
	CY7C289-85QMB	Q55	
	CY7C289-85WMB	W32	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{CAA}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11
t_{ACE}[13]	7, 8, 9, 10, 11

Notes:

12. Most of these products are available inindustrial temperature range. Contact a Cypress representative for specifications and product availability.
13. CY7C289 only.

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