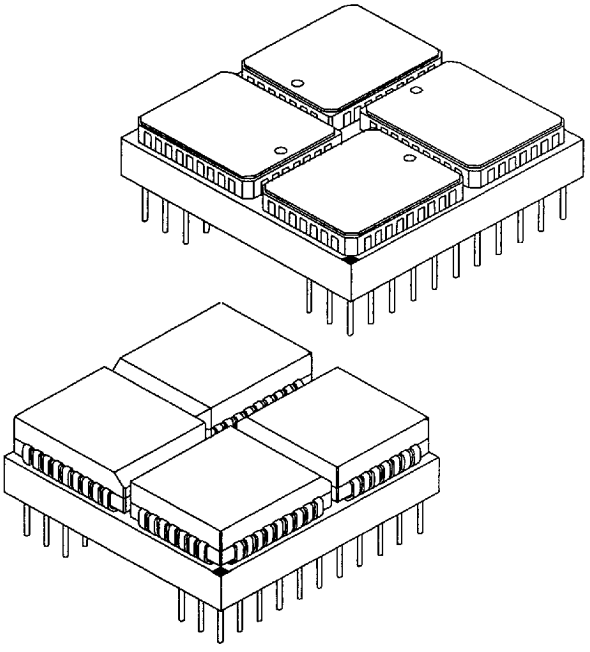
DESCRIPTION:

The DPZ128X32VA/VAP is a 4 megabit CMOS FLASH Electrically Erasable and Programmable nonvolatile memory module. The module is built with four 128K x 8 FLASH memory devices. The DPZ128X32VA/VAP can be user configurable as 512K x 8, 256K x 16 or 128K x 32 bits.

The DPZ128X32VA/VAP is ideal for use in systems that require periodic code updates, or for use as a high speed nonvolatile storage medium.

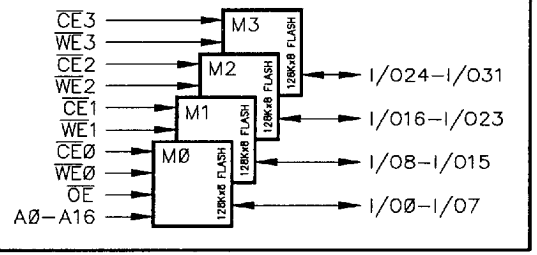


FEATURES:

- User Definable Configurations:
  512K x 8, 256K x 16 or 128K x 32
- Fast Read Access Times: 90*, 120, 150, 200ns
- Low Power:
  120mA Maximum Active (32 bit Mode)
  400µA Maximum Standby (CMOS)
- 1,000 Erase/Program Cycles Minimum
- Command Register Architecture for Microprocessor Compatible Write Interface.
- 12.0V ±5% V_{PP}
- TTL-Compatible Inputs and Outputs
- Military Versions Available with All Devices used to Construct the Module Compliant to MIL-STD-883; Class B
- 66-Pin Ceramic PGA

* Commercial Only.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES	
A0 - A16	Address Inputs
I/O0 - I/O31	Data In/Out
$\overline{CE0}$ - $\overline{CE3}$	Chip Enables
$\overline{WE0}$ - $\overline{WE3}$	Write Enables
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

PIN-OUT DIAGRAM

1	I/08	12	$\overline{WE1}$	23	I/015					34	I/024	45	VDD	56	I/031
2	I/09	13	$\overline{CE1}$	24	I/014					35	I/025	46	$\overline{CE3}$	57	I/03Ø
3	I/01Ø	14	VSS	25	I/013					36	I/026	47	$\overline{WE3}$	58	I/029
4	A13	15	I/011	26	I/012					37	A6	48	I/027	59	I/028
5	A14	16	A1Ø	27	$\overline{OE}$					38	A7	49	A3	6Ø	AØ
6	A15	17	A11	28	N.C.		(TOP VIEW)			39	N.C.	5Ø	A4	61	A1
7	A16	18	A12	29	$\overline{WEØ}$					4Ø	A8	51	A5	62	A2
8	N.C.	19	VDD	3Ø	I/07					41	A9	52	$\overline{WE2}$	63	I/023
9	I/ØØ	2Ø	$\overline{CEØ}$	31	I/06					42	I/016	53	$\overline{CE2}$	64	I/022
1Ø	I/01	21	N.C.	32	I/05					43	I/017	54	VSS	65	I/021
11	I/02	22	I/03	33	I/04					44	I/018	55	I/019	66	I/02Ø

DEVICE OPERATION:

The DPZ128X32VA/VAP is an electrically erasable and programmable memory that functions similar to an EPROM type device, but can be erased without removing it from the system and exposing it to ultraviolet light. Each 128K x 8 device on the module can be erased individually eliminating the need to re-program the entire module when partial code changes are required.

READ:

With $V_{PP} = 0V$ to $V_{DD} + 2.0V$ *(V_{PPLO})*, the DPZ128X32VA/VAP is a read-only memory and can be read like a standard EPROM. The module can be read as a 32 bit, 16 bit or an 8 bit device. $\overline{CE}0$ thru $\overline{CE}3$ select the device to be read. After a device is selected, $\overline{OE}$ is set to a logic-low level to enable the outputs of the module.

When $V_{PP} = 12.0V \pm 0.6V$ *(V_{PPHI})*, reads can be accomplished in the same manner as described above but must be preceded by writing 00H to the command register prior to reading the device. When V_{PP} is raised to V_{PPHI} the contents of the command register default to 00H and remain that way until the command register is altered.

STANDBY:

When $\overline{CE}0$ thru $\overline{CE}3$ are raised to a logic-high level, the standby operation disables the DPZ128X32VA/VAP reducing the power consumption substantially. The outputs are placed in a high-impedance state, independent of the $\overline{OE}$ input. If the module is deselected during programming, erasure, or program/erase verification, the device upon which the operation was being performed will continue to draw active current until the operation is completed.

PROGRAM:

The DPZ128X32VA/VAP programming and erasing functions are accessed via the command register when high voltage is applied to V_{PP}. The contents of the command register control the functions of the memory device *(see Command Definition Table)*.

The command register is not an addressable memory location. The register stores the address, data, and command information required to execute the command. When $V_{PP} = V_{PPLO}$ the command register is reset to 00H returning the device to the read-only mode.

The command register is written by enabling the device upon which the operation is to be performed *(see Truth Table)*. While the device is enabled bring $\overline{WE}$ to a logic-low (V_{IL}), the address is latched on the falling edge of $\overline{WE}$ and data is latched on the rising edge of $\overline{WE}$. Programming is initiated by writing 40H *(program setup command)* to the command register. On the next falling edge of $\overline{WE}$ the address to be programmed will be latched followed by the data being latched on the rising edge of $\overline{WE}$ *(see AC Operating and Characteristics Table)*.

PROGRAM VERIFY:

The DPZ128X32VA/VAP is programmed one byte at a time. Each byte may be programmed sequentially or at random. Following each programming operation, the byte must be verified.

To initiate the program-verify mode, C0H must be written to the command register of the device just programmed. The programming operation is terminated on the rising edge of $\overline{WE}$ the program-verify command is written to the command register.

After the program-verify command is written to the command register, the memory device applies an internally generated margin voltage to the byte just written. After waiting t_{WHGL}, the byte can be verified by doing a read. If true data is read from the device, the byte write was successful and the next byte may be programmed.

If the device fails to verify, the program/verify operation is repeated up to 25 times. Failure to verify after 25 program/verify operations indicates a failed device. Most bytes will program on the first or second write.

ERASE:

The DPZ128X32VA/VAP can be erased one 128K x 8 device at a time or two devices can be erased if using the module as a x16 or x32 bit device. The erase function is a command-only operation and can only be executed while $V_{PP} = V_{PPHI}$.

To setup the chip-erase, 20H must be written to the command register. The chip-erase is then executed by once again writing 20H to the command register *(see AC Operating and Characterstics Table)*.

To ensure a reliable erasure, all bits in the device to be erased should be programmed to their charged state *(data = 00H)* prior to starting the erase operation. With the algorithm provided, this operation should take approximately 2 minutes.

ERASE VERIFY:

The erase operation erases all bytes in the device selected in parallel. Upon completion of the erase operation, each byte must be verified. This operation is initiated by writing A0H to the command register. The address to be verified must be supplied because it is latched on the falling edge of $\overline{WE}$.

The memory device internally generates a margin voltage and applies it to the addressed byte. If FFH is read from the device, it indicates the byte is erased. The erase/verify command is issued prior to each byte verification to latch the address of the byte to be verified. This continues until FFH is not read from the device or the last address for the device being erased is read.

If FFH is not read from the byte being verified, an additional erase operation is performed. Verification then resumes from the last byte verified. Once all bytes in the device being erased are verified, the erase

operation is complete. The verify opertation should now be terminated by writing a valid command such as program set-up to the command register.

RESET:

The reset command is provided as a way to safely abort a program or erase command operation. Following either the program setup command *(40H)* or the set-up erase command *(20H)*, two consecutive writes of FFH will safely abort either operation. If the reset command is issued prior to the program command or the erase command, the memory contents will not be altered. A valid command must then be written to put the device in another mode.

DESIGN CONSIDERATIONS:

V_{PP} traces should use similar trace widths and layout considerations as the V_{DD} power bus. The V_{PP} supply traces should also be decoupled to help decrease voltage spikes.

Power-up sequencing should be such that V_{PP} doesn't go above $V_{DD}+2.0V$ before V_{DD} reaches a steady state voltage, while on power-down V_{PP} should be below $V_{DD}+2.0V$ before V_{DD} is lowered.

While the DPZ128X32VA/VAP memory module has high-frequency, low-inductance decoupling capacitors mounted on the substrate connected to V_{DD} and V_{SS}, it is recommended that a 4.7µF to 10µF electrolytic capacitor be placed near the memory module connected across V_{DD} and V_{SS} for bulk storage.

TRUTH TABLE

MODE		$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	V_{PP}	DATA I/O
READ - ONLY	Not selected	H	X	X	V_{PPLO}	High-Z
	Output Disable	L	H	H	V_{PPLO}	High-Z
	Read	L	H	L	V_{PPLO}	DOUT
READ/WRITE	Not Selected	H	X	X	V_{PPHI}	High-Z
	Output Disable	L	H	H	V_{PPHI}	High-Z
	Read	L	H	L	V_{PPHI}	DOUT
	Write	L	L	H	V_{PPHI}	DIN

X = Don't Care, L = LOW, H = HIGH

V_{PPHI} = 12.0V ± 0.6V, V_{PPLO} = 0V to V_{DD} +2.0V

COMMAND DEFINITION TABLE

Command	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
		Operation	Address	Data	Operation	Address	Data
Read Memory	1	Write	X	00H	-	-	-
Setup Erase/Erase	2	Write	X	20H	Write	X	20H
Erase Verify	2	Write	EA	A0H	Read	X	EVD
Setup Program/Program	2	Write	X	40H	Write	PA	PD
Program Verify	2	Write	X	C0H	Read	X	PVD
Reset	2	Write	X	FFH	Write	X	FFH

EA = Address to VerifyPA = Address to Program

EVD = Data Read from Location EAPD = Data to be Programmed at Location PA

PVD = Data to be Read from Location PA at Program Verify

ABSOLUTE MAXIMUM RATINGS [1]			
Symbol	**Parameter**	**Value**	**Units**
T_{STC}	Storage Temperature	-65 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
$V_{I/O}$	Voltage on Any Pin	-2.0 to +7.0 [2]	V
V_{PP}	V_{PP} Supply Voltage During Erase/Program	-2.0 to +14.0 [3]	V
V_{DD}	V_{DD} Supply Voltage	-2.0 to +7.0 [2]	V
I_{OUT}	Output Current	200 [4]	mA

RECOMMENDED OPERATING CONDITIONS [5]					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Units**
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IL}	Input Low Voltage	-0.5		0.8	V
V_{IH}	Input High Voltage	2.2		V_{DD}+0.5	V
T_A	Operating Temperature	0	25	70	°C

CAPACITANCE [6]: t_A = 25°C, f = 1MHz				
Symbol	**Parameter**	**Max**	**Unit**	**Condition**
C_{ADR}	Address Input	50	pF	V_{IN} = 0V
C_{CE}	Chip Enable	20		
C_{WE}	Write Enable	50		
C_{OE}	Output Enable	50		
$C_{I/O}$	Data Input/Output	25		

DC OPERATING CHARACTERISTICS									
Symbol	**Characteristic**	**Conditions**	**x8**		**x16**		**x32**		**Units**
			Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
I_{IL}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-4	+4	-4	+4	-4	+4	µA
I_{OL}	Output Leakage Current	V_{OUT} = V_{DD} or V_{SS}	-4	+4	-2	+2	-1	+1	µA
I_{CC1}	V_{DD} Active Read Current	$\overline{CE}$ = V_{IL}, f = 6MHz, I_{OUT} = 0mA		30		60		120	mA
I_{CC2}	V_{DD} Programming Current	Programming in Progress		30		60		120	mA
I_{CC3}	V_{DD} Erase Current	Erasure in Progress		30		60		120	mA
I_{SB1}	V_{DD} Supply Standby Current (CMOS)	$\overline{CE}$ = V_{DD} -0.2V, $V_{IN} \geq V_{DD}$ -0.2V or $V_{IN} \leq$ 0.2V		400		400		400	µA
I_{SB2}	V_{DD} Supply Standby Current (TTL)	$\overline{CE}$ = V_{IH}, V_{IN} = V_{IH} or V_{IN} = V_{IL}		4		4		4	mA
I_{PPS}	V_{PP} Leakage Current	V_{PP} = V_{PPLO}		4		4		4	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPHI}		200		200		200	µA
		V_{PP} = V_{PPLO}		4		4		4	
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPHI}, Programming in Progress		30		60		120	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPHI}, Erasure in Progress		30		60		120	mA
V_{IL}	Input Low Voltage		-0.5	0.8	-0.5	0.8	-0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{DD}+0.5	2.0	V_{DD}+0.5	2.0	V_{DD}+0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45		0.45		0.45	V
V_{OH}	Output High Voltage	I_{OH} = -2.5mA	2.4		2.4		2.4		V
V_{PPLO}	V_{PP} during Read-Only Operations		0	V_{DD}+2.0	0	V_{DD}+2.0	0	V_{DD}+2.0	V
V_{PPHI}	V_{PP} during Read/Write Operations		11.40	12.60	11.40	12.60	11.40	12.60	V

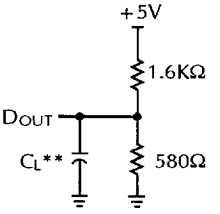
AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns *
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V

* Transition measured between 0.8V and 2.2V.

OUTPUT LOAD		
Load	**C_L**	**Parameters Measured**
1	100 pF	except t_{CLZ}, t_{OLZ}, t_{DF}
2	5 pF	t_{CLZ}, t_{OLZ}, t_{DF}

Figure 1. Output Load

** Including Probe and Jig Capacitance.

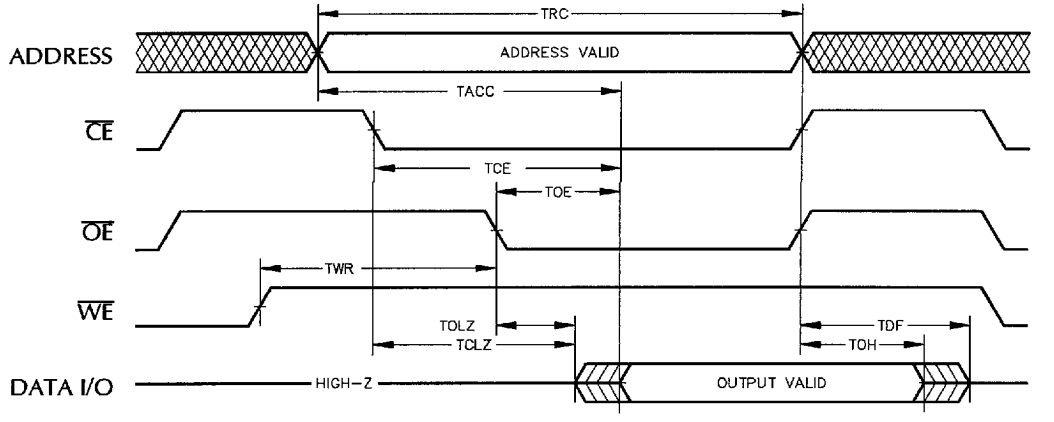


A.C. OPERATING AND CHARACTERISTICS - READ CYCLE: Over operating ranges											
No.	**Symbol**	**Parameter**	**90ns †**		**120ns**		**150ns**		**200ns**		**Unit**
			Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
1	t_{RC}	Read Cycle Time	90		120		150		200		ns
2	t_{CE}	Chip Enable Access Time		90		120		150		200	ns
3	t_{ACC}	Address Access Time		90		120		150		200	ns
4	t_{OE}	Output Enable Access Time		40		50		55		55	ns
5	t_{CLZ}	Chip Enable to Output in LOW-Z [6,7]	0		0		0		0		ns
6	t_{OLZ}	Output Enable to Output in LOW-Z [6,7]	0		0		0		0		ns
7	t_{DF}	Output Disable to Output in HIGH-Z [6,7]		25		30		35		35	ns
8	t_{OH}	Output Hold from Address, $\overline{CE}$, or $\overline{OE}$ Change	0		0		0		0		ns
9	t_{WR}	Write Recovery Time before Read	6		6		6		6		µs

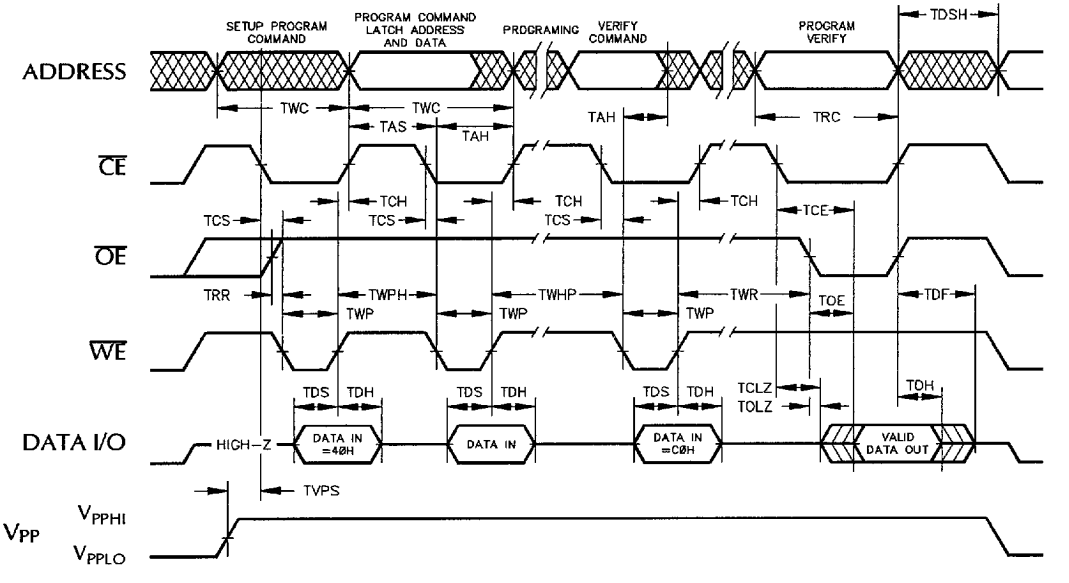
A.C. OPERATING AND CHARACTERISTICS - WRITE/ERASE OPERATIING CYCLE: Over operating ranges [8]											
No.	**Symbol**	**Parameter**	**90ns †**		**120ns**		**150ns**		**200ns**		**Unit**
			Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
10	t_{WC}	Write Cycle Time	90		120		150		200		ns
11	t_{AS}	Address Setup Time	0		0		0		0		ns
12	t_{AH}	Address Hold Time	45		50		60		75		ns
13	t_{DS}	Data Setup Time	45		50		50		50		ns
14	t_{DH}	Data Hold Time	10		10		10		10		ns
15	t_{WR}	Write Recovery Time before Read	6		6		6		6		µs
16	t_{RR}	Read Recover Time before Write	0		0		0		0		µs
17	t_{CS}	Chip Enable Setup Time before Write	20		20		20		20		ns
18	t_{CH}	Chip Enable Hold Time	0		0		0		0		ns
19	t_{WP}	Write Pulse Width	45		50		50		50		ns
20	t_{WPH}	Write Pulse Width HIGH	20		20		20		20		ns
21	t_{WHP}	Duration of Programming Operation	10	25	10	25	10	25	10	25	µs
22	t_{WHE}	Duration of Erase Operation	9.5	10.5	9.5	10.5	9.5	10.5	9.5	10.5	ms
23	t_{PS}	V_{PP} setup Time to Chip Enable LOW	100		100		100		100		ns
24	t_{VCS}	V_{DD} Setup Time	2		2		2		2		µs
25	t_{VPPR}	VPP Rise Time	500		500		500		500		ns
26	t_{VPPF}	VPP Fall Time	500		500		500		500		ns

† Commercial only.

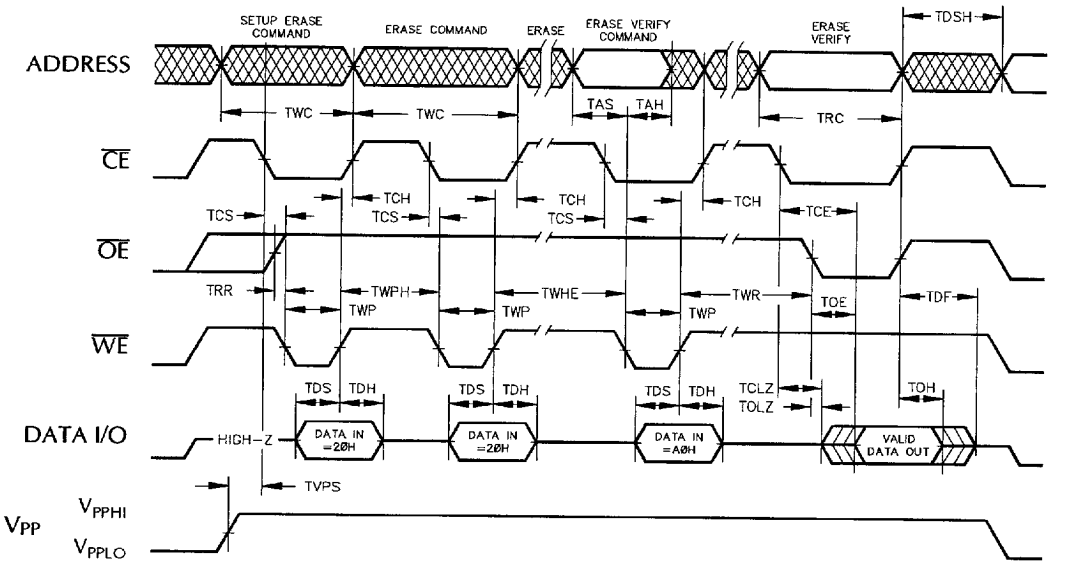
READ CYCLE



WRITE CYCLE



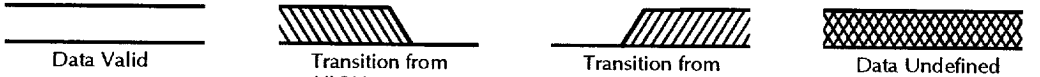
ERASE CYCLE



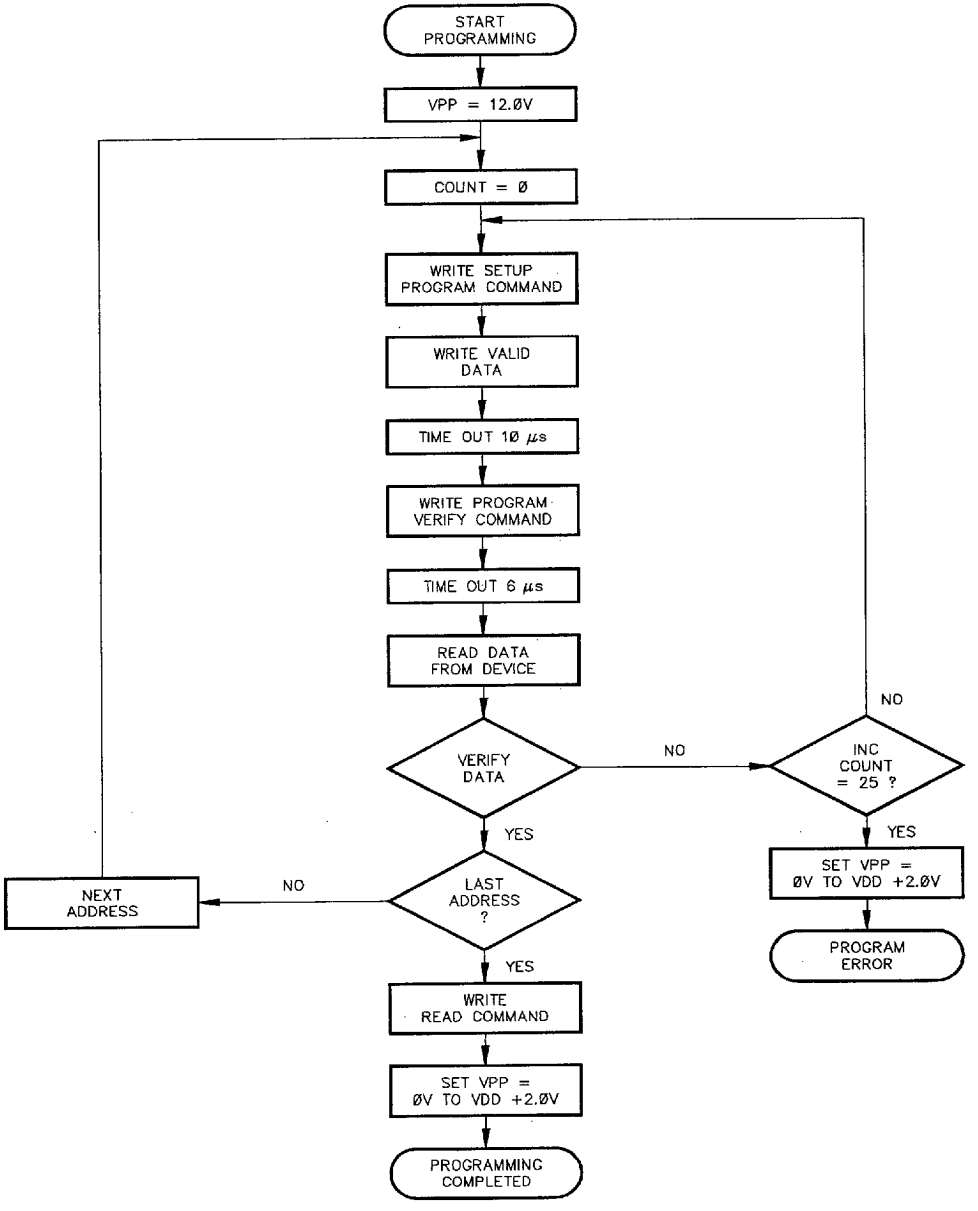
NOTES:

1. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposures to absolute maximum rating conditions for extended periods may affect reliability.
2. -2.0 minimum for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Maximum D.C. voltage on V_{PP} may overshoot to +14.0V for periods less than 20ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.
5. All voltages are with respect to V_{SS}.
6. This parameter is guaranteed and not 100% tested.
7. Transition is measured at the point of ±500mV from steady state voltage.
8. Read timing characteristics during read/write operations are the same as during read-only operations. See A.C. Characteristics for Read-Only Operations.

WAVEFORM KEY



WRITE ALGORITHM



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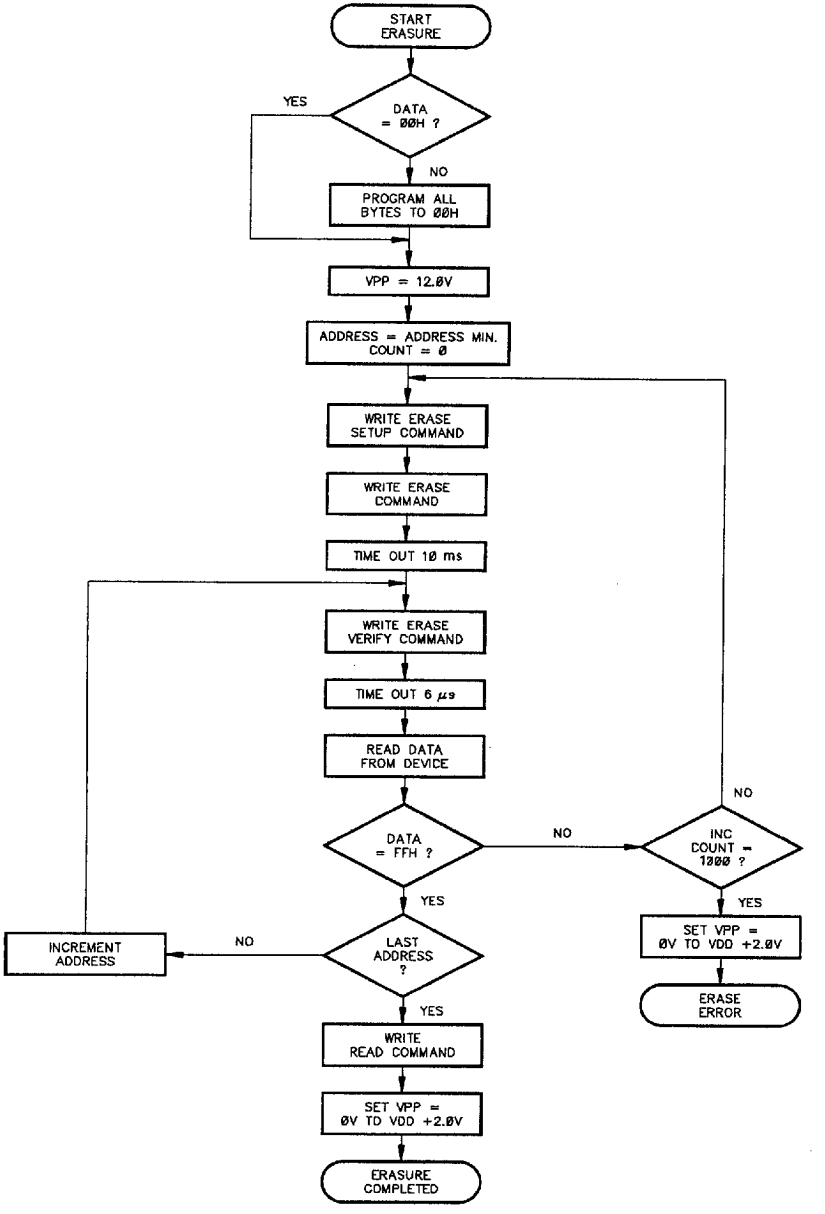
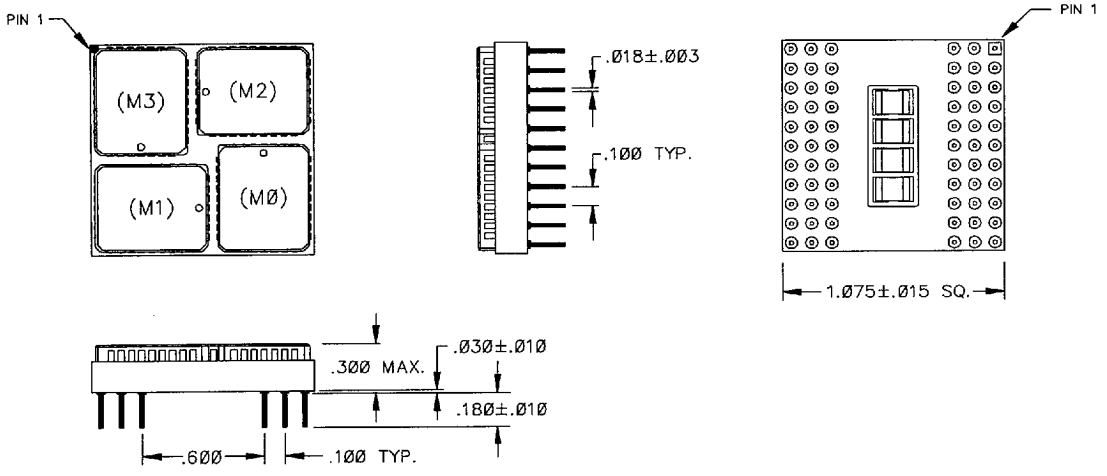
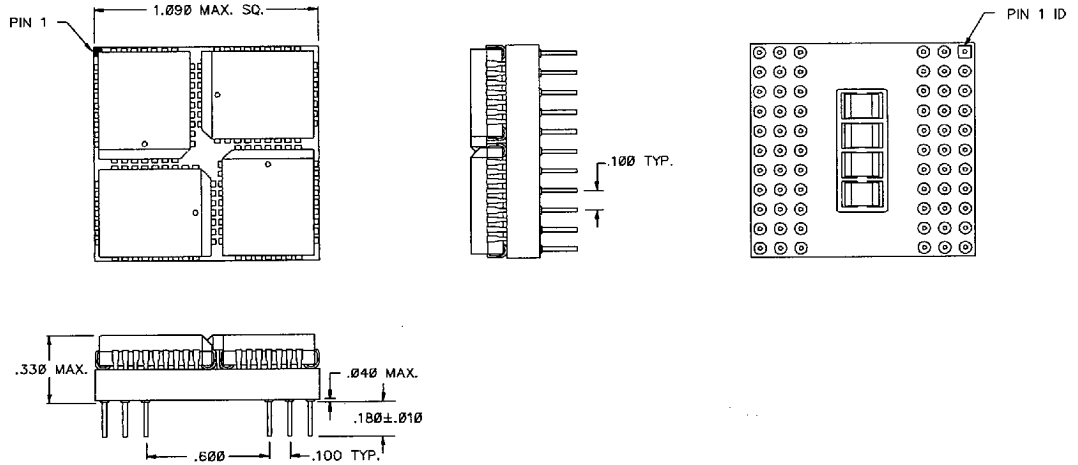
ERASE ALGORITHM



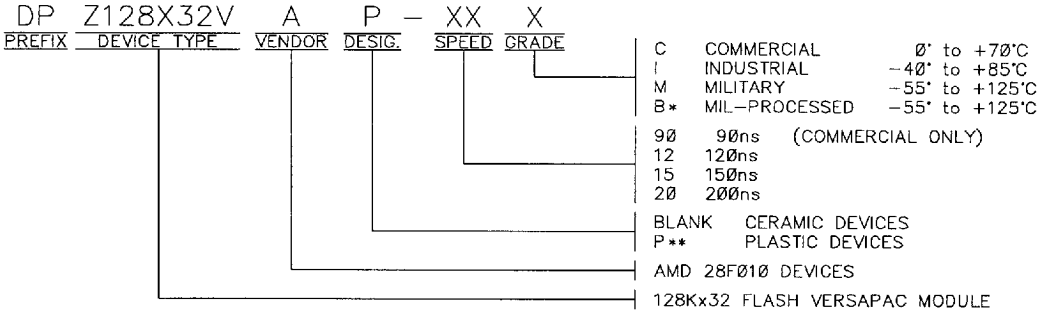
DPZ128X32VA - MECHANICAL DRAWING



DPZ128X32VAP- MECHANICAL DRAWING



ORDERING INFORMATION



* Built with 883 devices.
** Commercial and Industrial grade only.

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