National Semiconductor Corporation

PRELIMINARY

DS8911/DS8912 AM/FM/TV Sound Up-Conversion Frequency Synthesizers

General Description

The DS8911 and DS8912 are digital Phase-Locked Loop (PLL) frequency synthesizers intended for use as Local Oscillators (LO) in electronically tuned radios. The devices are used in conjunction with a serial data controller, a loop filter, some varactor diodes and several passive elements to provide the local oscillator function for both AM and FM tuning.

The conventional superheterodyne AM receiver utilizes a low IF or down conversion tuning approach whereby the IF is chosen to be below the frequencies to be received. The DS8911 and DS8912 PLL's on the other hand, utilize an up-conversion technique in the AM mode whereby the first IF frequency is chosen to be well above the RF frequency range to be tuned. This approach eliminates the need for tuned circuits in the AM frontend since the image, half IF, and other spurious responses occur far beyond the range of frequencies to be tuned. Sufficient selectivity and second IF image protection is provided by a crystal filter at the output of the first mixer.

A significant cost savings can be realized utilizing this up-conversion approach to tuning. Removal of the AM tuned circuits eliminates the cost of expensive matched varactor diodes and reduces the amount of labor required for alignment down from 6 adjustments to 2. Additional cost savings are realized because up-conversion enables both the AM and FM bands to be tuned using a single Voltage Controlled Oscillator (VCO) operating between 98 and 120 MHz. (The 2 to 1 LO tuning range found in conventional AM down conversion radios is reduced to a 10% tuning range; 9.94 MHz to 11.02 MHz).

Up-conversion AM tuning is accomplished by first dividing the VCO signal down by a modulus 10 (DS8911) or 20 (DS8912) to obtain the LO signal. This LO in turn is mixed on chip with the RF signal to obtain a first IF at the MIXER output pins. This first IF after crystal filtering is mixed (externally) with a reference frequency provided by the PLL to obtain a 450 kHz second IF frequency. The DS8911 derives the 450 kHz second IF by mixing an 11.55 MHz first IF with a 12.00 MHz reference frequency. The DS8912 derives the 450 kHz second IF by mixing a 4.45 MHz first IF with a 4.00 MHz reference frequency.

FM and WB (weather band) tuning is done using the conventional down conversion approach. Here the VCO signal is buffered to produce the LO signal and then mixed on chip with the RF signal to obtain an IF frequency at the MIXER output pins. This IF frequency is typically chosen to be 10.7 MHz although placement at 11.50 MHz can further enhance AM mode performance and minimize IF circuitry.

The DS8911 was designed to utilize an 11.55 MHz crystal filter because of its superior phase noise and temperature drift characteristics. The DS8912 on the other hand was designed to utilize a 4.45 MHz ceramic filter for cost savings in applications not requiring high performance.

Both PLLs provide phase comparator reference frequencies of 10, 12.5, 25, and 100 kHz. The tuning resolutions resulting from these reference frequencies are determined by dividing the reference by the premix modulus. Table II shows the tuning resolutions possible.

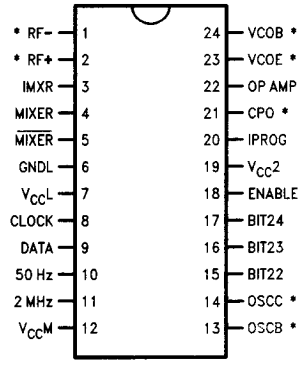
The DS8911 and DS8912 contain the following logic elements: a voltage controlled oscillator, a reference oscillator, a 14-bit programmable dual-modulus counter, a reference frequency divider chain, a premix divider, a mixer, a phase comparator, a charge pump, an operational amplifier, and control circuitry for latched serial data entry.

Features

- Direct synthesis of LW, MW, SW, FM, and WB frequencies
- Serial data entry for simplified processor control
- 10, 12.5, 25, and 100 kHz reference frequencies
- 8 possible tuning resolutions (see Table II)
- An op amp with high impedance inputs for loop filtering
- Programmable mixer with high dynamic range
- Fast-lock feature for Automatic Road Information (ARI) systems

Connection Diagrams

SO and Dual-In-Line Packages



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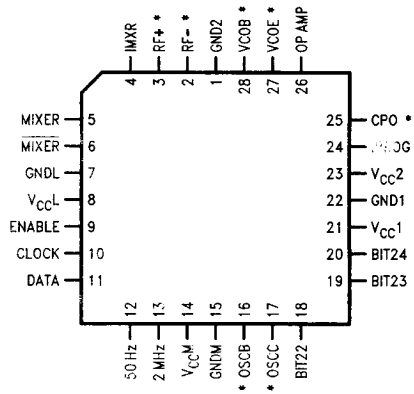
Top View

Plastic Chip Carrier



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Top View

Order Number DS8911M, DS8911N, DS8911V, DS8912M, DS8912N or DS8912V
See NS Package Number M24B, N24C or V28A

Note: Device pins marked with an asterisk (*) are not guaranteed to meet the NSC standard requirement for Electrostatic Discharge (ESD) protection of 2000 volts. The functional requirements of the application prohibit the additional resistive or capacitive components required for ESD protection on these pins.

Pin Descriptions

V_{CC1}: The V_{CC1} pin provides a 5V supply source for all circuitry except the reference divider chain, op amp and mixer sections of the die.

V_{CC2}: The V_{CC2} pin provides a 12V supply source for the Op amp.

V_{CCL}: The V_{CCL} pin provides an isolated 5V supply source for the premix divider and mixer functions.

V_{CCM}: The V_{CCM} pin provides a 5V supply source for the reference oscillator and divider chain down through the 50 Hz output, thus enabling low standby current for time-of-day clock applications.

GND1, GND2, GNDL and GNDM: Provide isolated circuit ground for the various sections of the device.

DATA and CLOCK: The DATA and CLOCK inputs are for serial data entry from a controller. They are CMOS inputs with TTL logic thresholds. The 24-bit data stream is loaded into the PLL on the positive transition of the CLOCK. The first 14 bits of the data stream select PLL divide code in binary form MSB first. The 15th through 24th bits select the premix modulus, the reference frequency, the loop response mode, the bit output status, and the test/operate modes as shown in Tables I through V.

ENABLE: The ENABLE input is a CMOS input with a TTL logic threshold. The ENABLE input enables data when at a logic "one" and latches data on the transition to a logic "zero".

BIT Outputs: The open-collector BIT outputs provide either the status of shift register bits 22, 23, and 24 or enable access to key internal circuit test nodes. The mode for the bit outputs is controlled by shift register bits 20 and 21. In operation, the bit outputs are intended to drive radio functions such as gain, mute, and AM/FM status. These outputs can also be used to program the loop gain by connection of an external resistor to IPROG. Bit 24 output can also be used as a 300 millisecond timer under control of shift register bit 19. During service testing, these pins can be used for the purpose of either monitoring or driving internal logic points as indicated in the TEST MODES description under Table V.

VCOb and VCOe: The Voltage Controlled Oscillator inputs drive the 14-bit programmable counter and the premix divider. These inputs are the base and emitter leads of a transistor which require connection of a coil, varactor, and several capacitors to function as a Colpitts oscillator. The VCO is designed to operate up to 225 MHz. The VCO's minimum operating frequency may be limited by the choice of reference frequency and the 961 minimum modulus constraint of the 31/32 dual modulus counter.

RF+ and RF−: The Radio Frequency inputs are fed differentially into the mixer.

IMXR: The bias current for the mixer is programmed by connection of external resistors.

MIXER and $\overline{\text{MIXER}}$: The MIXER outputs are the collectors of the double balanced pair mixer transistors. They are intended to operate at voltages greater than V_{CC1}.

OSCb and OSCc: The Reference Oscillator inputs are part of an on-chip Pierce oscillator designed to work in conjunction with 2 capacitors and a crystal resonator. The DS8911 requires a 12 MHz crystal, while the DS8912 requires a 4 MHz crystal.

The OSC input signal is mixed externally with the 1st AM IF output to obtain a 450 kHz 2nd IF frequency in the AM mode.

2 MHz: The 2 MHz output is provided to drive a controller's clock input.

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Pin Descriptions (Continued)

50 Hz: The 50 Hz output is provided as a time reference for radios with time-of-day clocks.

IPROG: The IPROG pin enables the charge pump to be programmed from .5 mA to 1.5 mA by connection of an extenal resistor to ground.

CPO: The Charge Pump Output circuit sources current if the VCO frequency is high and sinks current if the VCO frequency is low. The CPO is wired directly to the negative input of the loop filter op amp.

OP AMP: The OP AMP output is provided for loop filtering. The op amp has high impedance PMOS gate inputs and is wired as a transconductance amplifier/filter. The op amp's positive input is internally referenced while it's negative input is common with the CPO output.

Reference Tables DS8911 (DS8912)

TABLE I

Bit 15	Premix Modulus
0	÷ 1
1	÷ 10 (÷ 20)

TABLE II

Bit		Reference Frequency	Tuning Resolution	
16	17		÷ 1 Premix	÷ 10 (÷ 20) Premix
0	0	10 kHz	10 kHz	1 (.5) kHz
0	1	12.5 kHz	12.5 kHz	1.25 (.625) kHz
1	0	25 kHz	25 kHz	2.5 (1.25) kHz
1	1	100 kHz	100 kHz	10 (5) kHz

TABLE III

Bit 18	Loop Response
0	Normal Lock
1	Fast Lock

FAST LOCK OPERATION

The fast lock mode provides a means of moving from one frequency selection to another frequency selection anywhere on the band in a very short time frame. This is accomplished by setting a bit in the microprocessor serial data stream when loading a new frequency. When fast lock is activated the charge pump output (CPO) is latched into the pump up or down state, which drives the CPO at the maximum rate to correct the VCO frequency. The PLL meanwhile operates in a frequency lock mode, constantly comparing the frequencies and reducing any phase discrepancies. When the VCO passes beyond the desired lock frequency the CPO unlatches and reverts back to the phase lock mode of operation. The frequency lock mode of operation (during CPO latchup) ensures that the phases are always close and will quickly settle into phase lock once the CPO unlatches.

TABLE IV

Bit 19	Timer
0	Bit 24 Status
1	$\overline{\text{Bit 24}}$ for 300 ms

TIMER OPERATION

The timer function is provided for use as a retriggerable "one shot" to enable muting for approximately 300 milliseconds after station changes. The timer is enabled at bit 24's output if the normal operating mode is selected (shift register bits 20 and 21 = "LOW") and shift register bit 19 data is latched as a "HI". The timer's output state will invert immediately upon latching bit 19 "HI" and remain inverted for approximately 300 milliseconds. If the user readdresses the device with bit 19 data "LOW" before the timer finishes its cycle the timer's BIT 24 output will finish out the 300 ms pulse. Readdressing the device with bit 19 "HI" before the timer finishes its cycle will extend the BIT 24 output pulse width by 300 ms. Addressing should be performed immediately after the 50 Hz output transitions "HI". BIT 24's output state is not guaranteed during the first 300 ms after V_{CC_1} power up as a result of a timer reset in progress.

TABLE V

Bit		FUNCTION OF PINS 3, 4, & 5
20	21	
0	0	Status of Bits 22-24
0	1	Test mode 1
1	0	Test mode 2
1	1	Test mode 3

TEST MODE OPERATION

Test Mode 1: Enables the BIT output pins to edge trigger the phase comparator inputs and monitor an internal lock detector. BIT 22 negative edge triggers the reference divider input of the phase comparator if the reference divider state is low. BIT 23 provides the open collector ORing of the phase comparator's pump up and down outputs. BIT 24 negative edge triggers the N counter input of the phase comparator if the N counter state is preconditioned low.

Test Mode 2: Enables the BIT outputs to clock the programmable N counter, monitor its output, and force either its load or count condition. BIT 22 provides the N counter output which negative edge triggers the phase comparator and which appears low one N counter clock pulse before it reloads. BIT 23 positive edge triggers the N counter's clock input if the prescaler's output is preconditioned HI. BIT 24 clears the N counter output so that loading will occur on the next N counter clock edge.

Test Mode 3: Enables the BIT outputs to clock the 50 Hz and 10 kHz reference dividers, monitor the reference divider input to the phase comparator, and reset the fast lock latch. BIT 22 positive edge clocks the 10 kHz reference divider chain if the 10 kHz output is preconditioned HI. BIT 22 also positive edge clears the fast lock latch condition. Bit 23 positive edge clocks the 50 Hz divider chain. BIT 24 is the reference divider negative edge trigger input to the phase comparator.

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage
- V_{CCM} 7V
- V_{CC1} 7V
- V_{CC2} 15V

Input Voltage 7V

Output Voltage
- Logic 7V
- Op Amp and Mixer Outputs 15V

Storage Temperature Range −65°C to +150°C

Lead Temp. (Soldering, 10 seconds) 300°C

Operating Conditions

	Min	Max	Units
V_{CCM}	3.5	5.5	V
V_{CC1}	4.5	5.5	V
V_{CC2}	7.0	12.0	V
Temperature, T_A	−40	+85	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter		Test Conditions		Min	Typ	Max	Units
V_{IH}	Logic "1" Input Voltage				2.0			V
V_{IL}	Logic "0" Input Voltage						0.8	V
I_{IH}	Logic "1" Input Current		V_{IN} = 5.5V				10	μA
I_{IL}	Logic "0" Input Current		Data, Clock and Enable Inputs, V_{IN} = 0V				−10	μA
V_{OH}	Logic "1" Output Voltage	2 MHz	I_{OH} = −20 μA		V_{CCM} − 0.3			V
			I_{OH} = −400 μA		V_{CCM} − 2			V
		Op Amp	I_{OH} = −1.5 mA		V_{CC_2} − 1.5			V
V_{OL}	Logic "0" Output Voltage	2 MHz	I_{OL} = 20 μA				0.3	V
			I_{OL} = 400 μA				0.4	V
		50 Hz	I_{OL} = 250 μA				0.3	V
		Bit Outputs	I_{OL} = 1 mA				0.3	V
		Op Amp	I_{OL} = 1.5 mA				1.5	V
V_{BIAS}	Op Amp Input VΔ		Op Amp I/O Shorted, V_{CC1} = 5.5V, V_{CC2} = 12V, CPO = TRI-STATE®, Op Amp I_{OH} vs. I_{OL} Applied				150	mV
I_{CEX}	High Level Output Current	Bit Outputs	V_{CC_1} = 4.5V, V_O = 8.8V				100	μA
		50 Hz	V_{CC_M} = 3.5V, V_O = 5.5V				10	μA
		Mixers	V_{CC_L} = V_{CC_1} = 4.5V, V_O = 8.8V				100	μA
I_{CPO}	Charge Pump Program Current		0.5 mA < I_{CPO} < 1.5 mA 2 I_{PROG} = V_{CC_1}/R_{PROG}, Measured I_{PROG} to CPO	Pump-up	−20	2 I_{PROG}	+20	%
				Pump-down	−20	2 I_{PROG}	+20	%
				TRI-STATE		0	100	nA
I_{CCM}	V_{CCM} Supply Current		V_{CCM} = 5.5V			0.5	1.0	mA
I_{CC1} + I_{CCL}	V_{CC1} + V_{CCL} Supply Current		V_{CC} = 5.5V, Bits Hi, I_{MXR} and I_{PROG} Open			25	35	mA
I_{CC2}	V_{CC2} Supply Current		V_{CC2} = 12V			1.5	2.5	mA
R_{IN}	Mixer Input Impedance		I_{MXR} = 2.5 mA I_{MXR} = 7.5 mA			TBD TBD		Ω Ω
R_{OUT}	Mixer Output Impedance		I_{MXR} = 2.5 mA I_{MXR} = 7.5 mA			TBD TBD		Ω Ω
g_m	Mixer Transconductance		I_{MXR} = 2.5 mA I_{MXR} = 7.5 mA			TBD TBD		mhos mhos
NF	Noise Figure		I_{MXR} = 2.5 mA, R_S = 50Ω I_{MXR} = 7.5 mA, R_S = 10Ω			TBD TBD		dB dB
XMOD	Cross Modulation		I_{MXR} = 2.5 mA I_{MXR} = 7.5 mA			TBD TBD		mVRms mVRms
I_{MXR}	Mixer Current		V_{CC1} = 5.5V		1		7.5	mA
VCO_{MAX}	VCO_{MAX} frequency						225	MHz

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the device should be operated at these limits.

Note 2: Unless otherwise specified, min/max limits apply across the −40°C to +85°C temperature range for DS8911 and DS8912.

Note 3: All currents into device pins are shown as positive, out of device pins as negative, all voltage referenced to ground unless otherwise noted. All values shown as maximum or minimum on absolute value basis.

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AC Electrical Characteristics (Note 2)

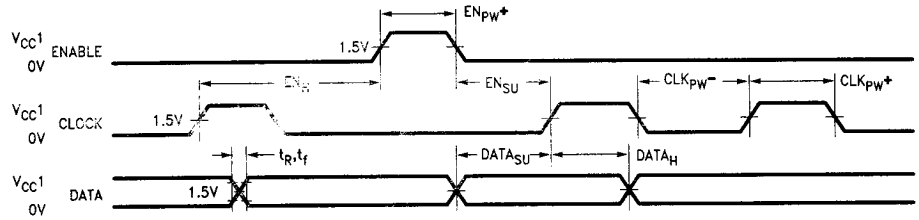
Symbol	Parameter	Conditions	Min	Max	Units
t_r	20%–80% Rise Time	V_{CC_1} = 4.5V to 5.5V		200	ns
t_f	80%–20% Fall Time			200	ns
$DATA_{SU}$	Data Setup Time		100		ns
$DATA_H$	Data Hold Time		100		ns
EN_{SU}	Enable Setup Time		100		ns
EN_H	Enable Hold Time		100		ns
EN_{PW+}	Enable Positive Pulse Width		200		ns
CLK_{PW+}	Clock Positive Pulse Width		200		ns
CLK_{PW-}	Clock Negative Pulse Width		200		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the device should be operated at these limits.

Note 2: Unless otherwise specified, min/max limits apply across the −40°C to +85°C temperature range for DS8911 and DS8912.

Note 3: All currents into device pins are shown as positive, out of device pins as negative, all voltage referenced to ground unless otherwise noted. All values shown as maximum or minimum on absolute value basis.

Timing Diagram



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MICROWIRE™ Bus Format

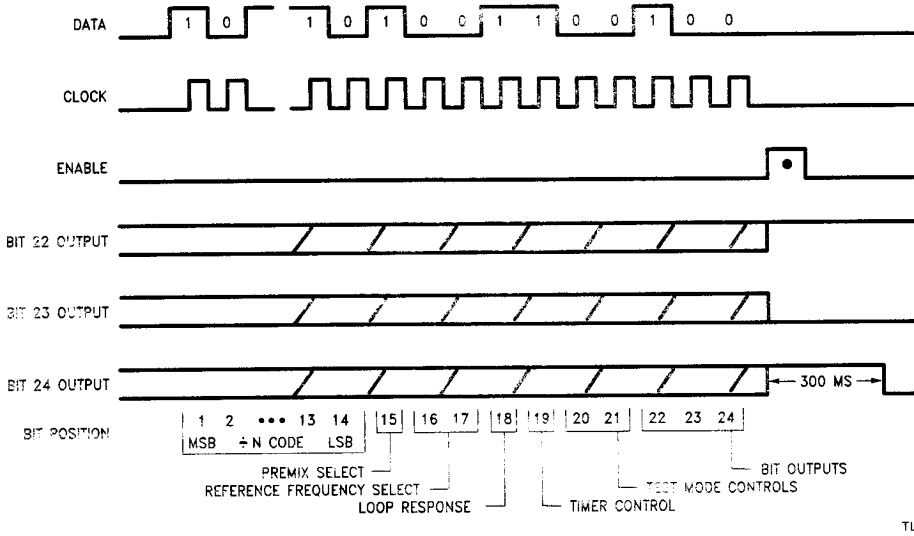

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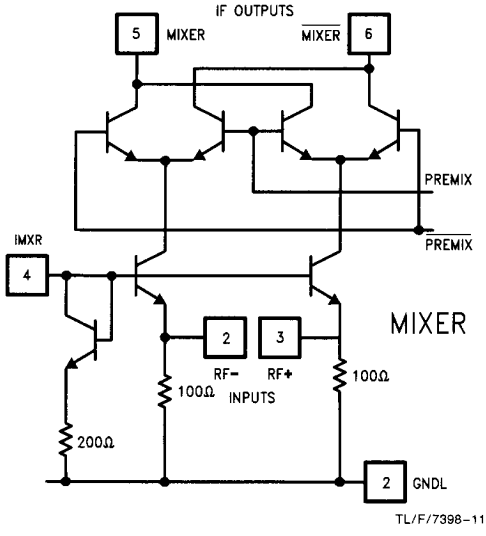
TABLE VI. DS8911 Tuning Characteristics

Mode	IF Frequency (MHz)	Tuning Range (MHz)	VCO Range (MHz)	Premix Modulus	Reference Frequency (kHz)	Tuning Resolution (kHz)	Image (MHz)
LW	11.55/.450	.145–.290	112.4–114.1	10	10	1	22–23
MW	11.55/.450	.515–1.61	99.4–110.2	10	10, 12.5, 25, 100	1, 1.25, 2.5, 10	21–23
SW	11.55/.450	5.94–6.2	53.5 to 56.1	10	10, 12.5, 25	1, 1.25, 2.5	28–30
FM	10.7	87.4–108.1	98.1–118.8	1	10, 12.5, 25, 100	10, 12.5, 25, 100	109–130
WB	10.7	162.4–162.6	151–152	1	12.5, 25	12.5, 25	140–142
TV_1	10.7	59.75–87.75	70.45–98.45	1	25	25	81–109
TV_2	10.7	179.75–215.75	169.1–205.1	1	25	25	158–194

TABLE VII. DS8912 Tuning Characteristics

Mode	IF Frequency (MHz)	Tuning Range (MHz)	VCO Range (MHz)	Premix Modulus	Reference Frequency (kHz)	Tuning Resolution (kHz)	Image (MHz)
LW	4.45/.450	.145–.290	91.9–94.8	20	10	.5	13–14
MW	4.45/.450	.515–1.61	99.6–121.2	20	10, 12.5, 25, 100	.5, .625, 1.25, 5	14–17
SW	4.45/.450	5.94–6.2	207.9–213.1	20	25, 100	1.25, 5	14–16
FM	10.7	87.4–108.1	98.1–118.8	1	10, 12.5, 25, 100	10, 12.5, 25, 100	109–130
WB	10.7	162.4–162.6	151–152	1	12.5, 25	12.5, 25	140–142

Input and Output Schematics



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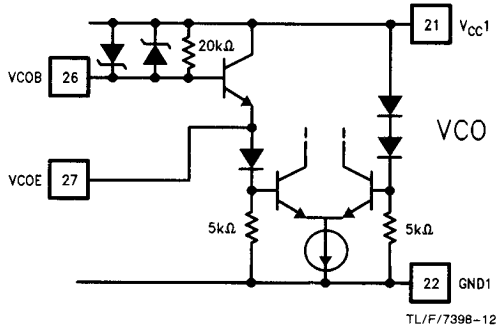

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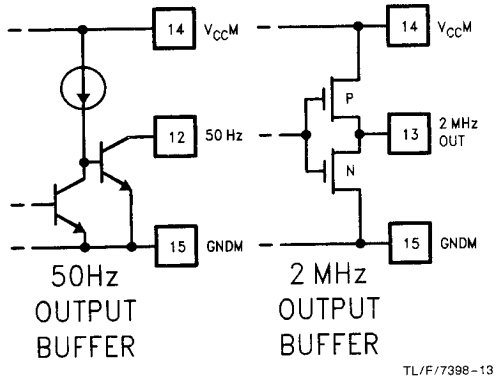
Input and Output Schematics (Continued)



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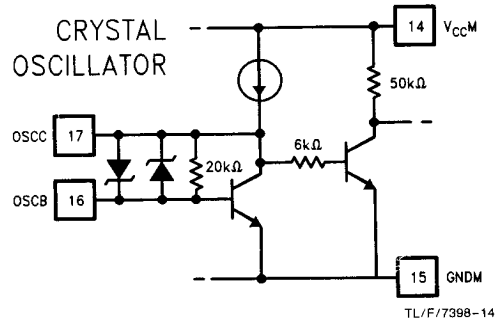

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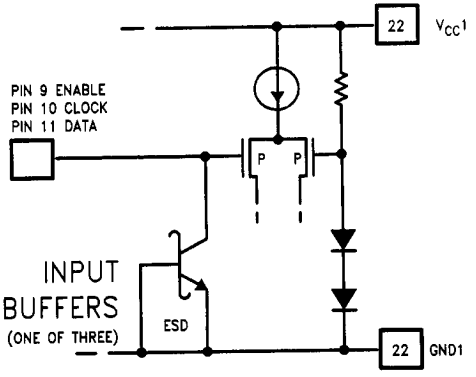

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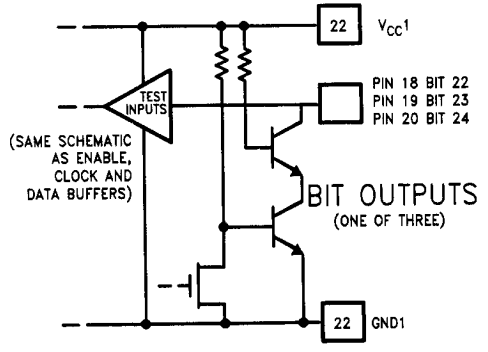

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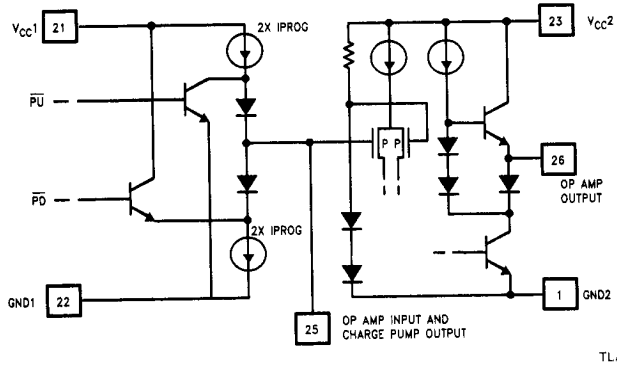

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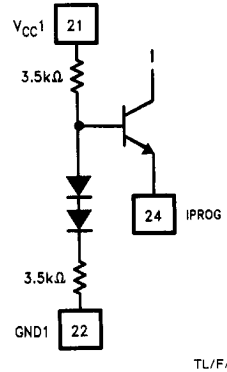

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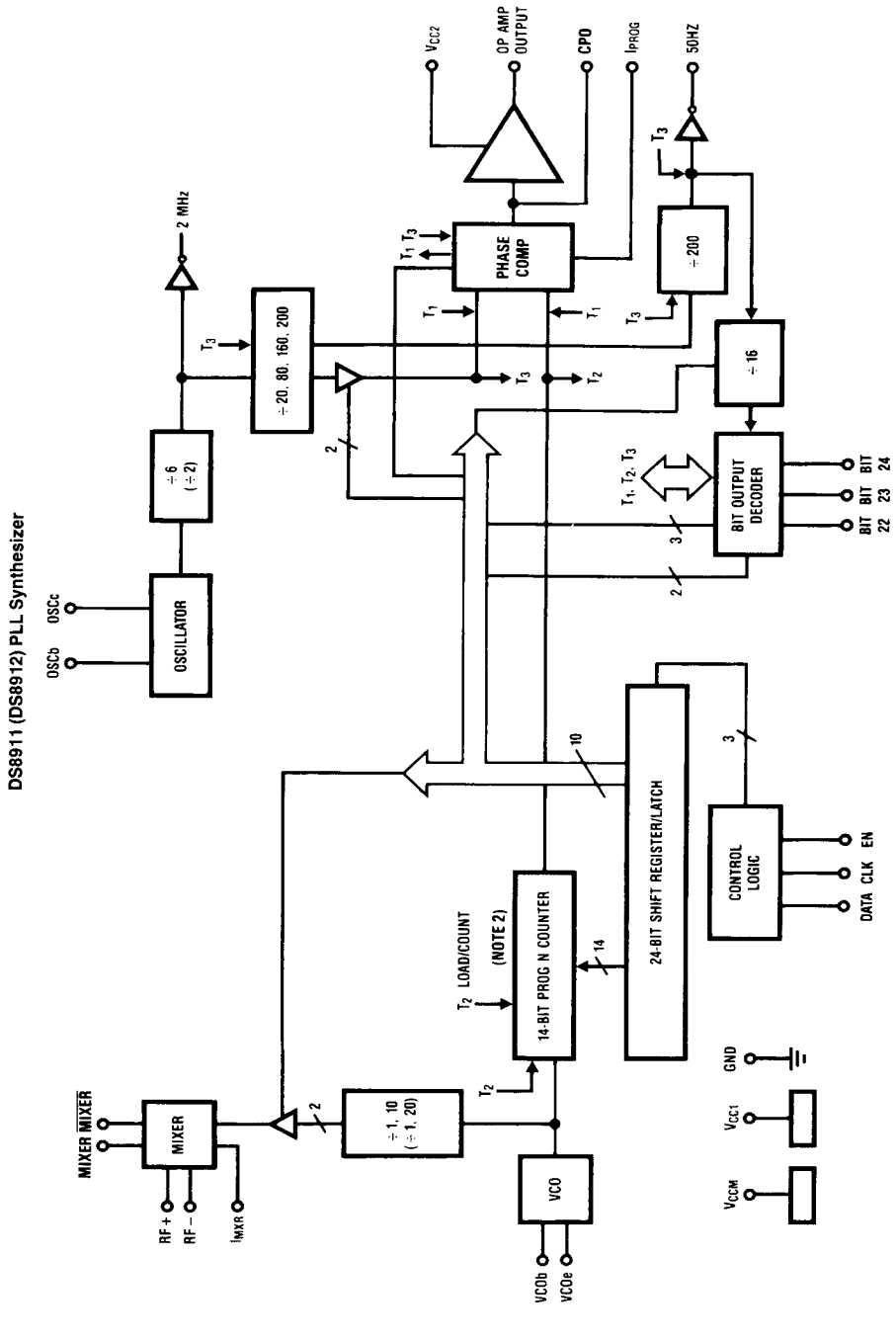
Logic Diagram



Note 1: Logic labels (in parentheses) pertain to the DS8912 option.

Note 2: The 14 bit programmable N counter is a dual modulus counter with 31/32 prescaler. The minimum continuous modulus of the N counter is 961. (There are a limited number of valid modulus codes below 961.)

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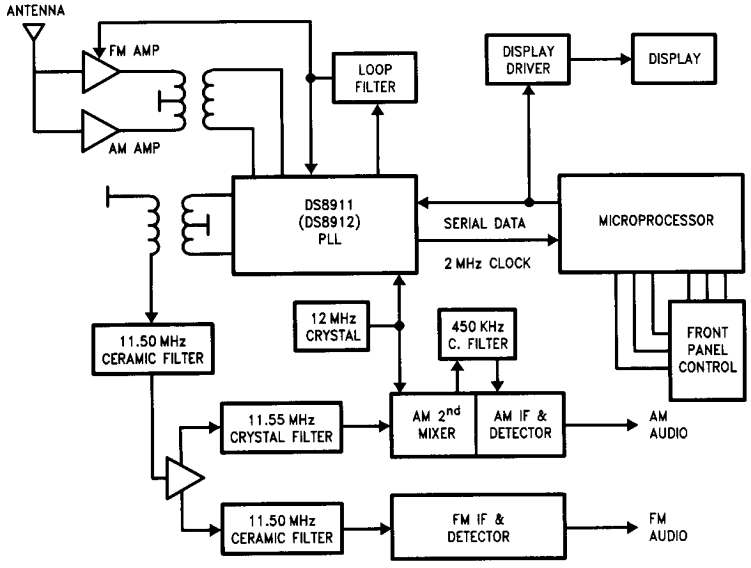
Typical Application

AM/FM ETR Radio Application



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