HD66840F

LCD Video Interface Controller (LVIC)

For Maintenance Only

For new designs please see data sheet for HD66841F

Description

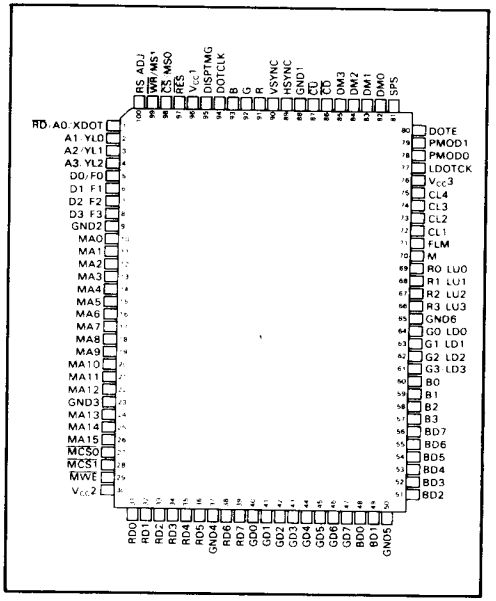
The HD66840F LVIC interface controller converts the standard video signals R, G, B for CRT display into LCD data. It enables a CRT display system to be replaced by an LCD system without any changes. It also enables the software originally intended for CRT display to control the LCD.

Since the LVIC can control TFT-type LCDs in addition to the current TN-type LCD, it can support color display as well as monochrome display. It can program screen size and can control a large-panel LCD of 720 dots × 512 dots (max).

Features

- Converts video R, G, B signals for CRT display into LCD data:
  - —Monochrome display data
  - —8-level gray scale display data
  - —8-color display data
- Can select LVIC control method:
  - —Pin programming method
  - —Internal register programming method (either with MPU or ROM)
- Can program screen size:
  - —200, 350, 400, 480, 512, or 540 dots (lines) in height and 640, or 720 dots (80, or 90 characters) in width by pin programming method
  - —4-1024 dots (lines) in height and 32-4048 dots (4-506 characters) in width by internal register programming method
- Can regenerate the display timing signal from HSYNC and VSYNC
- Internal PLL circuit can generate the dot clock (external charge pump, low pass filter (LPF), and voltage-controlled oscillator (VCO) required)
- Can control both TN-type LCD and TFT-type LCD
- Maximum operating frequency: 25 MHz (dot clock for CRT display)
- LCD driver interface: 4-, 8-, or 12-bit (4 bits each for R, G, B) parallel data transfer
- Recommended LCD drivers: HD61104 (column) and HD61105 (common), HD66204 (column) and HD66205 (common), HD66106 and HD66107T (column/common)
- CMOS 1.3 μm process
- Single power supply: +5 V ± 10 %
- 100-pin plastic QFP (FP-100A)

Pin Arrangement



Ordering Information

Type No.	Dot clock (MHz)	Package
HD66840F	25 MHz	100-pin Plastic QFP (FP-100A)

Pin Description

Table 1 describes the pins.

Table 1 Pin Description

Symbol	Pin Number	Pin Name	I/O
$V_{CC}1$-$V_{CC}3$	96, 30, 76	$V_{CC}1$, V_{CC} 2, V_{CC} 3	—
GND1-GND6	88, 9, 23, 37, 50, 65	Ground 1-6	—
R, G, B[1]	91, 92, 93	Red, green, blue serial data	I
HSYNC	89	Horizontal synchronization	I
VSYNC	90	Vertical synchronization	I
DISPTMG[2]	95	Display timing	I
DOTCLK	94	Dot clock	I
R0-R3[3] LU0-LU3[4]	69-66 69-66	LCD red data 0-3 LCD up panel data 0-3	O O
G0-G3[3,5] LD0-LD3[4,5]	64-61 64-61	LCD green data 0-3 LCD down panel data 0-3	O O
B0-B3[3,6]	60-57	LCD blue data 0-3	O
CL1	72	LCD data line clock	O
CL2	73	LCD data shift clock	O
CL3[7]	74	Y-driver shift clock 1	O
CL4[7]	75	Y-driver shift clock 2	O
FLM	71	First line marker	O
M	70	LCD driving signal alternation	O
LDOTCK	77	LCD dot clock	I
$\overline{MCS0}$, $\overline{MCS1}$[8]	27, 28	Memory chip select 0, 1	O
$\overline{MWE}$[9]	29	Memory write enable	O
MA0-MA15[9]	10-22, 24-26	Memory address 0-15	O
RD0-RD7[9]	31-36, 38-39	Memory red data 0-7	I/O
GD0-GD7[9,10]	40-47	Memory green data 0-7	I/O
BD0-BD7[9,10]	48, 49 51-56	Memory blue data 0-7	I/O

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Table 1 Pin Description (cont)

Symbol	Pin Number	Pin Name	I/O
PMOD0, PMOD1	78, 79	Program mode 0, 1	I
DOTE	80	Dot clock edge change	I
SPS	81	Synchronization polarity select	I
DM0-DM3	82-85	Display mode 0-3	I
$\overline{CS}$ (MPU programming)[11]	98	Chip select	I
MS0 (pin programming)[11]	98	Memory select 0	I
$\overline{WR}$ (MPU programming)[11,12]	99	Write	I
MS1 (pin programming)[11]	99	Memory select 1	I
$\overline{RD}$ (MPU programming)[12]	1	Read	I
A0 (ROM programming)	1	Address 0	O
XDOT (pin programming)	1	X-dot	I
RS (MPU programming)[11]	100	Register select	I
ADJ (pin programming)[11]	100	Adjust	I
D0-D3 (MPU programming)	5-8	Data 0-3	I/O
D0-D3 (ROM programming)	5-8	Data 0-3	I
F0-F3 (pin programming)	5-8	Fine adjust 0-3	I
A1-A3 (ROM programming)[13]	2-4	Address 1-3	O
YL0-YL2 (pin programming)[13]	2-4	Y-line 0-2	I
$\overline{RES}$[14]	97	Reset	I
$\overline{CD}$	86	Charge down	O
$\overline{CU}$	87	Charge up	O

Notes: 1. When CRT display data is monochrome, G and B pins should be fixed low.
2. Fix high or low when regenerating the display timing signal internally.
3. For 8-color display modes.
4. For monochrome and 8-level gray scale display modes.
5. Leave disconnected in 4-bit/single screen data transfer modes.
6. Leave disconnected in monochrome and 8-level gray scale display modes.
7. Leave disconnected when controlling TN-type LCD.
8. Leave disconnected when using no buffer memories.
9. Leave disconnected when using no buffer memories.
10. In monochrome display modes, the LVIC writes the OR of R, G, B signals into R-plane RAMs. Thus, no RAMs are required for G and B planes in these modes.
Pull up these pins with 20-kΩ resistance. If G and B plane RAMs are connected in monochrome display modes, the LVIC writes G and B signals into each RAM. However, it does not affect the display or the contents of R-plane RAM whether G- and B-plane RAMs are connected or not.
11. Fix high or low when controlling the LVIC by ROM programming method.
12. $\overline{WR}$ and $\overline{RD}$ must not be low at the same time.
13. Fix high or low when controlling the LVIC by MPU programming method.
14. Make sure to input $\overline{RES}$ signal after power-on.

Power Supply

$V_{CC}1$-$V_{CC}3$: Connect $V_{CC}1$-$V_{CC}3$ with +5 V.

GND1-GND6: Ground GND1-GND6.

CRT Display Interface

R, G, B: Input CRT display R, G, B signals on R, G and B respectively.

HSYNC: Input the CRT horizontal synchronization on HSYNC.

VSYNC: Input the CRT vertical synchronization on VSYNC.

DISPTMG: Input the display timing signal, which announces the horizontal or vertical display period, on DISPTMG.

DOTCLK: Input the dot clock for CRT display on DOTCLK.

LCD Interface

R0-R3: R0-R3 output R data for the LCD.

LU0-LU3: LU0-LU3 output LCD up panel data.

G0-G3: G0-G3 output G data for the LCD.

LD0-LD3: LD0-LD3 output LCD down panel data.

B0-B3: B0-B3 output B data for the LCD.

CL1: CL1 outputs the line select clock for LCD data.

CL2: CL2 outputs the shift clock for LCD data.

CL3: CL3 outputs the line select and shift clock when a Y-driver is set on one side of an LCD screen (see "LCD System Configuration").

CL4: CL4 outputs the line select and shift clock when Y-drivers are set on both sides of an LCD screen (see "LCD System Configuration").

FLM: FLM outputs the first line marker for a Y-driver.

M: The M output signal converts the LCD drive signal to AC.

LDOTCK: LDOTCK outputs the LCD dot clock.

Buffer Memory Interface

$\overline{MCS0}$, $\overline{MCS1}$: $\overline{MCS0}$ and $\overline{MCS1}$ output the buffer memory chip select signal.

$\overline{MWE}$: $\overline{MWE}$ outputs the write enable signal of buffer memories.

MA0-MA15: MA0-MA15 output buffer memory addresses.

RD0-RD7: RD0-RD7 transfer data between R data buffer memory and the LVIC.

GD0-GD7: GD0-GD7 transfer data between G data buffer memory and the LVIC.

BD0-BD7: BD0-BD7 transfer data between B data buffer memory and the LVIC.

Mode Setting

PMOD0, PMOD1: The PMOD0-PMOD1 input signals select a programming method (table 6).

DOTE: The DOTE input signal switches the timing of the data latch. The LVIC latches R, G, B signal at the falling edge of DOTCLK when DOTE is high, and at the rising edge when low.

SPS: The SPS input signal selects the polarity of VSYNC. (The polarity of HSYNC is fixed.) VSYNC is high active when SPS is high, and low active when low.

DM0-DM3: The DM0-DM3 input signals select a display mode (table 8).

MS0-MS1: The MS0-MS1 input signals select the kind of buffer memories (table 2).

XDOT: The XDOT input signal specifies the number of horizontal displayed characters. The number is 90 when XDOT is high, and 80 when low.

YL0-YL2: The YL0-YL2 input signals specify the number of vertical displayed lines (table 3).

ADJ: The ADJ input signal determines whether F0-F3 pins adjust the number of vertical displayed lines or the display timing signal. F0-F3 pins adjust the display timing signal when ADJ is high, and adjust the number of vertical displayed lines when low.

F0-F3: F0-F3 input data for adjusting the number of vertical displayed lines (table 4), or the display timing signal (see "Fine

Adjustment of Display Timing Signal").

MPU Interface

$\overline{CS}$: The MPU selects the LVIC when $\overline{CS}$ is low.

$\overline{WR}$: The MPU inputs the $\overline{WR}$ write signal to write data into internal registers of the LVIC. The MPU can write data when $\overline{WR}$ is low and cannot write data when high.

$\overline{RD}$: The MPU inputs the $\overline{RD}$ read signal to read data from internal registers of the LVIC. The MPU can read data when $\overline{RD}$ is low and cannot read data when high.

RS: The MPU inputs the RS signal together with $\overline{CS}$ to select internal registers. The MPU selects data registers (R0-R15) when RS is high and $\overline{CS}$ is low, and selects the address register (AR) when RS is low and $\overline{CS}$ is low.

D0-D3: D0-D3 transfer internal register data between the MPU and LVIC.

$\overline{RES}$: $\overline{RES}$ inputs the external reset signal.

ROM Interface

A0-A3: A0-A3 output address 0 to address 3 to an external ROM.

D0-D3: D0-D3 input data from an external ROM to internal registers.

PLL Circuit Interface

$\overline{CD}$: $\overline{CD}$ outputs the charge down signal to an external charge pump.

$\overline{CU}$: $\overline{CU}$ outputs the charge up signal to an external charge pump.

Table 2 Memory Type and MS1, MS0 Pins

MS1	MS0	Memory Type
0	0	No memory
0	1	8-kbytes memory
1	0	32-kbytes memory
1	1	64-kbytes memory

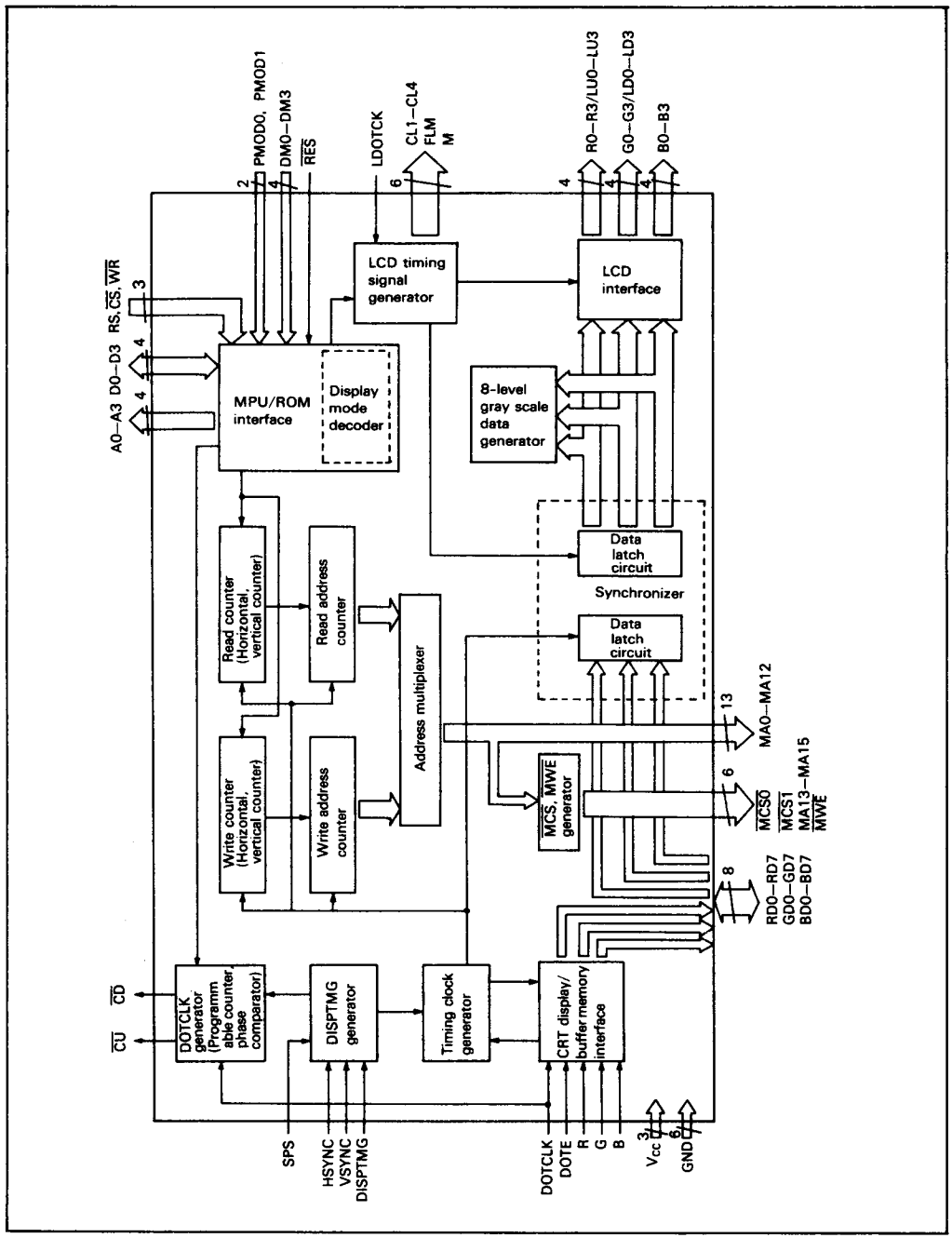
Table 3 Number of Vertical Displayed Lines and YL0-YL2 Pins

YL2	YL1	YL0	Number of Vertical Displayed Lines
0	0	0	200
0	0	1	350
0	1	0	400
0	1	1	480
1	0	0	512
1	0	1	540
1	1	0	Prohibited
1	1	1	

Table 4 Fine Adjustment of Vertical Displayed Lines

F3	F2	F1	F0	Number of Lines Adjusted
0	0	0	0	± 0
0	0	0	1	+ 1
0	0	1	0	+ 2
⋮	⋮	⋮	⋮	⋮
1	1	1	0	+ 14
1	1	1	1	+ 15

Internal Block Diagram



Registers

Table 5 lists the internal registers and figure 1 illustrates the bit assignment to the registers.

Table 5 Register List

$\overline{CS}$	RS	Address Register 3	2	1	0	Reg. No.	Register Name	Program Unit	Read/ Write
1	—	—	—	—	—	—	Invalid	—	—
0	0	—	—	—	—	AR	Address register[1]	—	W
0	1	0	0	0	0	R0	Control register 1	—	R/W
0	1	0	0	0	1	R1	Control register 2	—	R/W
0	1	0	0	1	0	R2	Vertical displayed lines register (middle-order)[2]	Line	R/W
0	1	0	0	1	1	R3	Vertical displayed lines register (low-order)[2]	Line	R/W
0	1	0	1	0	0	R4	Vertical displayed lines register (high-order)[2]	Line	R/W
							CL3 period register (high-order)[3]	Char	R/W
0	1	0	1	0	1	R5	CL3 period register (low-order)[3]	Char	R/W
0	1	0	1	1	0	R6	Horizontal displayed characters register (high-order)[4]	Char	R/W
0	1	0	1	1	1	R7	Horizontal displayed characters register (low-order)	Char	R/W
0	1	1	0	0	0	R8	CL3 pulse width register	Char	R/W
0	1	1	0	0	1	R9	Fine adjust register[5]	Dot	R/W
0	1	1	0	1	0	R10	PLL frequency-dividing ratio register (high-order)[6]	—	R/W
0	1	1	0	1	1	R11	PLL frequency-dividing ratio register (low-order)[6]	—	R/W
0	1	1	1	0	0	R12	Vertical backporch register (high-order)[2,7]	Line	R/W
0	1	1	1	0	1	R13	Vertical backporch register (low-order)[2,7]	Line	R/W
0	1	1	1	1	0	R14	Horizontal backporch register (high-order)[2,7]	Dot	R/W
0	1	1	1	1	1	R15	Horizontal backporch register (low-order)[2,7]	Dot	R/W

Notes: 1. If you attempt to read data from the register with RS = 0, the bus is driven to high-impedance state and the output data is indefinite.
2. (The specified value − 1) should be written into these registers.
3. Valid only in 8-color display modes with horizontal stripes.
4. The most significant bit is invalid in dual screen configuration modes.
5. Valid only when the display timing signal is supplied externally.
6. Valid only when generating the dot clock.
7. Valid only when generating the display timing signal internally.

Register No.	Data Bit 3	2	1	0	
—					
AR	Address register				
R0			DSP	DCK	← Control register 1
R1	MC	DON	MS1	MS0	← Control register 2
R2	Vertical displayed				
R3	lines register				
R4					
R5	CL3 period register				
R6	Horizontal displayed				
R7	characters register				
R8	CL3 pulse width register				
R9	Fine adjust register				
R10	PLL frequency-				
R11	dividing ratio register				
R12	Vertical Backporch				
R13	register				
R14	Horizontal Backporch				
R15	register				

Note: ▨ indicates invalid bits. Attempting to read data from these register bits returns indefinite output data.

Figure 1 Register Bit Assignment

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System Configuration

Figure 2 is the block diagram of a system in which the LVIC is used outside of a personal computer.

The LVIC converts the R, G, B serial data sent from the personal computer into parallel data and writes them into the buffer memories once. It reads out the data in turn and outputs them to LCD drivers to drive an LCD. Here the latch clock of the serial data, namely the dot clock (DOTCLK) is generated by a PLL circuit, using HSYNC as a basic clock. The frequency of the dot clock is specified by the PLL frequency-dividing ratio register (R10, R11).

The user may also configure a system without VCO and LPF if supplying the dot clock externally and may configure a system without the MPU if the LVIC is controlled by the pin programming method.

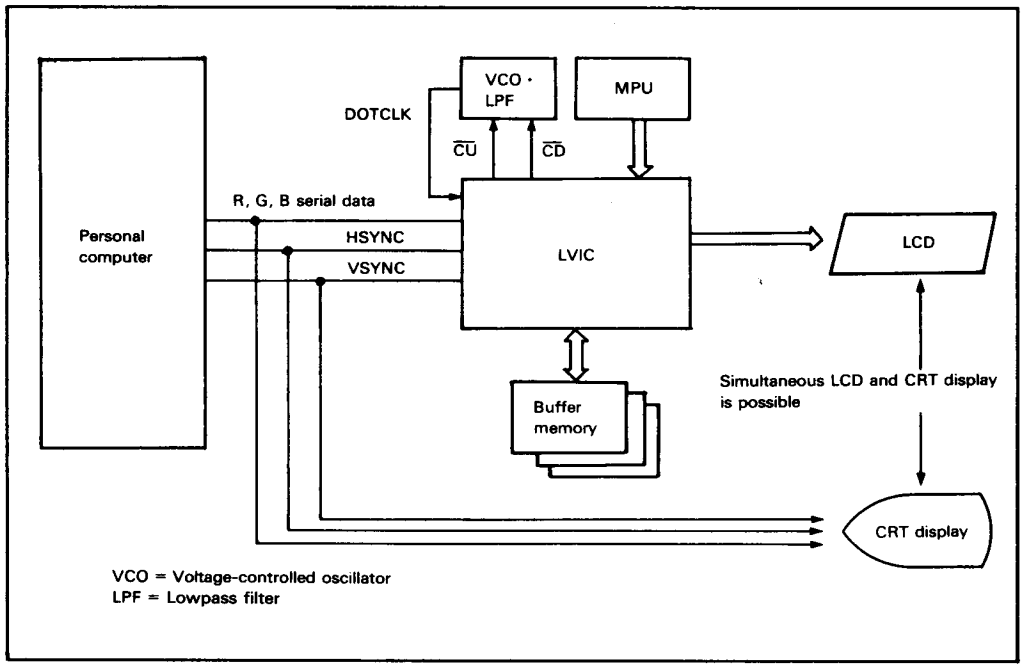

Figure 2 System Block Diagram (MPU Programming Method, Regenerates DOTCLK)

Functional Description

Programming Method

The user may select one of two methods to control the LVIC functions: by pin programming method or by internal registers (internal register programming method). The internal register programming method can be divided into the MPU programming method and the ROM programming method. The MPU writes data into internal registers in the MPU programming method and ROM writes the data in the ROM programming method. Table 6 lists the relation between programming method and pins.

Pin Programming Method: LVIC mode setting pins control functions in the pin programming method.

Internal Register Programming Method: In the internal register programming method, an MPU or ROM writes data into internal registers to control functions. Figure 3 illustrates the connections of MPU or ROM and the LVIC. Figure 3 (1) is an example of using a 4-bit microprocessor, but since the LVIC's MPU bus is compatible with the 4-MHz 80-family controller bus, it can also be connected directly with the bus of host MPU.

Table 6 Programming Method Selection

Pins			
PMOD1	**PMOD0**	**Programming Method**	
0	0	Pin programming	
0	1	Internal register	With MPU
1	0	Programming	With ROM
1	1	Prohibited (Note)	

Note: This combination is for a test mode and disables display.

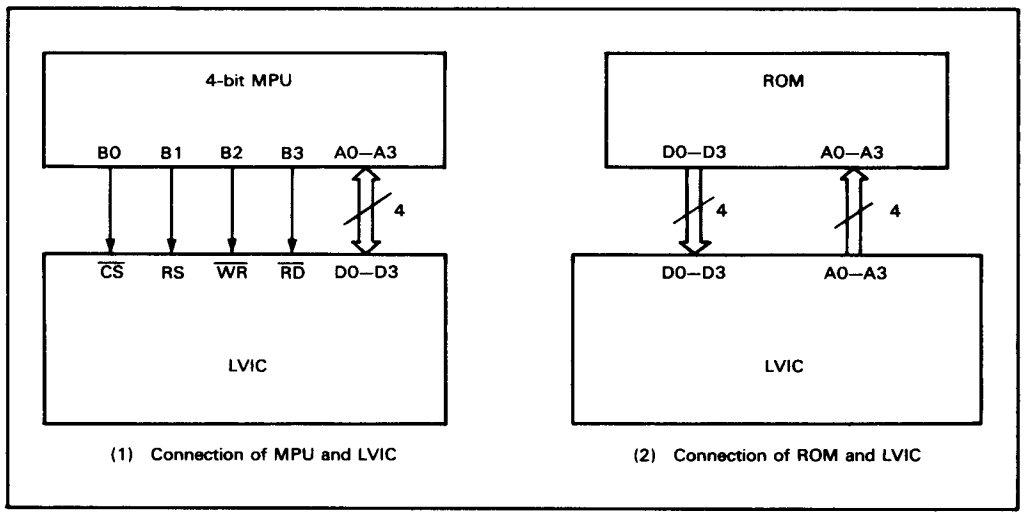

Figure 3 Connection of MPU or ROM and LVIC

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Screen Size

Screen size can be programmed either by pins or internal registers.

In the pin programming method, the user may select either 640 dots or 720 dots (80 characters or 90 characters) as the number of horizontal displayed characters with the XDOT pin, and 200, 350, 400, 480, 512, or 540 lines as the number of vertical displayed lines with YL2-YL0 pins. The number of vertical displayed lines can be adjusted with ADJ and F3-F0 pins within +0 to +15 lines.

In the internal register programming method, the user may select any even number from 32 dots to 4048 dots (= 4 characters up to 506 characters) with the horizontal displayed characters register (R6, R7), and any even number from 4 lines up to 1028 lines with the vertical displayed lines register (R2, R3 and the high-order two bits of R4). However, odd number of lines can also be selected when screen configuration is single and a Y-driver (scan driver) is set on one side of an LCD screen.

Figure 4 illustrates the relation between an LCD screen and pins and internal registers controlling screen size.

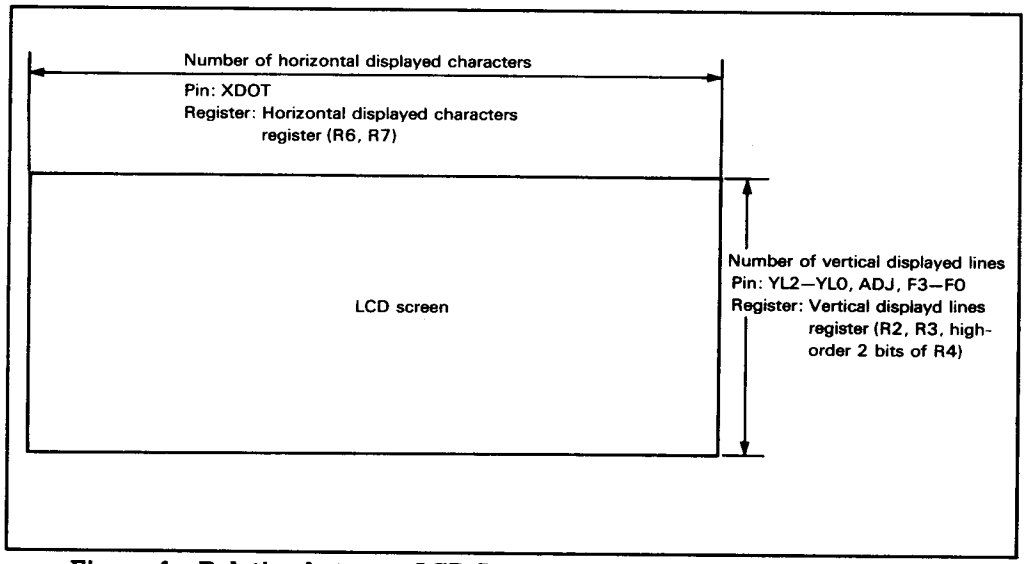

Figure 4 Relation between LCD Screen and Pins and Internal Registers

Memory Selection

The user may select 8-, 32-, or 64-kbyte SRAMs as buffer memory for the LVIC. Since the LVIC has a chip selector for these memories, no external decoder is required. The user selects the memory with pins MS1 and MS0 or with data bits MS1 and MS0 of the control register 2 (R1). Table 7 lists the kinds of memories and pin address assignments.

Memory capacity required depends on screen size and can be obtained with the following expression:

Memory capacity (bytes) = Nhd × Nvd
Nhd: number of horizontal displayed characters
Nvd: number of vertical displayed lines

For example, a screen of 640 × 200 dots requires 16-kbyte memory capacity since 80 characters × 200 lines is 16 kbytes. (8 dots compose a character.) Therefore, each plane needs two HM6264s, which have 8-kbyte memory capacity, in 8-level gray scale display modes. Connect $\overline{MCS0}$ with one of the memories of each plane and $\overline{MCS1}$ with the other (figure 5 (a)).

When the screen size is 640 × 400 dots, 32-kbyte memory capacity is required (figure 5 (b)). Therefore, each plane needs a HM62256, which have 32-kbyte memory capacity.

Connect $\overline{MCS0}$ with $\overline{CS}$ of the memories here.

Table 7 Memories and Pin Address Assignment

Pins or Bits					
MS1	**MS0**	**Memory**	**Address Output Pins**	**Chip Select Pins**	**Address Assignment**
0	0	No memory[1]	—	—	—
0	1	8-kbytes	MA0-MA12	$\overline{MCS0}$	$0000-$1FFF
				$\overline{MCS1}$	$2000-$3FFF
				MA13	$4000-$5FFF
				MA14	$6000-$7FFF
				MA15	$8000-$9FFF
1	0	32-kbytes	MA0-MA14	$\overline{MCS0}$	$00000-$07FFF
				$\overline{MCS1}$	$08000-$0FFFF
				MA15	$10000-$17FFF
1	1	64-kbytes	MA0-MA15	$\overline{MCS0}$	$00000-$0FFFF
				$\overline{MCS1}$	$10000-$1FFFF

Note: 1. There are some limitations when the user uses no memory. Refer to "User Precautions."

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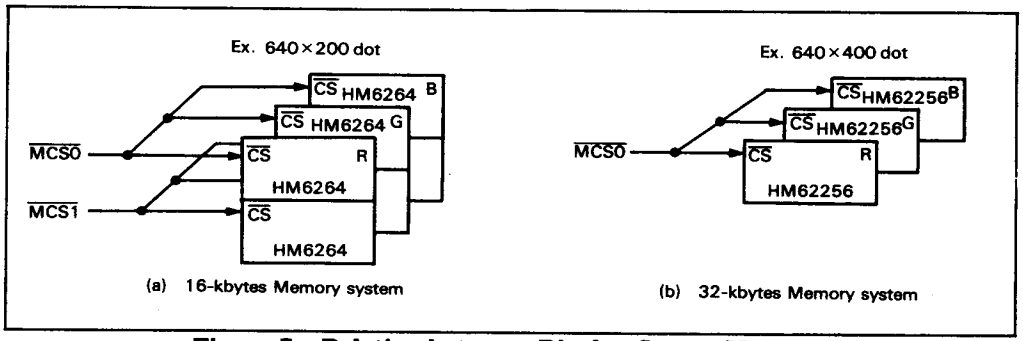

Figure 5 Relation between Display Screen Memories

Display Modes

The LVIC supports 16 display modes, depending on the state of the DM3-DM0 pins. The display mode consists of display color, type of LCD data output, how to set LCD drivers around an LCD screen, how to arrange color data (= type of stripes), and how to output M signal (= type of alternating signal). Table 8 lists display modes.

Table 8 Modes List

Mode	Pins				Display	LCD Data Output		LCD Driver Setting			
						Data	Screen				
No.	DM3	DM2	DM1	DM0	Color	Transfer	Config.	X-Driver[2]	Y-Driver[3]	Stripe[4]	Alternating
1	0	0	0	0	Monochrome	4-bits	Dual	One side	One side	—	Per frame
2	0	0	0	1			Single				
3[1]	0	0	1	0					Both sides		
4	0	0	1	1		8-bits			One side		
5[1]	0	1	0	0					Both sides		
6	0	1	0	1	8-level	4-bits	Dual		One side		
7	0	1	1	0	gray scale		Single				
8	0	1	1	1		8-bits					
9[1]	1	0	0	0	8-color	12-bits				Vertical	Per line
10[1]	1	0	0	1		(4 bits			Both sides		
11[1]	1	0	1	0		for R,G,B		Both sides	One side		
12[1]	1	0	1	1		each)			Both sides		
13[1]	1	1	0	0				One side	One side	Horizontal	
14[1]	1	1	0	1					Both sides		
15[1]	1	1	1	0				Both sides	One side		
16[1]	1	1	1	1					Both sides		

Notes: 1. For TFT-type LCD
2. Data output driver
3. Scan driver
4. Refer to "Display Color, 8-Color Display"

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Display Color

The LVIC converts R, G, B, the color data for CRT display, into the monochrome, 8-level gray scale, or 8-color display data.

Monochrome Display (Mode 1 to Mode 5): In monochrome modes 1-5, the LVIC displays two colors, namely black (= display on) and white (= display off). As shown in table 9, the OR of CRT display R, G, B data determines the display color.

8-Level Gray Scale Display (Mode 6 to Mode 8): In 8-level gray scale modes 6-8, the LVIC thins out data on certain lines to display an 8-level gray scale according to CRT display color (luminosity). Table 10 shows the relation between CRT display color (luminosity) and LCD color (contrast).

8-Color Display (Mode 9 to Mode 16): In 8-color modes 9-16, the LVIC displays 8 colors with red (R), green (G), and blue (B) filters on liquid crystal cells. The eight colors are the same as those provided by CRT display. As illustrated in figure 5, 8-color display has of two stripe modes: horizontal stripe mode and vertical stripe mode. In the former mode, the LVIC arranges R, G, B data horizontally, with horizontal filters. In the latter mode, the LVIC arranges R, G, B data vertically, with vertical filters. Three cells express a dot in both modes.

Table 9 Monochrome Display

CRT Display Data				LCD	
R	G	B	CRT Display Color	On/Off	Color
1	1	1	White	On	Black
1	1	0	Yellow	On	Black
0	1	1	Cyan	On	Black
0	1	0	Green	On	Black
1	0	1	Magenta	On	Black
1	0	0	Red	On	Black
0	0	1	Blue	On	Black
0	0	0	Black	Off	White

Table 10 8-Level Gray Scale Display

CRT Display Data			CRT		LCD	
R	G	B	Color	Luminosity	Color	Contrast
1	1	1	White	High	Black	Strong
1	1	0	Yellow			
0	1	1	Cyan			
0	1	0	Green			
1	0	1	Magenta			
1	0	0	Red			
0	0	1	Blue			
0	0	0	Black	Low	White	Weak

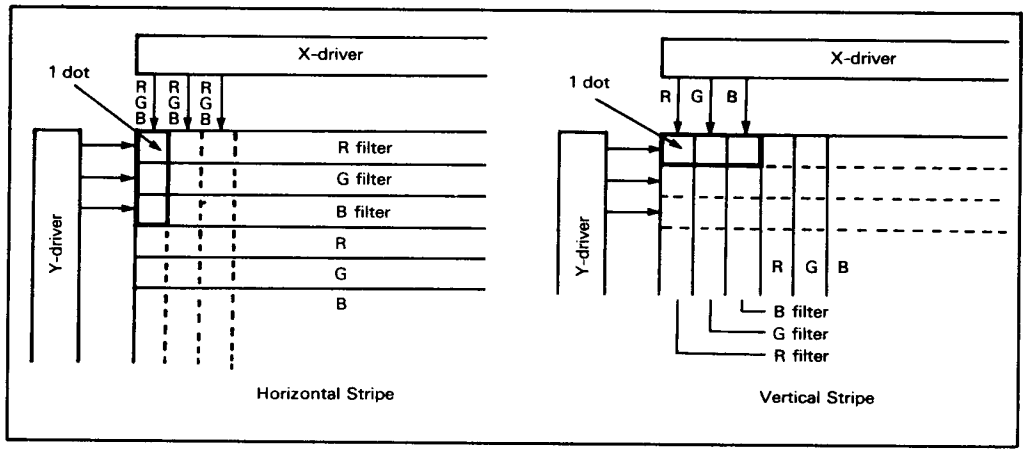

Figure 6 Stripe Modes in 8-Color Display

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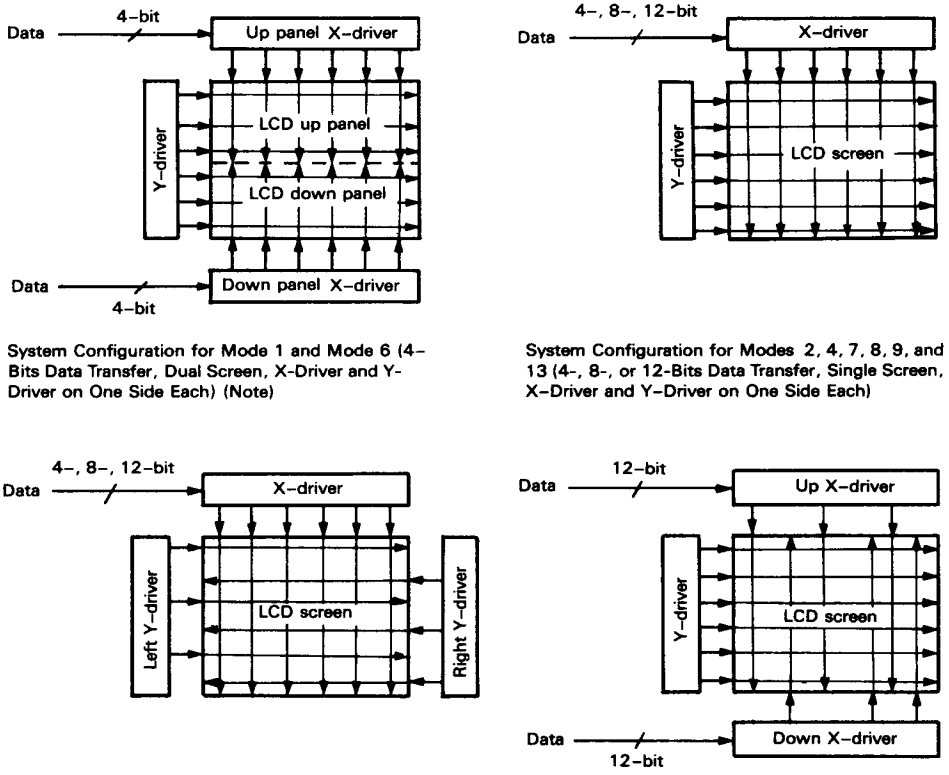
LCD System Configuration

The LVIC supports the following system configurations for LCD:

- Types of LCD data output:
  —Data transfer: 4-bit, 8-bit, or 12-bits (4 bits for R, G, B each)
  —Screen configuration: Single or dual
- How to set LCD drivers around LCD screen:
  —X-driver: On one side or on both sides
  —Y-driver: On one side or on both sides

Figure 7 illustrates these system configurations by mode.



System Configuration for Mode 1 and Mode 6 (4-Bits Data Transfer, Dual Screen, X-Driver and Y-Driver on One Side Each) (Note)

System Configuration for Modes 2, 4, 7, 8, 9, and 13 (4-, 8-, or 12-Bits Data Transfer, Single Screen, X-Driver and Y-Driver on One Side Each)

System Configuration for Modes 3, 5, 10, and 14 (4-, 8-, or 12-Bits Data Transfer, Single Screen, X-Driver on One Side and Y-Driver on Both Sides)

System Configuration for Mode 11 and Mode 15 (12-Bits Data Transfer, Single Screen, X-Driver on Both Sides and Y-Driver on One Side)

Note: Although there are two X-drivers, the X-driver is considered to be set on one side, not on both sides, because the LCD up panel and down panel are each regarded as one screen.

Figure 7 System Configurations by Mode

Calculation of LDOTCK

LDOTCK frequency f_L is calculated from the following expression:

$f_L = (Nhd + 6) \times 8 \times Nvd \times f_F$

Nhd: number of horizontal characters displayed on LCD

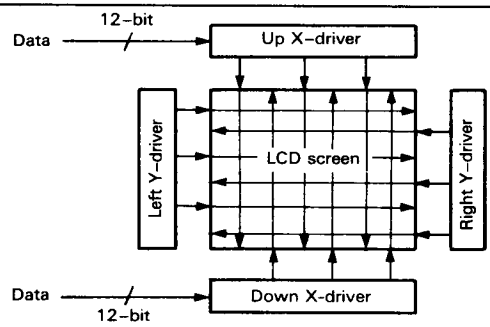
Nvd: number of virtical displayed lines on LCD

f_F: FLM frequency

Here f_L must hold the following relation, where f_D is frequency of dot clock for CRT display (= DOTCLK).

$f_L < f_D \times 15/16$ or

$f_L = f_D$ (The LDOTCK phase must be inverse of the DOTCLK phase in this case)



System Configuration for Mode 12 and Mode 16 (12-Bit Data Transfer, Single Screen, X-Driver and Y-Driver on Both Sides Each)

Notes: 1. X-drivers on both sides: Data output wires run from up and down X-drivers alternately, which widens the interval between wires to twice that for an X-driver an one side (figure 8).

2. Y-drivers on both sides: Line select signal output wires run from right and left Y-drivers alternately, which widens the interval between wires to twice that for Y-driver on one side (figure 9).

Figure 7 System Configurations by Mode (cont)

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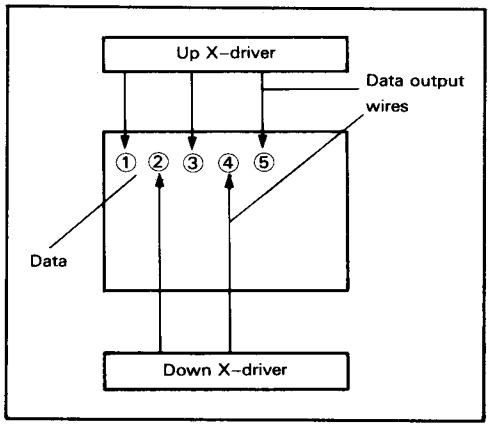


Figure 8 X-Drivers on Both Sides

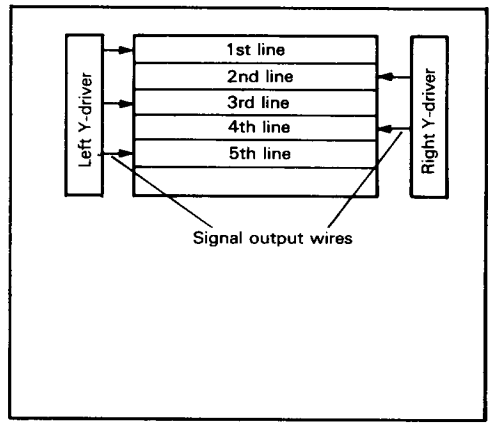


Figure 9 Y-Drivers on Both Sides

Display Timing Signal Generation

CRT display data is classified into display period data and retrace period data. Only display period data is necessary for LCD. Therefore, the LVIC needs a signal announcing whether the CRT display data transferred is for the display period or not. This signal is the display timing signal.

The LVIC can generate the display timing signal from HSYNC and VSYNC. Figure 10 illustrates the relation between HSYNC, VSYNC, the display timing signal (DISPTMG), and display data. Y lines and X dots in the figure are specified by the vertical backporch register (R12, R13) and the horizontal backporch register (R14, R15) respectively.

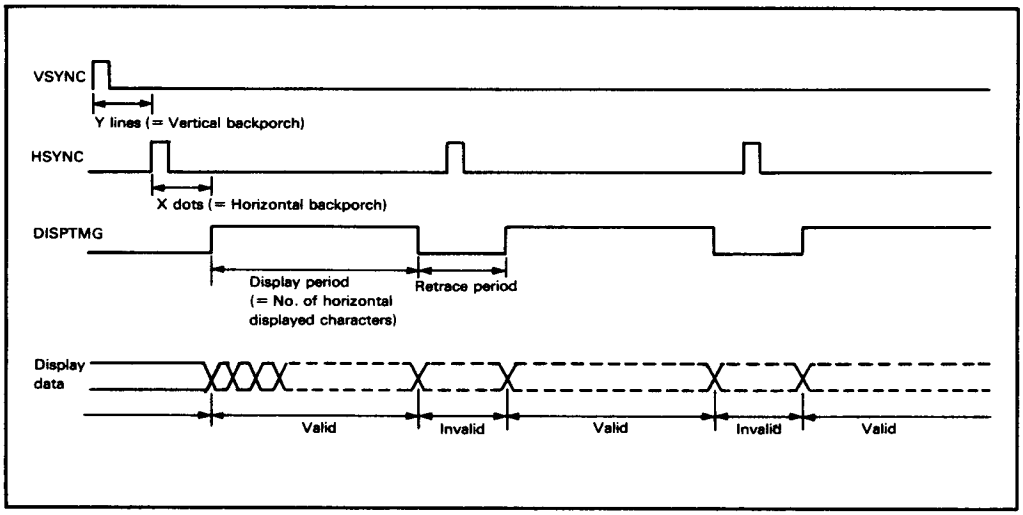


Figure 10 Relation between HSYNC, VSYNC, DISPTMG, and Display Data

Dot Clock Generation

The dot clock, which is a data latch clock, is not a standard video signal and does not appear from the CRT display plug. Thus it is necessary to generate the dot clock. The LVIC has a programmable counter and a phase comparator which are parts of a PLL circuit, and can generate the dot clock from HSYNC if a charge pump, a lowpass filter (LPF), and a voltage-controlled oscillator (VCO) are externally attached.

Figure 11 is a block diagram of a PLL circuit. A PLL (phase-locked loop) circuit is a feedback controller regenerating a clock whose frequency and phase are the same as those of a basic clock. The basic clock is HSYNC here.

At power-on, VCO outputs to the programmable counter a signal whose frequency depends on the voltage at the time. The counter divides the frequency of the signal according to the value in the PLL frequency-dividing ratio register (R10, R11) and outputs it to the phase comparator. This is the frequency-divided clock.

The comparator compares the edges of the clock and HSYNC and outputs $\overline{CU}$ or $\overline{CD}$ signal to the charge pump and LPF according to the result. The comparator outputs $\overline{CU}$ when the frequency of the clock is lower than that of HSYNC or when the phase of the clock is behind that of HSYNC, while it outputs $\overline{CD}$ in the contrary case. The charge pump and LPF apply voltage to the VCO according to $\overline{CU}$ or $\overline{CD}$ signal.

This operation is repeated until the phase and the frequency of the frequency-divided clock coincide with those of HSYNC, making it a stable dot clock.

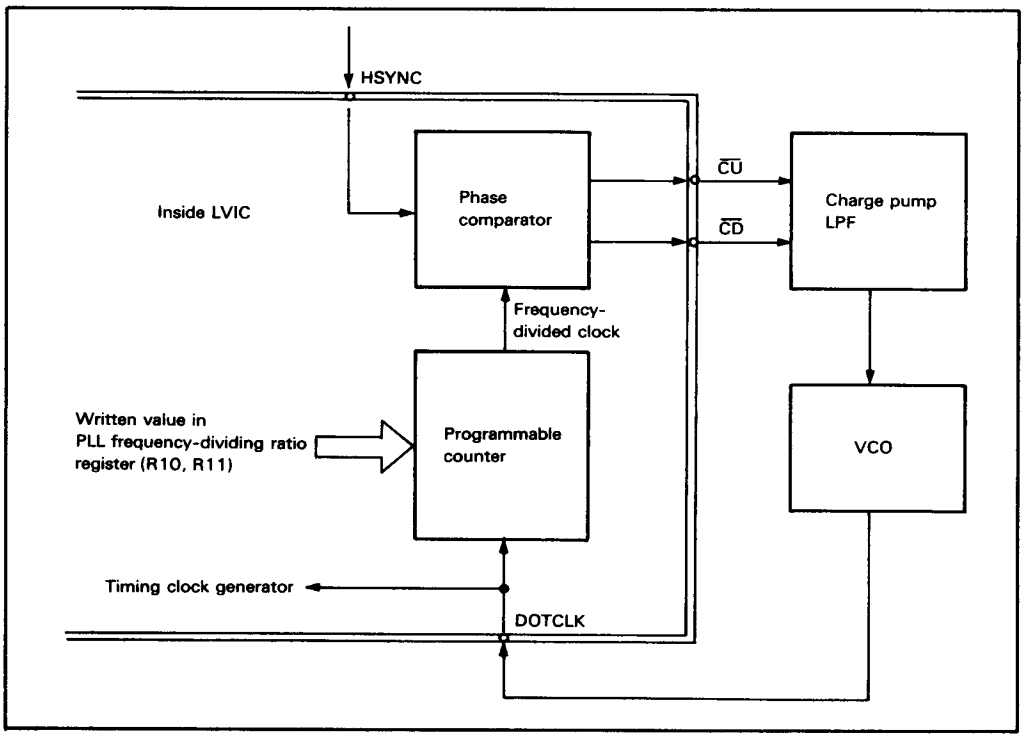


Figure 11 PLL Circuit Block Diagram

5

Doubled-in-Height Display

Doubled-in-height display doubles characters and pictures in height as illustrated in figure 12.

In TN-type LCD modes (= modes 1, 2, 4, 6, 7, and 8), CL3 frequency is twice as high as CL1 frequency (figure 13). As a result, using CL3 instead of CL1 as a shift clock (figure 14) enables two lines to be selected while an X-driver (data output driver) is outputting the same data, realizing doubled-in height display. However, the following procedures are necessary in this display since multiplexing duty ratio becomes twice as great as the value specified as the number of vertical displayed lines.

1. Halve the frequency of the LCD dot clock (= LDOTCK)
2. Halve the number of vertical displayed lines

This function is provided only for TN-type LCD.

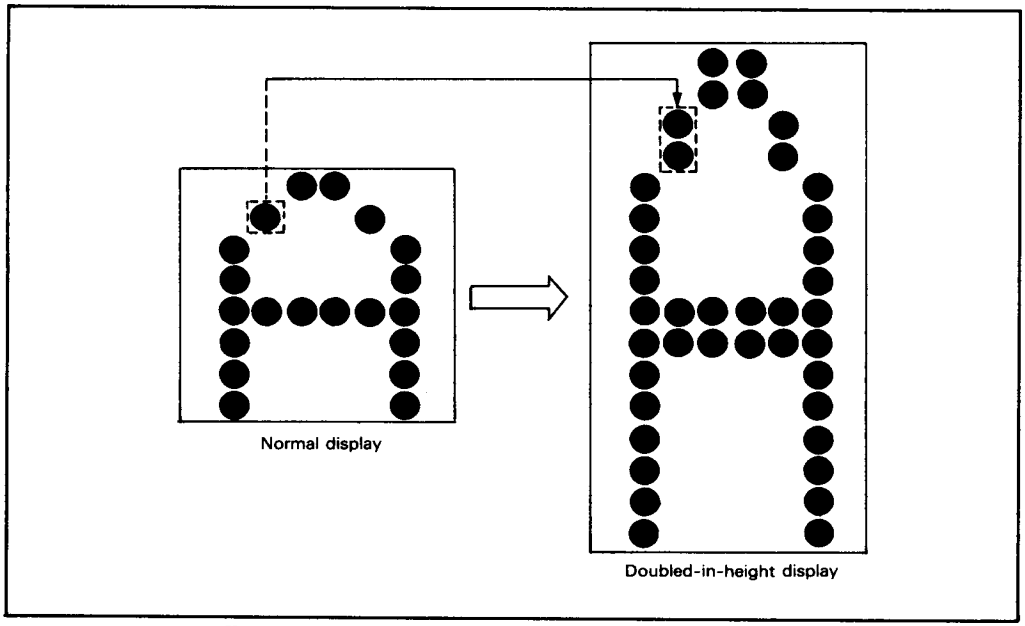


Figure 12 Doubled-in-Height Display Example

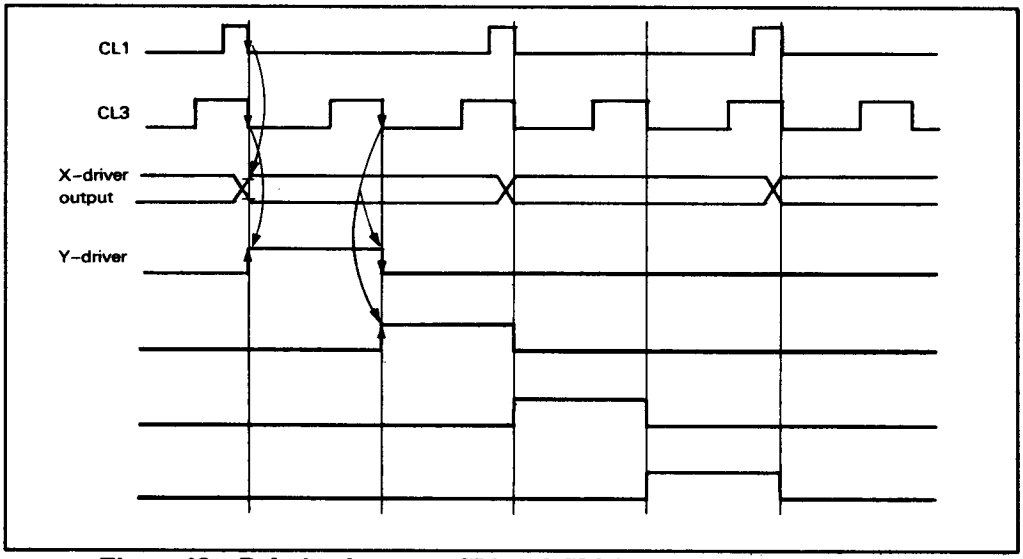


Figure 13 Relation between CL1 and CL3 in Modes 1, 2, 4, 6, 7, and 8

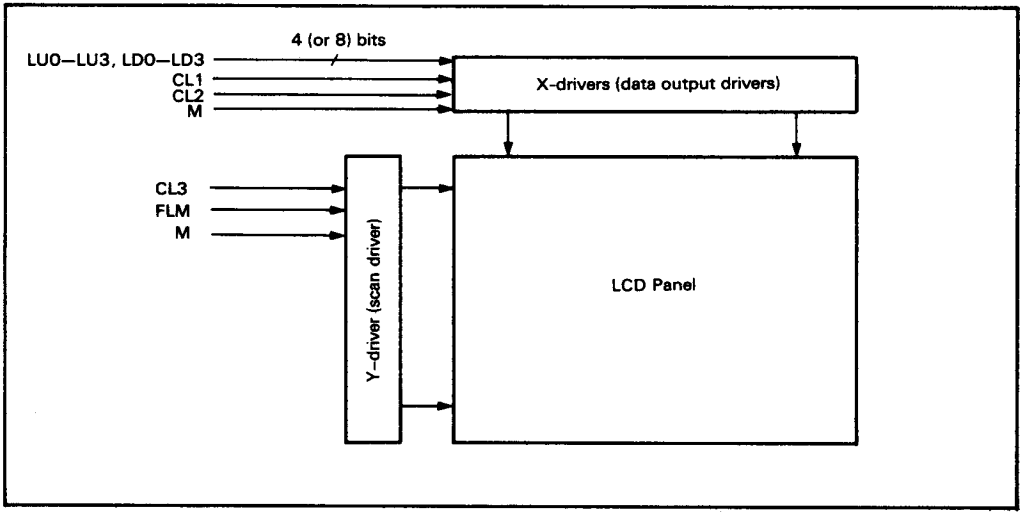


Figure 14 Connection for Doubled-in-Height Display

5

Display Timing Signal Fine Adjusment

When the display timing signal is supplied externally, a phase shift might appear between CRT data and the display timing signal. This is because each signal has its own peculiar lag. The LVIC can adjust the display timing signal with the F0-F3 pins or the fine adjust register (R9) to correct this phase shift.

Table 11 shows the relation between F3-F0 pins, data bit 3 to data bit 0 of the fine adjust register, and fine adjustment. Concerning the polarity of the number of dots adjusted, − indicates advancing the phase of the display timing signal and + indicates delaying it. F3 pin or data bit 3 of R9 selects the polarity. The adjustment reference point is the display start position.

Figure 15 shows examples of adjusting the display timing signal. Since the signal is two dots ahead of the display start position in case (1), (F3, F2, F1, F0) or (data bits 3, 2, 1, 0 of R9) should be set to (1, 0, 1, 0) to delay the signal for two dots. Since the signal is two dots behind the display start position in case (2), they should be set to (0, 0, 1, 0) to advance the signal for two dots. When there is no need to adjust the signal, settings of either (0, 0, 0, 0) or (1, 0, 0, 0) will do.

Table 11 Pins, Data Bits of R9, and Fine Adjustment

Pin:	F3	F2	F1	F0	Number of Dots
R9 Bit:	3	2	1	0	Adjusted
	0	0	0	0	0
		0	0	1	− 1
		⋮	⋮	⋮	⋮
		1	1	0	− 6
		1	1	1	− 7
	1	0	0	0	0
		0	0	1	+ 1
		⋮	⋮	⋮	⋮
		1	1	0	+ 6
		1	1	1	+ 7

Note: When adjusting the display timing signal with pins, set ADJ pin to 1.

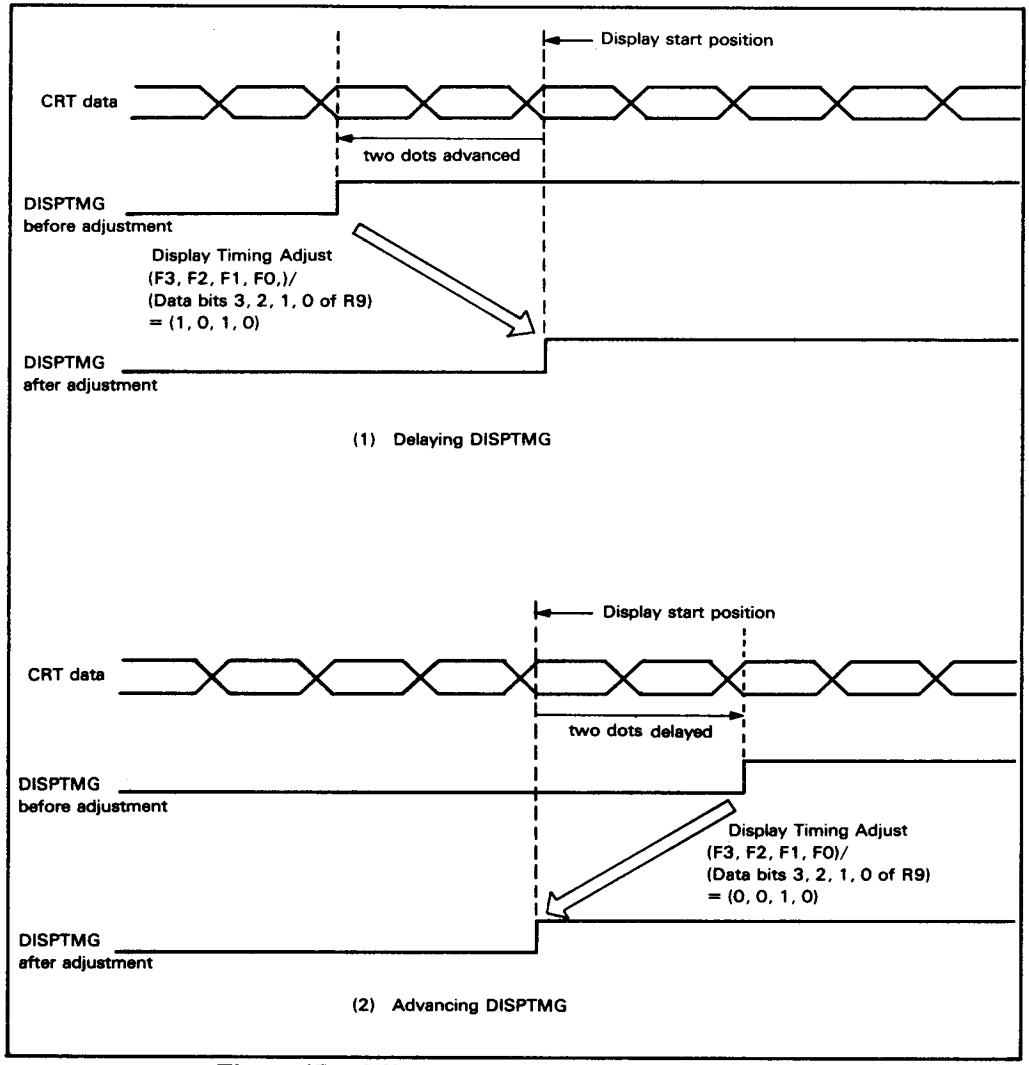


Figure 15 Adjustment of Display Timing Signal

5

Internal Registers

The LVIC has an address register (AR) and sixteen data registers (R0-R15). In order to specify one of the sixteen data registers, write its register address into the address register. The MPU transfers data to the data register corresponding to the written address.

All the registers are valid only when the LVIC is controlled by the internal register programming method and are invalid (don't care) when by the pin programming method.

Address Register (AR)

The address register (figure 16) is composed of four bits and specifies one data register out of sixteen. This register is selected by the MPU when RS pin is low and specifies any data register with the register address written by the MPU.

Control Register 1 (R0)

Control register 1 (figure 17) is composed of four bits, including two invalid bits. Each of two valid bits has its own function. Reading from and writing into invalid bits are possible. However, these operations do not affect the LSI function.

- DSP Bit
  —DSP = 1: LVIC generates the display timing signal
  —DSP = 0: LVIC does not generate the display timing signal
  (If DCK = 1, the display timing signal is generated in spite that DSP = 0)
- DCK Bit
  —DCK = 1: LVIC generates the dot clock
  —DCK = 0: LVIC does not generate the dot clock

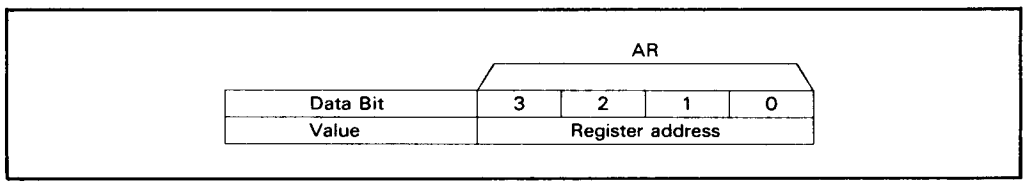


Figure 16 Address Register

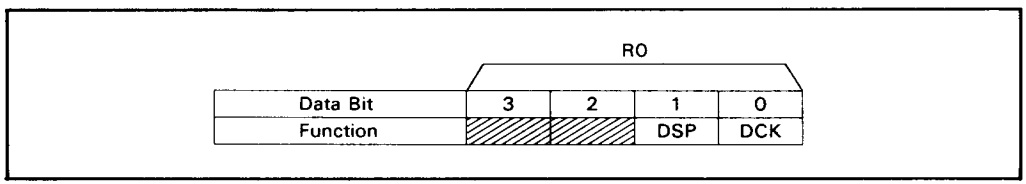


Figure 17 Control Register 1

Control Register 2 (R0)

Control register 2 (figure 18) is composed of four bits and has three functions.

- MC Bit
  —MC = 1: M signal alternates per line
  —MC = 0: M signal alternates per frame
- DON Bit
  —DON = 1: Display on
  —DON = 0: Display off
- MS1 and MS0 Bits
  —Select the memory type (table 12)

Vertical Displayed Lines Register (R2, R3, High-Order 2 Bits of R4), CL3 Period Register (Low-order 2 Bits of R4, R5)

The vertical displayed lines register (figure 19) is composed of ten bits (R2 + R3 + high-order two bits of R4) and specifies the number of vertical displayed lines. This register can specify both even and odd numbers in modes for a Y-driver on one side and single screen configuration, but even numbers only in the other modes. The value to be written into this register is (Nvd − 1), where Nvd = number of vertical displayed lines.

The CL3 period register is composed of six bits (low-order two bits of R4 + R5) and specifies the period of CL3 in 8-color display modes with horizontal stripes. Thus this register is invalid in the other modes. CL3 is a clock for the LVIC to output R, G, B data separately to LCD drivers. The value to be written into this register is (Nhd + 6) × 1/3 − 1, where Nhd = number of horizontal displayed characters. When (Nhd + 6) is not divisible by 3, the quotient should be rounded up or rounded down.

Table 12 Memory Type and MS1, MS0

MS1	MS0	Memory Type
0	0	No memory
0	1	8-kbytes
1	0	32-kbytes
1	1	64-kbytes

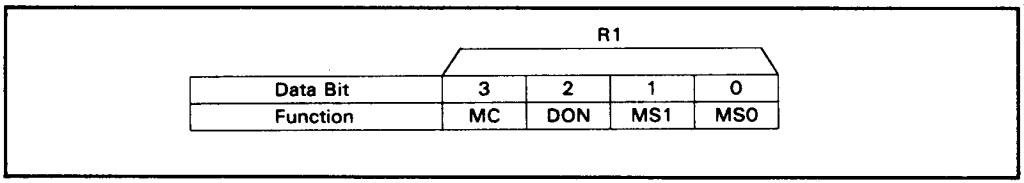


Figure 18 Control Register 2

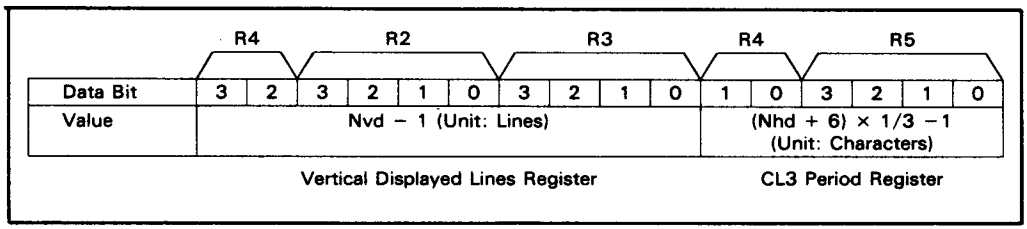


Figure 19 Vertical Displayed Lines Register and CL3 Period Register

Horizontal Displayed Characters Register (R6, R7)

The horizontal displayed characters register (figure 20) is composed of eight bits (R6 + R7) and specifies the number of horizontal displayed characters. This register can specify even numbers only. The most significant bit of R6 is invalid in the modes for dual screen configuration. When writing into this register, shift (Nhd − 1) in the low-order direction for one bit to cut off the least significant bit. Figure 20 shows how to write a value into the register when Nhd = 90.

CL3 Pulse Width Register (R8)

The CL3 period register (figure 22) is composed of four bits and specifies the high-level pulse width of CL3. When controlling TFT-type LCDs, each gate of the LCD has to hold data from the time a Y-driver outputs the line select and shift signal to the time an X-driver the outputs next display data. Data must be held while CL3 is high. However, even when the LVIC is not controlling TFT-type LCDs, CL3 appears with the high-level pulse width specified by this register.

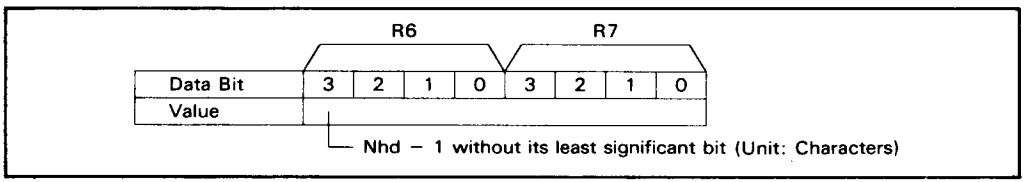


Figure 20 Horizontal Displayed Characters Register

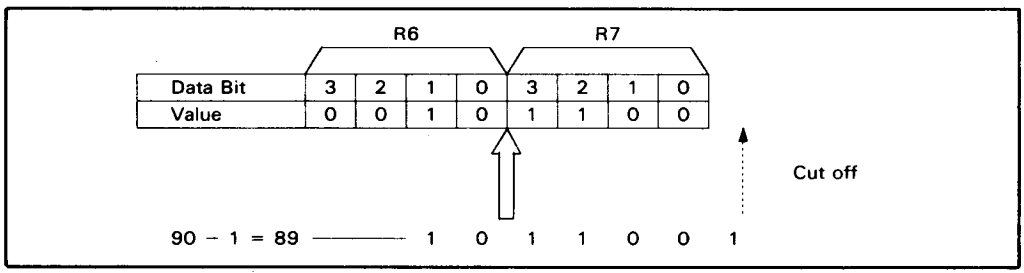


Figure 21 How to Write The Number of Horizontal Displayed Characters

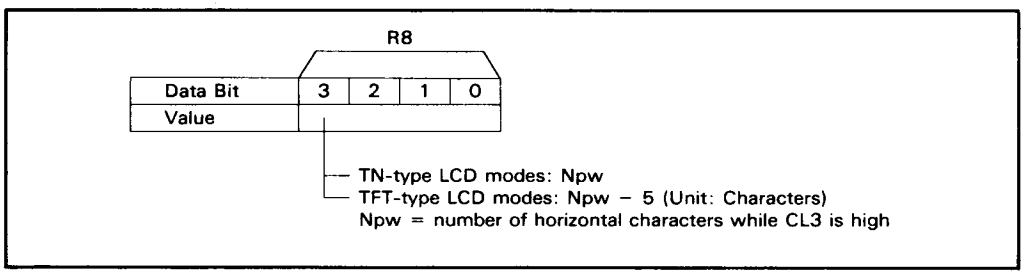


Figure 22 CL3 Pulse Width Register

Fine Adjust Register (R9)

The fine adjust register (figure 23) is composed of four bits and adjusts the externally supplied display timing signal to synchronize its phase with that of LCD data. The value to be written into this register is determined by the interval between the positive edge of the display timing signal and the display start position. For more details, refer to "Display Timing Signal Fine Adjustment." This register is invalid when the display timing signal is generated internally.

PLL Frequency-Dividing Ratio Register (R10, R11)

The PLL frequency-dividing ratio register (figure 24) is composed of eight bits (R10 + R11) and specifies the PLL frequency-dividing ratio for generating a dot clock by a PLL circuit. The value to be written into this register is determined by the ratio of the frequency of HSYNC to that of the dot clock which the user wants. This register is invalid when the dot clock is supplied externally and is valid only when the LVIC is controlled by the internal register programming method and the DCK bit of control register 1 (R0) is 1. The written value in this register (N_{PLL}) is obtained with the following expression:

$N_{PLL} = Ncht \times 8 - 731$

Ncht: total number of characters for CRT

Ncht can be obtained as follows from the specifications of a CRT monitor:

Ncht = 1/8 × (DOTCLK frequency)/(HSYNC frequency)

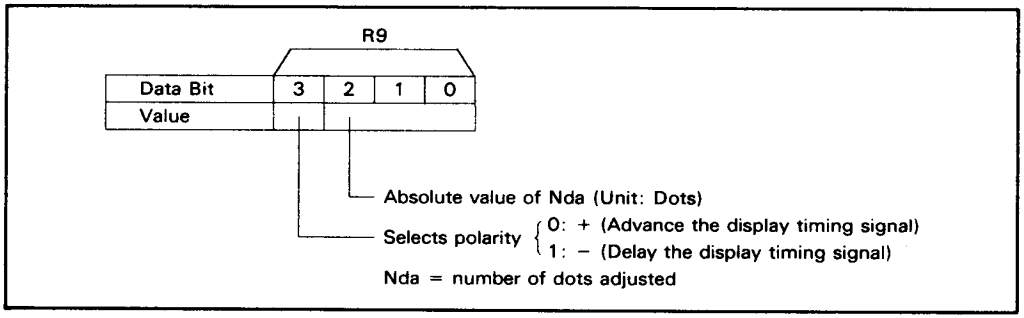
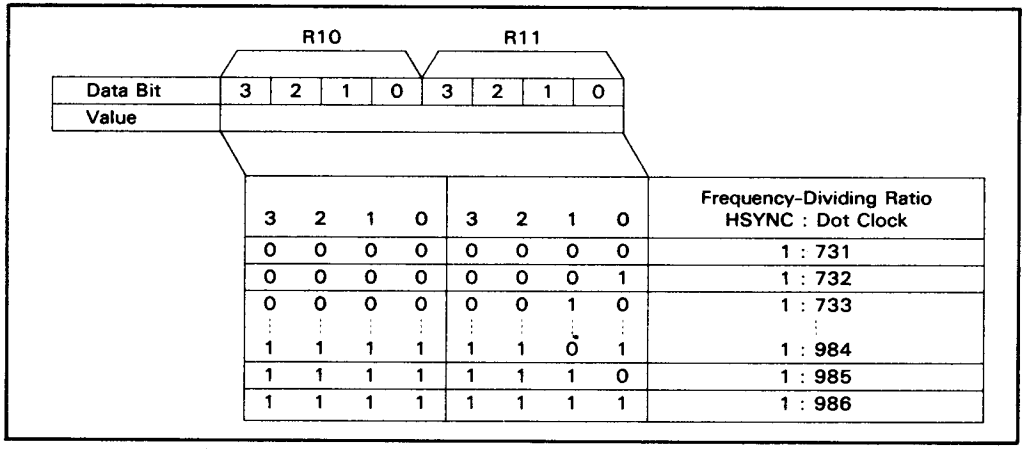


Figure 23 Fine Adjust Register



R10 3	R10 2	R10 1	R10 0	R11 3	R11 2	R11 1	R11 0	Frequency-Dividing Ratio HSYNC : Dot Clock
0	0	0	0	0	0	0	0	1 : 731
0	0	0	0	0	0	0	1	1 : 732
0	0	0	0	0	0	1	0	1 : 733
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	0	1	1 : 984
1	1	1	1	1	1	1	0	1 : 985
1	1	1	1	1	1	1	1	1 : 986

Figure 24 PLL Frequency-Dividing Ratio Register

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Vertical Backporch Register (R12, R13)

The vertical backporch register (figure 25) is composed of eight bits (R12 + R13) and specifies the vertical backporch. The vertical backporch is the number of lines between the positive edge of VSYNC and that of the display timing signal (DISPTMG). For more details, refer to "Display Timing Signal Generation." This register is invalid when the display timing signal is supplied externally and is valid only in a system which controls the LVIC by the internal register programming method and where the DSP bit of control register 1 (R0) is 1. (If the DCK bit of control register 1 (R0) is 1, DISPTMG will always be regenerated and the register is enabled even when DSP = 0.)

Horizontal Backporch Register (R14, R15)

The horizontal backporch register (figure 26) is composed of eight bits (R14 + R15) and specifies the horizontal backporch. The horizontal backporch is the number of characters between the positive edge of HSYNC and that of the display timing signal (DISPTMG). For more details, refer to "Display Timing Signal Generation". This register is invalid when the display timing signal is supplied externally and is valid only in a system which controls the LVIC by the internal register programming method and where the DSP bit of control register 1 (R0) is 1. (If the DCK bit of control register 1 (R0) is 1, DISPTMG will always be generated and this register is enabled even when DSP = 0.)

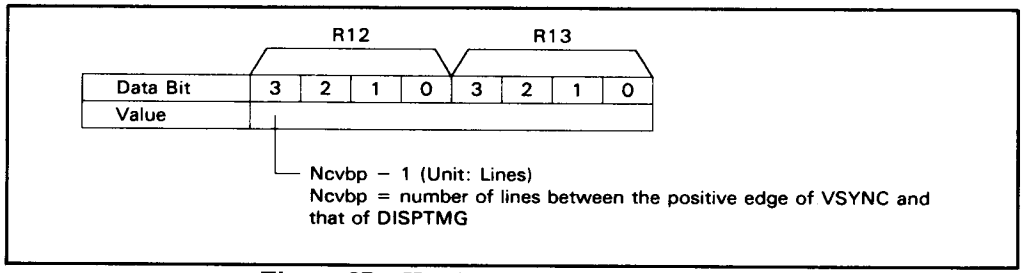

Figure 25 Vertical Backporch Register

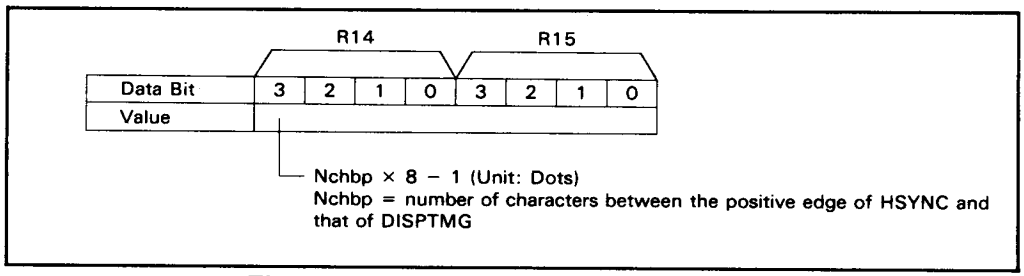

Figure 26 Horizontal Backporch Register

Reset

$\overline{RES}$ pin resets and starts the LVIC. Make sure to hold the reset signal low for at least 1 μs after power-on.

Reset is defined as shown in figure 27.

State of Pins During Reset

$\overline{RES}$ basically does not control output pins and operates regardless of the other input pins. Output pins can be classified into the following five groups depending on their reset state.

1. Keeps state before reset: CL2
2. Driven to high-impedance state (fixed low when using no memory): RD0-RD7, GD0-GD7, BD0-BD7
3. Fixed high: $\overline{MWE}$, CL4, M, $\overline{CD}$, $\overline{MCS1}$
4. Fixed low: MA0-MA12, R0-R3, G0-G3, B0-B3, $\overline{CS}$, CL1, CL3, FLM, A0-A3, $\overline{CU}$
5. Fixed high or low depending on the memory in use (table 13): MA13-MA15, $\overline{MCS0}$

State of Registers During Reset

$\overline{RES}$ pin does not affect register contents. Therefore, registers can be both read and written by the MPU even during reset. Registers keep the contents they had before reset until they are rewritten.

Memory Clear Function

After reset, the LVIC writes 0 in the memory area specified by MSEL0 and MSEL1 (table 7) regardless of R, G, B data.

Table 13 Memory Type and State of Pins During Reset

Kind of Memories	MA13	MA14	MA15	$\overline{MCS0}$
No memory	Low	Low	High	High
8-kbyte memory	High	High	High	Low
32-kbyte memory	Low	Low	High	Low
64-kbyte memory	Low	Low	Low	Low

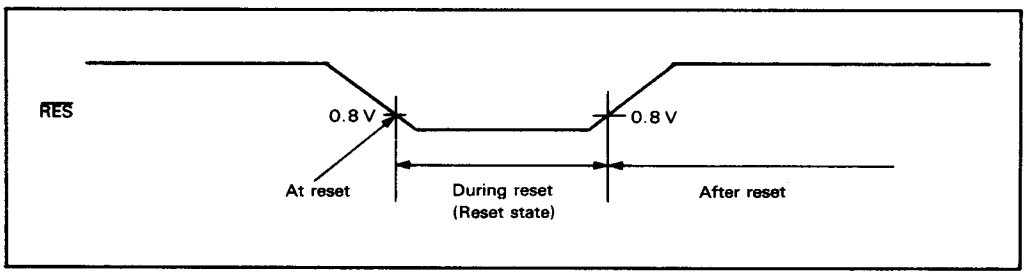

Figure 27 Reset Definition

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User Precautions

1. There are the following limitations when the user uses no memory (MSEL0 = 0, MSEL1 = 1).

   - The display modes for dual screen configuration (= mode 1 and mode 6) are disabled.
   - The LVIC cannot support the LCD systems with Y-drivers on both sides. Even if the user selects the mode for a system with Y-drivers on both sides (= mode 3, 5, 10, 12, 14, or 16), the operation of the LVIC is exactly the same as that in the mode for the system with a Y-driver on one side (= mode 2, 4, 9, 11, 13, or 15).

   Leave CL4 terminal disconnected in this case.

2. The LVIC might operate irregularly until the internal registers have been written after reset in the system which controls the LVIC by internal register programming method.

3. Memory clear function might not work normally at power-on or after reset if MSEL0 and MSEL1 are not properly set to the value corresponding to the memories in use.

4. Since the LVIC is a CMOS LSI, input pins must not be left disconnected. Refer to table 1 concerning how to deal with each pin.

Programming

The values written in internal registers have the limits listed in table 14. The symbols in the table are defined as shown in table 15 and figure 27.

Table 14 Limit on Values Written in Registers

Function	Limit	Notes	Applicable Registers
Screen Configuration	$4 \leq Nvd \leq (Ncvbp + Ncvsp) - 1 \leq 1024$		R2, R3, R4, R6, R7
	$4 \leq Nhd \leq (Nchbp \times 1/n + Nchsp) - 1 \leq 506$	1, 8	
	$(Nhd + 6) \times n \times Nvd \times f_F \leq f_D \leq 30$ MHz	2, 8	R2, R3, R4, R6, R7
CL3 Control	$1 \leq Npw \leq (Nhd + 6) \times 1/2 - 1$	3	R4, R5, R6, R7, R8
	$1 \leq Npw \leq Nhd$	4	
	$1 \leq Npw \leq Npc - 1$	5	
DISPTMG	$1 \leq Nchbp \leq 256$	6	R12, R13, R14, R15
Regeneration	$1 \leq Ncvbp \leq 256$	6	
Without Buffer Memory	$4 \leq Nhd \leq Nchsp - 4$	7	R2, R3, R4, R6, R7
	$4 \leq Nvd \leq Ncvsp - 4$	7	

Notes: 1. $Nhd \leq 256$ in dual screen configuration (= mode 1 and mode 6)
2. f_F: FLM frequency, f_D: frequency of CRT dot clock, f_L: frequency of LCD dot clock for LCD $f_L < f_D \times 15/16$, or $f_L = f_D$
3. In modes 1, 2, 4, 6, 7, and 8
4. In modes 3, 5, 9, 10, 11, and 12 (Npw = (value in R8) + 5)
5. In modes 13, 14, 15, and 16 (Npw = (value in R8) + 5)
6. Value in R14, R15 $\leq$ (Nchsp $\times$ n + Nchbp) $-$ Nhd $\times$ n $-$ 2
   Value in R12, R13 $\leq$ (Ncvsp + Ncvbp) $-$ Nvd $-$ 2
7. Nht = Nchsp + Nchbp $\times$ 1/n, Nd = Ncvbp + Ncvsp
   (Nht = Nhd + 6, Nd = Nvd when using buffer memory)
8. n: Horizontal character pitch (the number of horizontal dots in one character).

Table 15 Symbol Definition

Symbol	Definition
Nchd	Number of horizontal displayed characters on CRT display
Nchsp	Number of characters between the positive edge of DISPTMG and that of HSYNC (= Horizontal sync position)
Nchbp	Number of dots between the positive edge of HSYNC and that of DISPTMG (= horizontal backporch)
Ncvbp	Number of lines between the negative edge (positive edge when VSYNC is high in active state) of VSYNC and the first positive edge of DISPTMG (= vertical backporch)
Ncvsp	Number of lines between the first positive edge of DISPTMG and the next negative edge of VSYNC (= vertical sync position)
Ncvd	Number of vertical displayed lines on CRT display
Nhd	Number of horizontal displayed characters (on LCD)
Npc	Number of characters during CL3 period (= CL3 pulse cycle)
Npw	Number of characters while CL3 is high (= CL3 pulse width)
Nht	Total number of horizontal characters
Nvd	Number of vertical displayed lines (on LCD)

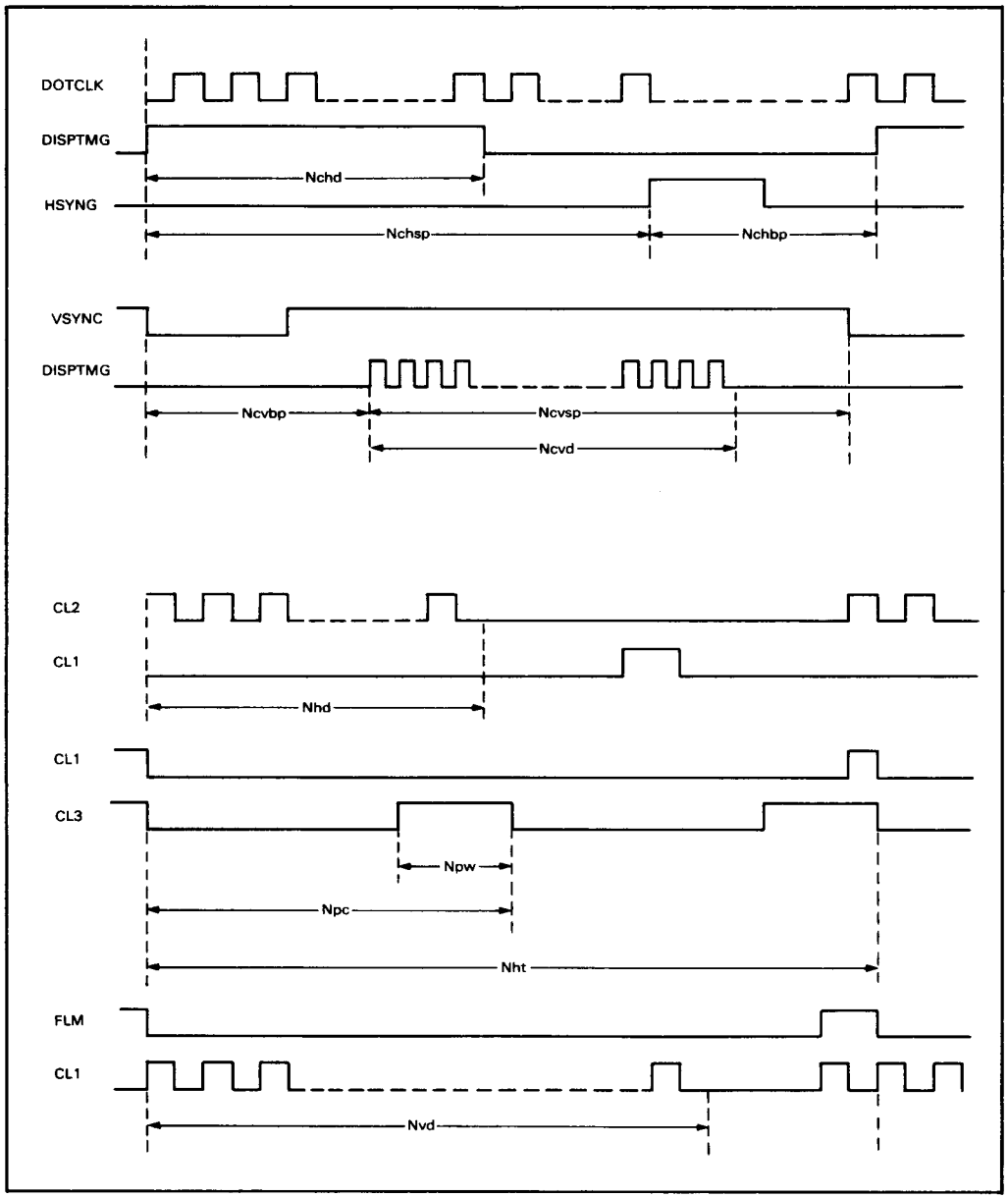

Figure 28 Symbol Definition

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	− 0.3 to + 7.0	V
Input voltage	V_{in}	− 0.3 to V_{CC} + 0.3	V
Operating temperature	T_{opr}	− 20 to + 75	°C
Storage temperature	T_{stg}	− 55 to + 125	°C

Notes: 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions (V_{CC} = 5.0 V ± 10 %, GND = 0 V, Ta = −20°C to +75°C). If these conditions are exceeded, it could affect reliability of the LSI.
2. All voltages are referenced to GND = 0 V.

Electrical Characteristics

DC Characteristics 1 (V_{CC} = 5.0 V ± 10 %, GND = 0 V, Ta = − 20°C to + 75°C, unless otherwise noted)

Item		Symbol	Min	Max	Unit	Test Conditions
Input high voltage	$\overline{RES}$	V_{IH}	V_{CC} − 0.5	V_{CC} + 0.3	V	
	TTL interface[1]		2.0	V_{CC} + 0.3		
	TTL interface[4]		2.2	V_{CC} + 0.3		
	CMOS interface[1]		0.7 V_{CC}	V_{CC} + 0.3		
Input low voltage	TTL interface[1], $\overline{RES}$	V_{IL}	−0.3	0.8	V	
	TTL interface[5]		−0.3	0.6		
	CMOS interface[1]		−0.3	0.3 V_{CC}		
Output high voltage	TTL interface[2]	V_{OH}	2.4	—	V	I_{OH} = −200 μA
	CMOS interface[2]		V_{CC} − 0.8	—		I_{OH} = −200 μA
Output low voltage	TTL interface[2]	V_{OL}	—	0.4	V	I_{OL} = 1.6 mA
	CMOS interface[2]		—	0.8		I_{OL} = 200 μA
Input leakage current	All inputs except I/O common pins[3]	I_{IL}	−2.5	2.5	μA	
Three state (off-state) leakage current	I/O common pins[3]	I_{TSL}	−10.0	10.0	μA	
Current consumption	—	I_{CC}	—	250	mA	f_{DOTCLK} = 25 MHz Output pins left disconnected

Notes: 1. TTL interface inputs: R, G, B, HSYNC, VSYNC, DISPTMG, RD0-RD7, GD0-GD7, BD0-BD7, D0-D3, A0/$\overline{RD}$/XDOT, $\overline{RS}$/ADJ, $\overline{CS}$/MS0
CMOS interface inputs: DM0-DM3, DOTE, PMOD0, PMOD1, A1/YL0-A2/YL2
2. TTL interface outputs: A0/$\overline{RD}$/XDOT, A1/YL0-A3/YL2, D0-D3, RD0-RD7, GD0-GD7, BD0-BD7, MA0-MA15, $\overline{MCS0}$, $\overline{MCS1}$, $\overline{MWE}$
CMOS interface outputs: $\overline{CU}$, $\overline{CD}$, R0/LU0-R3/LU3, G0/LD0-G3/LD3, B0-B3, M, FLM, CL1, CL2, CL3, CL4
3. I/O common pins: A0/$\overline{RD}$/XDOT, A1/YL0-A3/YL2, D0-D3, RD0-RD7, GD0-GD7, BD0-BD7
Inputs except I/O common pins: HSYNC, VSYNC, PMOD0, PMOD1, RS/ADJ, $\overline{CS}$/MS0, $\overline{WR}$/MS1, $\overline{RES}$, DOTE, DM0-DM3, LDOTCK, DOTCLK, R, G, B, DISPTMG
4. TTL interface: $\overline{WR}$/MS1, LDOTCK, DOTCLK
5. TTL interface: $\overline{WR}$/MS1

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DC Characteristics 2 (V_{CC} = 5.0 V ± 5 %, GND = 0 V, Ta = − 20°C to + 75°C, unless otherwise noted)

Item		Symbol	Min	Max	Unit	Test Conditions
Input high voltage	$\overline{RES}$	V_{IH}	V_{CC} − 0.5	V_{CC} + 0.3	V	
	TTL interface[1], $\overline{RES}$		2.0	V_{CC} + 0.3		
	CMOS interface[1]		0.7 V_{CC}	V_{CC} + 0.3		
Input low voltage	TTL interface[1]	V_{IL}	−0.3	0.8	V	
	CMOS interface[1]		−0.3	0.3 V_{CC}		
Output high voltage	TTL interface[2]	V_{OH}	2.4	—	V	I_{OH} = −200 μA
	CMOS interface[2]		V_{CC} − 0.8	—		I_{OH} = −200 μA
Output low voltage	TTL interface[2]	V_{OL}	—	0.4	V	I_{OL} = 1.6 mA
	CMOS interface[2]		—	0.8		I_{OL} = 200 μA
Input leakage current	All inputs except I/O common pins[3]	I_{IL}	−2.5	2.5	μA	
Three state (off-state) leakage current	I/O common pins[3]	I_{TSL}	−10.0	10.0	μA	
Current consumption	—	I_{CC}	—	250	mA	f_{DOTCLK} = 30 MHz Output pins left disconnected

Notes: 1. TTL interface inputs: R, G, B, HSYNC, VSYNC, DISPTMG, DOTCLK, LDOTCK, RD0-RD7, GD0-GD7, BD0-BD7, D0-D3, A0/$\overline{RD}$/XDOT, $\overline{RS}$/ADJ, $\overline{CS}$/MS0, $\overline{WR}$/MS1
CMOS interface inputs: DM0-DM3, DOTE, PMOD0, PMOD1, A1/YL0-A2/YL2

2. TTL interface outputs: A0/$\overline{RD}$/XDOT, A1/YL0-A3/YL2, D0-D3, RD0-RD7, GD0-GD7, BD0-BD7, MA0-MA15, $\overline{MCS0}$, $\overline{MCS1}$, $\overline{MWE}$
CMOS interface outputs: $\overline{CU}$, $\overline{CD}$, R0/LU0-R3/LU3, G0/LD0-G3/LD3, B0-B3, M, FLM, CL1, CL2, CL3, CL4

3. I/O common pins: A0/$\overline{RD}$/XDOT, A1/YL0-A3/YL2, D0-D3, RD0-RD7, GD0-GD7, BD0-BD7
Inputs except I/O common pins: HSYNC, VSYNC, PMOD0, PMOD1, RS/ADJ, $\overline{CS}$/MS0, $\overline{WR}$/MS1, $\overline{RES}$, DOTE, DM0-DM3, LDOTCK, DOTCLK, R, G, B, DISPTMG

Video Signal Interface

Item	Symbol	Min	Max	Unit	Remark
DOTCLK cycle time	t_{CYCD}	40	1000	ns	
DOTCLK high-level pulse width	t_{WDH}	20	—	ns	
DOTCLK low-level pulse width	t_{WDL}	20	—	ns	
DOTCLK rise time	t_{Dr1}	—	5	ns	
DOTCLK fall time	t_{Df1}	—	5	ns	
R, G, B, setup time	t_{VDS}	10	—	ns	
R, G, B, hold time	t_{VDH}	10	—	ns	
DISPTMG setup time	t_{DTS}	10	—	ns	
DISPTMG hold time	t_{DTH}	10	—	ns	
HSYNC setup time	t_{HSS}	10	—	ns	
HSYNC hold time	t_{HSH}	10	—	ns	
Phase shift setup time	t_{PDS}	2 t_{CYCD}	—	ns	
Phase shift hold time	t_{PDH}	2 t_{CYCD}	—	ns	
Input signal rise time	t_{Dr2}	—	10	ns	Except DOTCLK
Input signal fall time	t_{Df2}	—	10	ns	Except DOTCLK

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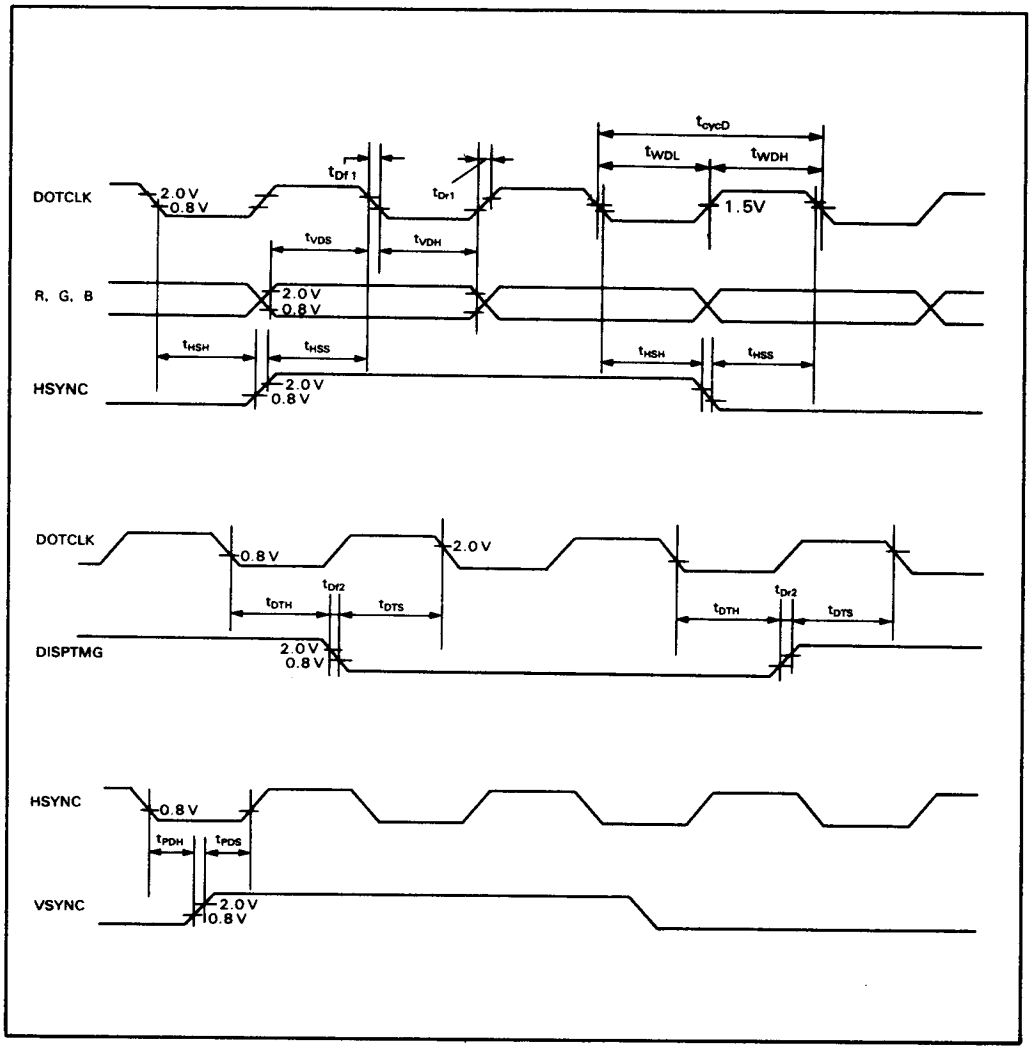

Figure 29 Video Signal Interface

Buffer Memory Interface

Item	Symbol	Min	Max	Unit
Read cycle time	t_{RC}	5 t_{CYCD} – 50	—	ns
RD0-RD7, GD0-GD7, BD0-BD7 data setup time	t_{SMD}	25	—	ns
RD0-RD7, GD0-GD7, BD0-BD7 data hold time	t_{HMD}	0	—	ns
Write cycle time	t_{WC}	6 t_{CYCD} – 50	—	ns
Address setup time	t_{AS}	t_{CYCD} – 30	—	ns
Address hold time	t_{WR}	t_{CYCD} – 30	—	ns
Chip select time	t_{CW}	4 t_{CYCD} – 40	—	ns
Write pulse width	t_{WP}	4 t_{CYCD} – 40	—	ns
RD0-RD7, GD0-GD7, BD0-BD7 output setup time	T_{SMDW}	2 t_{CYCD} – 25	—	ns
RD0-RD7, GD0-GD7, BD0-BD7 output hold time	t_{HMDW}	0	—	ns

Note: t_{CYCD} indicates DOTCLK cycle time (min 40 ns, max 1000 ns).

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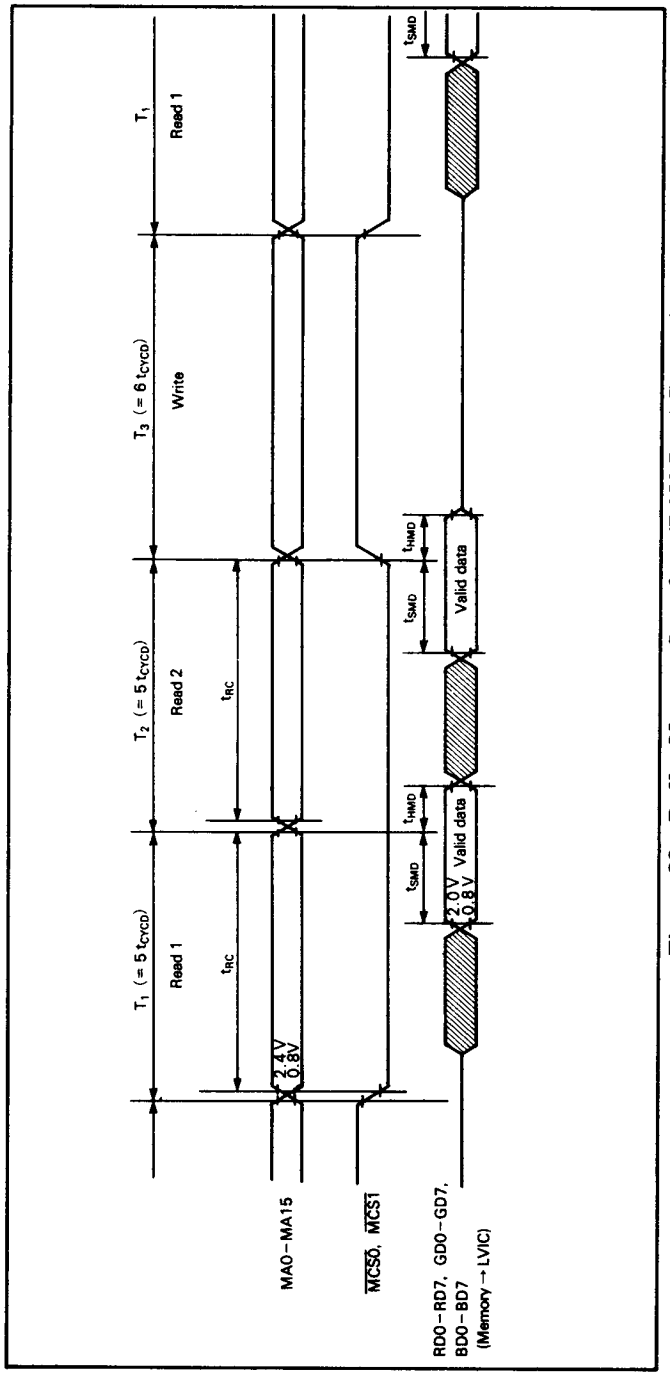

Figure 30 Buffer Memory Interface (RAM Read Timing)

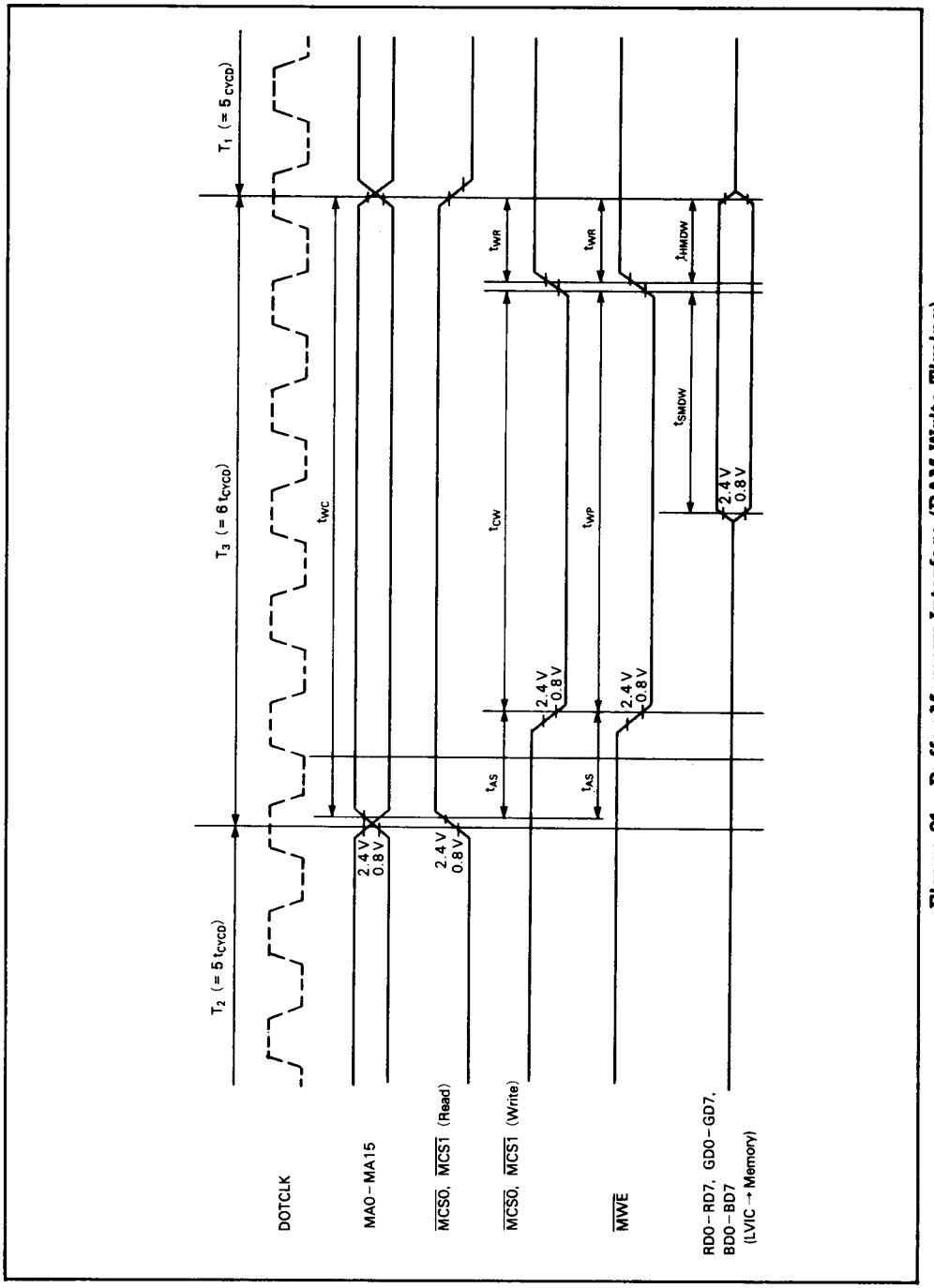

Figure 31 Buffer Memory Interface (RAM Write Timing)

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LCD Driver Interface (TN-Type LCD Driver)

Item	Symbol	Min	Max	Unit
CL2 cycle time	t_{WCL2}	166	—	ns
CL2 high-level pulse width	t_{WCL2H}	50	—	ns
CL2 low-level pulse width	t_{WCL2L}	50	—	ns
CL2 rise time	t_{CL2r}	—	30	ns
CL2 fall time	t_{CL2f}	—	30	ns
CL1 high-level pulse width	t_{WCL1H}	200	—	ns
CL1 rise time	t_{CL1r}	—	30	ns
CL1 fall time	t_{CL1f}	—	30	ns
CL1 setup time	t_{SCL1}	500	—	ns
CL1 hold time	t_{HCL1}	200	—	ns
FLM hold time	t_{HF}	200	—	ns
M output delay time	t_{DM}	—	300	ns
Data delay time	t_{DD}	− 20	20	ns
LDOTCK cycle time	t_{WLDOT}	41	—	ns

Note: All the values are measured at f_{CL2} = 6 MHz.

LCD Driver Interface (TFT-Type LCD Driver)

Item	Symbol	Min	Max	Unit	Remark
CL2 cycle time (X drivers on one side)	t_{TCL2S}	160	—	ns	Figure 34, 35
CL2 high-level width (X drivers on one side)	t_{TCL2HS}	30	—	ns	
CL2 low-level width (X drivers on one side)	t_{TCL2LS}	30	—	ns	
CL2 cycle time (X drivers on both side)	t_{TCL2D}	320	—	ns	
CL2 high-level width (X drivers on both side)	t_{TCL2HD}	80	—	ns	
CL2 low-level width (X drivers on both side)	t_{TCL2LD}	80	—	ns	
CL2 rise time	t_{CL2r}	—	30	ns	
CL2 fall time	t_{CL2f}	—	30	ns	
CL1 high-level width	t_{TCL1H}	200	—	ns	
CL1 rise time	t_{CL1r}	—	30	ns	
CL1 fall time	t_{CL1f}	—	30	ns	
Data delay time	t_{DD1}	−20	20	ns	
Data set up time	t_{LDS}	15	—	ns	
Data hold time	t_{LDH}	15	—	ns	
CL1 setup time	t_{TSCL1}	500	—	ns	
CL1 hold time	t_{THCL1}	200	—	ns	
CL3 delay time	t_{DCL3}	50	—	ns	
M delay time	t_{DM}	—	300	ns	
FLM hold time	t_{TFH}	200	—	ns	
LDOTCK cycle time	t_{WLDOT}	40	—	ns	

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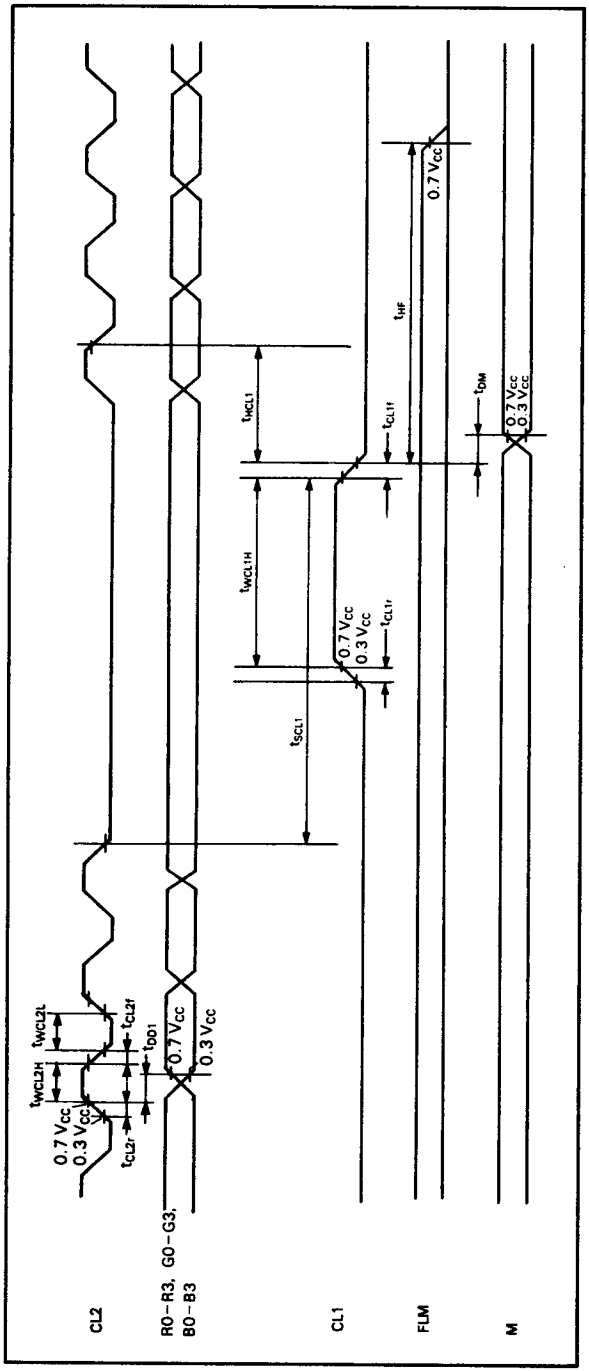

Figure 32 LCD Driver Interface (TN-Type LCD Driver Interface)

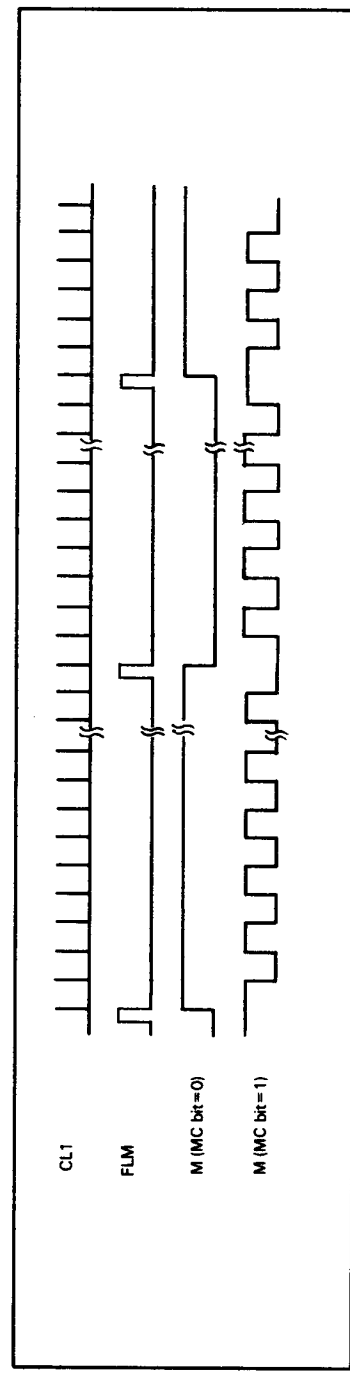

Figure 33 CL1, FLM and M (Reduced View of Figure 32)

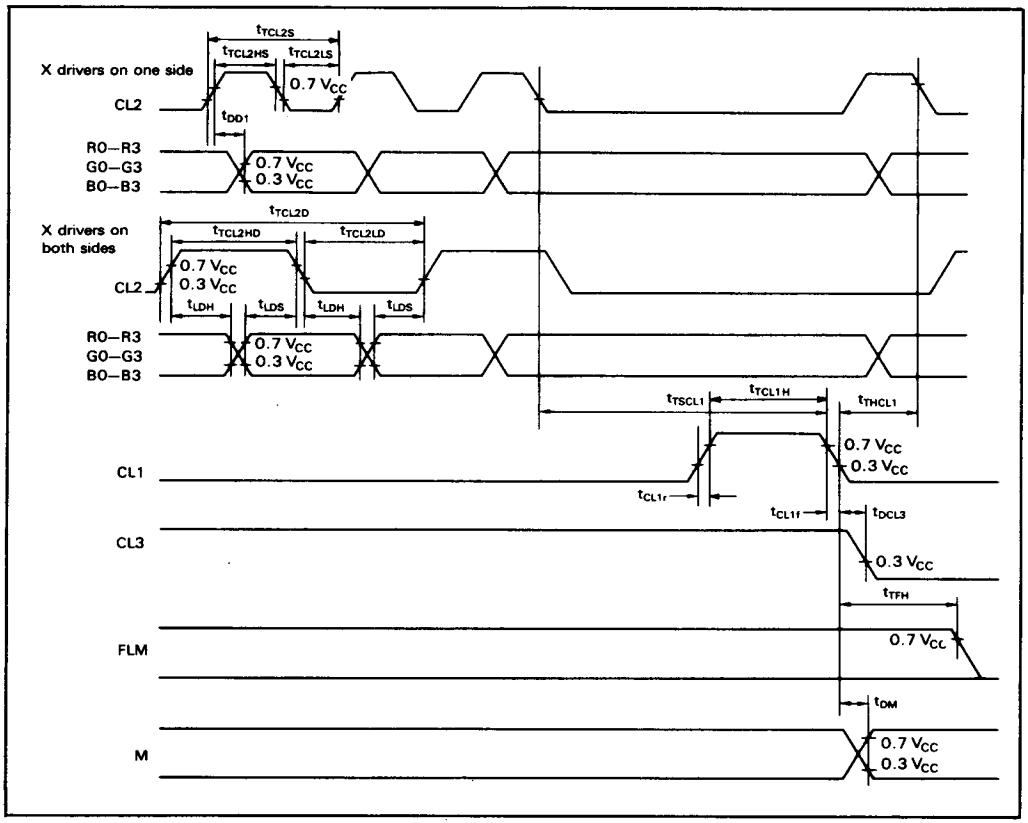

Figure 34 LCD Driver Interface (TFT-type LCD Driver Interface)

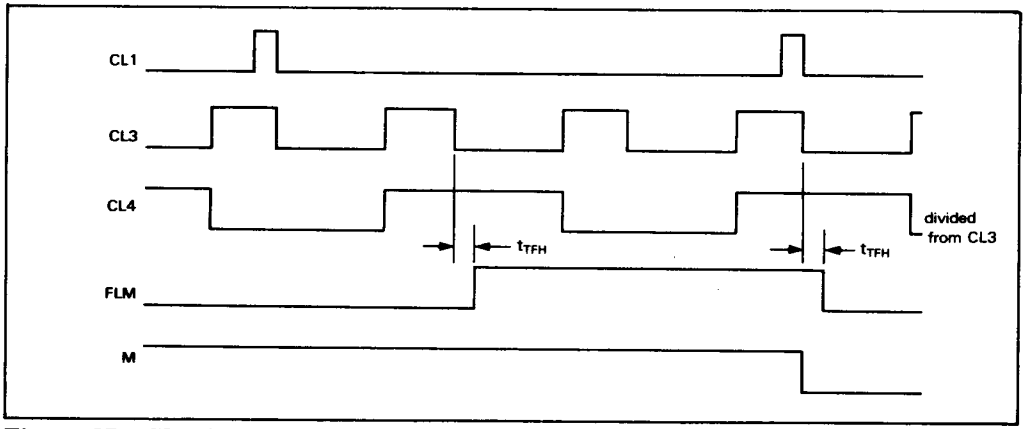

Figure 35 CL1, CL3, CL4, FLM, M (Reduced view of figure 34 in the horizontal stripe mode)

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Register Programming, MPU Write

Item	Symbol	Min	Max	Unit
$\overline{RD}$ high-level pulse width	t_{WRDH}	190	—	ns
$\overline{RD}$ low-level pulse width	t_{WRDL}	190	—	ns
$\overline{WE}$ high-level pulse width	t_{WWEH}	190	—	ns
$\overline{WE}$ low-level pulse width	t_{WWEL}	190	—	ns
$\overline{CS}$, RS setup time	t_{AS}	0	—	ns
$\overline{CS}$, RS hold time	t_{AH}	0	—	ns
D0-D3 setup time	t_{DSW}	100	—	ns
D0-D3 hold time	t_{DHW}	0	—	ns
D0-D3 output delay time	t_{DDR}	—	150	ns
D0-D3 output hold time	t_{DHR}	10	—	ns

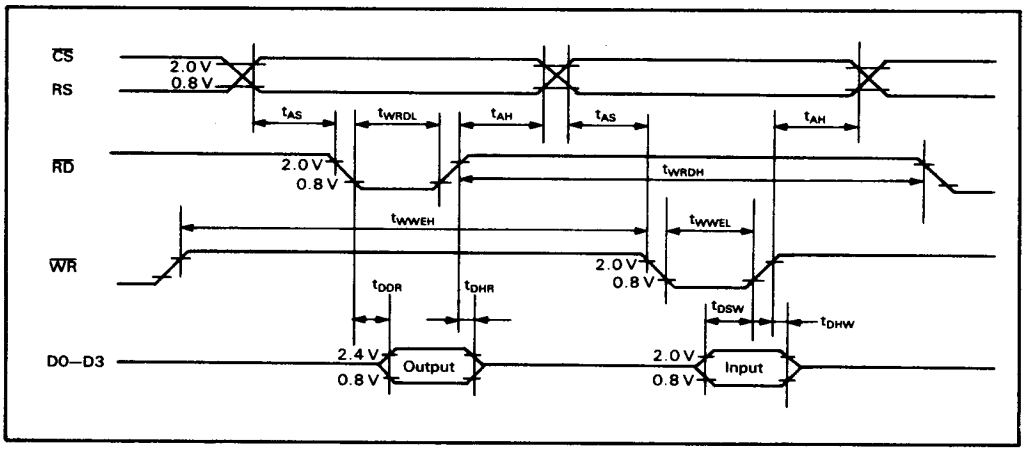

Figure 36 MPU Interface

Register Programming, ROM Write

Item	Symbol	Min	Max	Unit
A cycle time	t_{CYCA}	528	—	ns
A rise time	t_{Ar}	—	100	ns
A fall time	t_{Af}	—	100	ns
D ROM data setup time	t_{DSWD}	120	—	ns
D ROM data hold time	t_{DHWD}	0	—	ns

Note: $t_{CYCA} = 16\ t_{CYCD}$

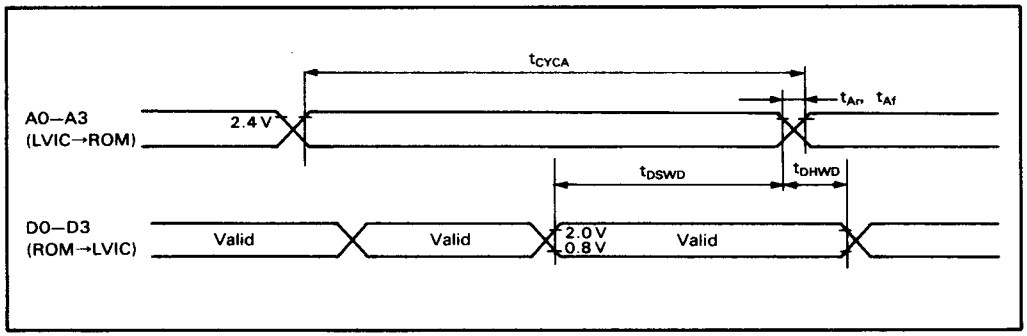

Figure 37 ROM Interface

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PLL Interface

Item	Symbol	Min	Max	Unit
$\overline{CU}$ fall delay time	t_{Uf}	—	80	ns
$\overline{CU}$ rise delay time	t_{Ur}	—	80	ns
$\overline{CD}$ fall delay time	t_{Df}	—	80	ns
$\overline{CD}$ rise delay time	t_{Dr}	—	80	ns

Reset Input

Item	Symbol	Min	Max	Unit
$\overline{RES}$ input pulse width	$t_{\overline{RES}}$	1	—	μs

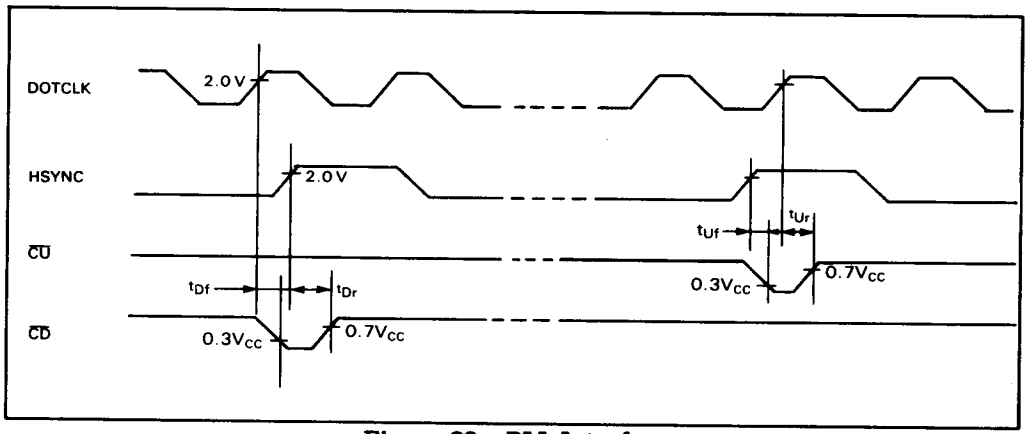

Figure 38 PLL Interface

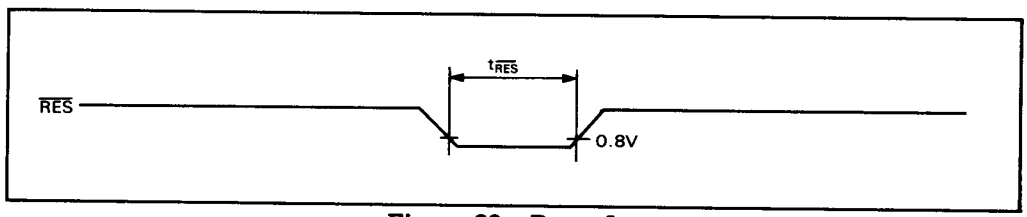

Figure 39 Reset Input

Load Circuits

TTL Load

Pin	R_L	R	C_L	Remarks
MA0-MA15, $\overline{MWE}$, $\overline{MCS0}$,$\overline{MCS1}$, RD0-RD7, GD0-GD7, BD0-BD7	2.4 kΩ	11 kΩ	40 pF	tr, tf: Not specified
A0/RD/XDOT, A1/YL0-A3/YL2	2.4 kΩ	11 kΩ	40 pF	tr, tf: Specified

Capacitive Load

Pin	C	Remarks
CL1, CL2, CL3, CL4	40 pF	tr, tf: Specified
R0-R3, G0-G3, B0-B3, FLM $\overline{CU}$, $\overline{CD}$, M	40 pF	tr, tf: Not specified

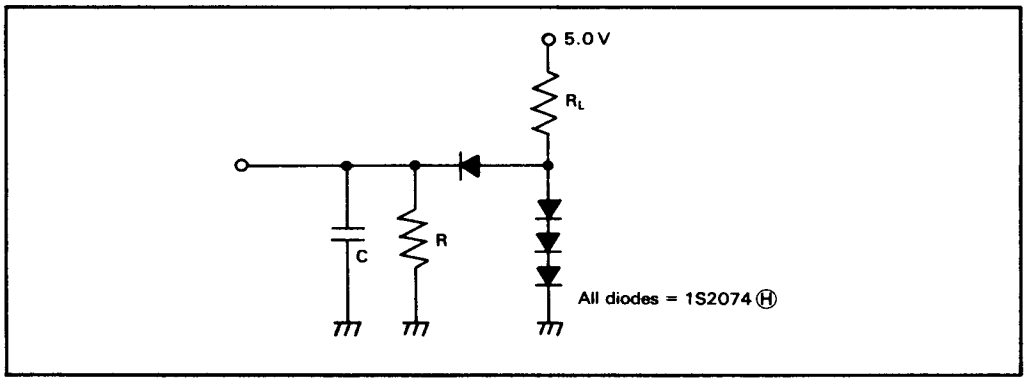

Figure 40 TTL Load Circuit

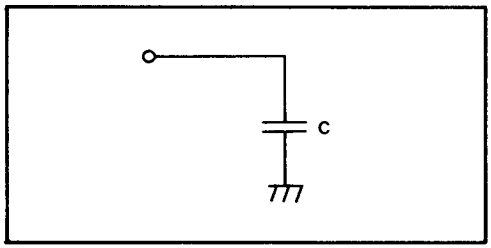

Figure 41 Capacitive Load Circuit

Refer to application note (No. ADE-502-011) for detail of this product.