

# MC100EPT24

## 3.3V LVTTTL/LVCMOS to Differential LVECL Translator

The MC100EPT24 is a LVTTTL/LVCMOS to differential LVECL translator. Because LVECL levels and LVTTTL/LVCMOS levels are used, a  $-3.3\text{ V}$ ,  $+3.3\text{ V}$  and ground are required. The small outline 8-lead package and the single gate of the EPT24 makes it ideal for those applications where space, performance, and low power are at a premium.

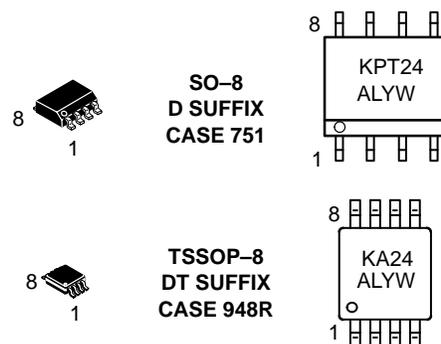
- 350 ps Typical Propagation Delay
- Maximum Frequency > 1.0 GHz Typical
- The 100 Series Contains Temperature Compensation
- Operating Range:  $V_{CC} = 3.0\text{ V}$  to  $3.6\text{ V}$ ;  
 $V_{EE} = -3.6\text{ V}$  to  $-3.0\text{ V}$ ;  $GND = 0\text{ V}$
- PNP LVTTTL Inputs for Minimal Loading
- Q Output Will Default HIGH with Input Open



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### MARKING DIAGRAMS\*



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week

\*For additional information, see Application Note AND8002/D

### ORDERING INFORMATION

Device	Package	Shipping
MC100EPT24D	SO-8	98 Units / Rail
MC100EPT24DR2	SO-8	2500 Tape & Reel
MC100EPT24DT	TSSOP-8	100 Units / Rail
MC100EPT24DTR2	TSSOP-8	2500 Tape & Reel

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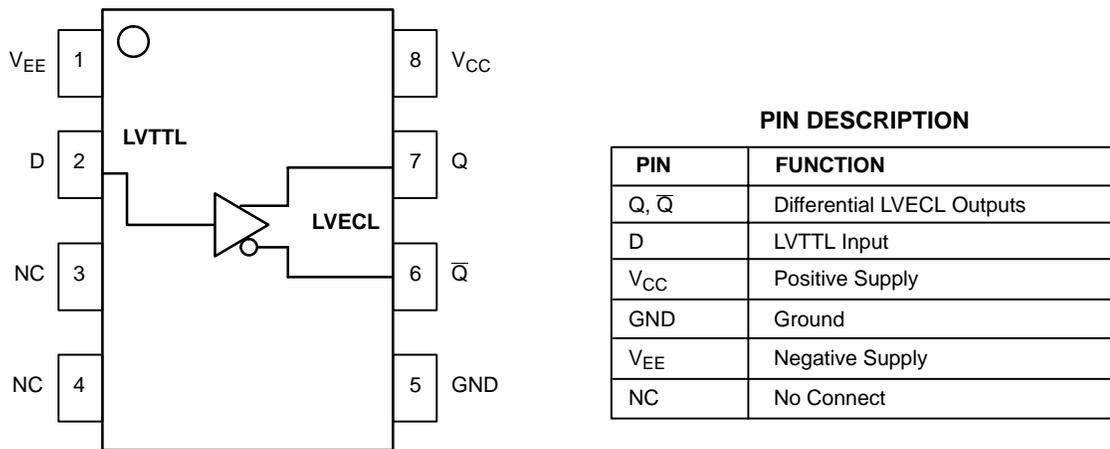


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

## ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	N/A
Internal Input Pullup Resistor	N/A
ESD Protection	Human Body Model Machine Model Charged Device Model
	> 4 kV > 200 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1.)	Level 1
Flammability Rating Oxygen Index	UL-94 code V-0 A 1/8" 28 to 34
Transistor Count	181 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

## MAXIMUM RATINGS (Note 2.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V <sub>CC</sub>	Positive Power Supply	GND = 0 V	V <sub>EE</sub> = -3.3 V	3.8	V
V <sub>EE</sub>	Negative Power Supply	GND = 0 V	V <sub>CC</sub> = +3.3 V	-3.8	V
V <sub>IN</sub>	Input Voltage	GND = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub>	0 to V <sub>CC</sub>	V
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44	°C/W
T <sub>sol</sub>	Wave Solder	<2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

# MC100EPT24

## LVTTL INPUT DC CHARACTERISTICS $V_{CC}= 3.3\text{ V}$ , $V_{EE}= -3.6\text{ V}$ to $-3.0\text{ V}$ , $GND= 0.0\text{ V}$ ; $T_A= -40^\circ\text{C}$ to $85^\circ\text{C}$

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
$I_{IH}$	Input HIGH Current	$V_{IN} = 2.7\text{ V}$			20	$\mu\text{A}$
$I_{IHH}$	Input HIGH Current	$V_{IN} = 6.0\text{ V}$			100	$\mu\text{A}$
$I_{IL}$	Input LOW Current	$V_{IN} = 0.5\text{ V}$			-0.6	$\text{mA}$
$V_{IK}$	Input Clamp Diode Voltage	$I_{IN} = -18\text{ mA}$			-1.2	$\text{V}$
$V_{IH}$	Input HIGH Voltage		2.0			$\text{V}$
$V_{IL}$	Input LOW Voltage				0.8	$\text{V}$

## NECL OUTPUT DC CHARACTERISTICS $V_{CC}= 3.3\text{ V}$ , $V_{EE}= -3.3\text{ V}$ , $GND= 0.0\text{ V}$ (Note 3.)

Symbol	Characteristic	$-40^\circ\text{C}$			$25^\circ\text{C}$			$85^\circ\text{C}$			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{OH}$	Output HIGH Voltage (Note 4.)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1030	-895	$\text{mV}$
$V_{OL}$	Output LOW Voltage (Note 4.)	-1945	-1820	-1695	-1945	-1820	-1695	-1945	-1820	-1695	$\text{mV}$
$I_{CC}$	Power Supply Current		2.0	4.0		2.0	4.0		2.0	4.0	$\text{mA}$
$I_{EE}$	Power Supply Current	20	30	38	20	30	38	20	30	38	$\text{mA}$

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lpm is maintained.

3. Output levels will vary 1:1 with GND.  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .

4. Outputs are terminated through a 50 ohm resistor to GND-2 volts.

## AC CHARACTERISTICS $V_{CC}= 3.0\text{ V}$ to $3.6\text{ V}$ , $V_{EE}= -3.6\text{ V}$ to $-3.0\text{ V}$ , $GND= 0.0\text{ V}$ (Note 5.)

Symbol	Characteristic	$-40^\circ\text{C}$			$25^\circ\text{C}$			$85^\circ\text{C}$			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Frequency (See Figure 2. $F_{max}/\text{JITTER}$ )		> 1			> 1			> 1		$\text{GHz}$
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Output Differential (Note 6.)	300	500	800	300	530	800	300	560	800	$\text{ps}$
$t_{\text{JITTER}}$	Cycle-to-Cycle Jitter (See Figure 2. $F_{max}/\text{JITTER}$ )		0.2	< 1		0.2	< 1		0.2	< 1	$\text{ps}$
$t_r$ , $t_f$	Output Rise/Fall Times (20% – 80%)	70	125	170	80	130	180	100	150	200	$\text{ps}$

5. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 ohms to  $V_{CC}-2.0\text{ V}$ .

6. Specifications for standard TTL input signal.

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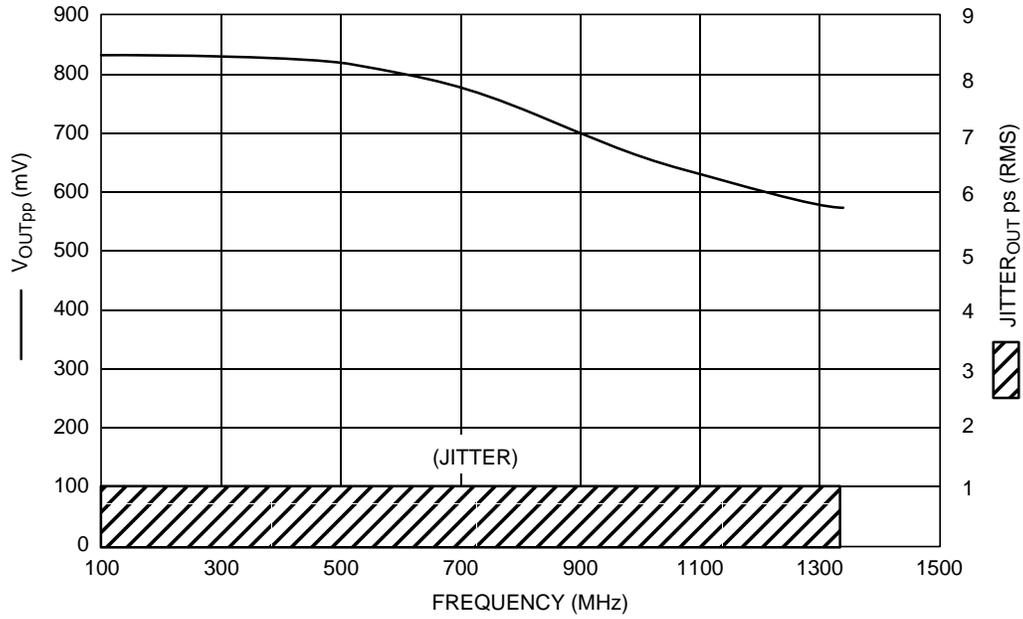


Figure 2. F<sub>max</sub>/Jitter

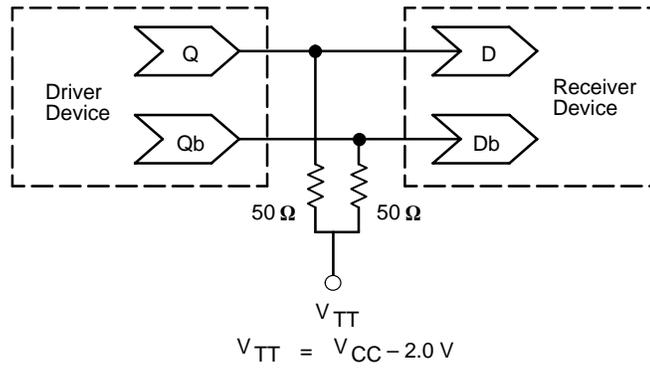


Figure 3. Typical Termination for Output Driver and Device Evaluation  
(See Application Note AND8020 – Termination of ECL Logic Devices.)

## Resource Reference of Application Notes

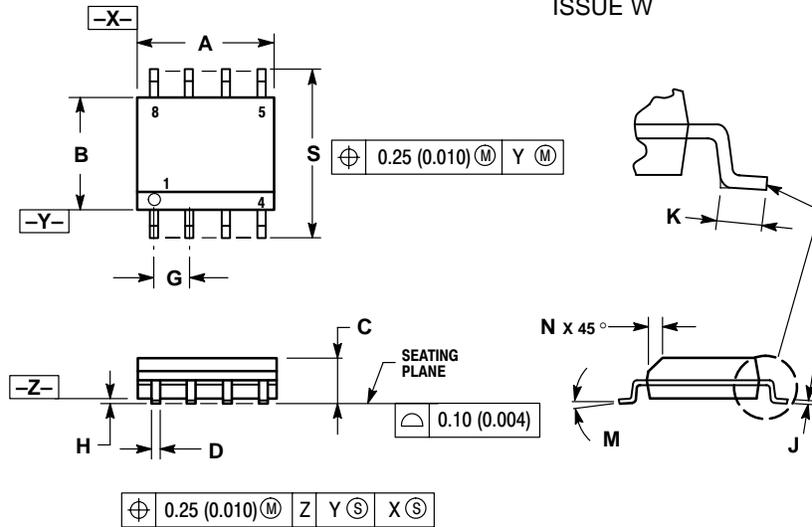
- AN1404** – ECLinPS Circuit Performance at Non-Standard  $V_{IH}$  Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1560** – Low Voltage ECLinPS SPICE Modeling Kit
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

For an updated list of Application Notes, please see our website at <http://onsemi.com>.

# MC100EPT24

## PACKAGE DIMENSIONS

### SO-8 D SUFFIX PLASTIC SOIC PACKAGE CASE 751-07 ISSUE W

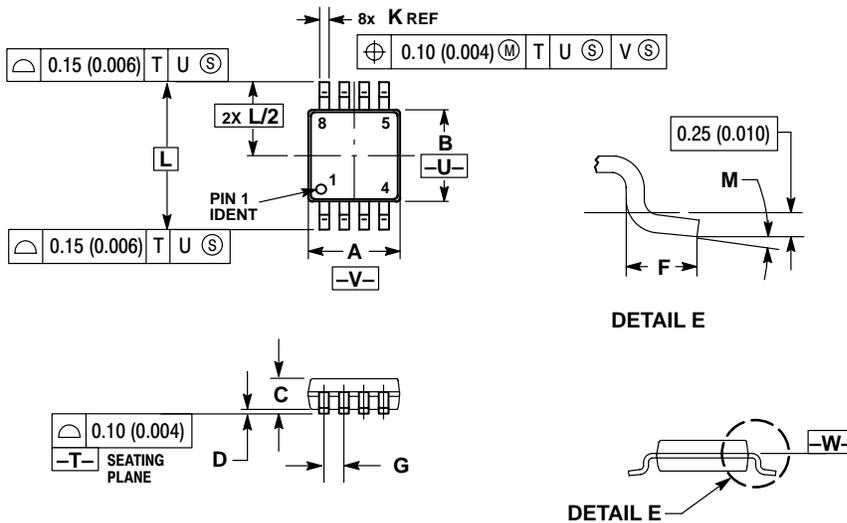


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### TSSOP-8 DT SUFFIX PLASTIC TSSOP PACKAGE CASE 948R-02 ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

**Notes**

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