

NTD20N03L27

Power MOSFET 20 Amps, 30 Volts N-Channel DPAK

This logic level vertical power MOSFET is a general purpose part that provides the “best of design” available today in a low cost power package. Avalanche energy issues make this part an ideal design in. The drain-to-source diode has a ideal fast but soft recovery.

Features

- Ultra-Low $R_{DS(on)}$, single base, advanced technology
- SPICE parameters available
- Diode is characterized for use in bridge circuits
- I_{DSS} and $V_{DS(on)}$ specified at elevated temperatures
- High Avalanche Energy Specified
- ESD JEDAC rated HBM Class 1, MM Class A, CDM Class 0

Typical Applications

- Power Supplies
- Inductive Loads
- PWM Motor Controls
- Replaces MTD20N03L in many applications

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	30	Vdc
Drain-to-Gate Voltage ($R_{GS} = 1.0\text{ M}\Omega$)	V_{DGR}	30	Vdc
Gate-to-Source Voltage	V_{GS}	± 20	Vdc
– Continuous	V_{GS}	± 24	
– Non-Repetitive ($t_p \leq 10\text{ ms}$)			
Drain Current	I_D	20	Adc
– Continuous @ $T_A = 25^\circ\text{C}$	I_D	16	
– Continuous @ $T_A = 100^\circ\text{C}$	I_{DM}	60	Apk
– Single Pulse ($t_p \leq 10\text{ }\mu\text{s}$)			
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	74	Watts
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ (Note 1.)		0.6	$\text{W}/^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 30\text{ Vdc}$, $V_{GS} = 5\text{ Vdc}$, $L = 1.0\text{ mH}$, $I_{L(pk)} = 24\text{ A}$, $V_{DS} = 34\text{ Vdc}$)	E_{AS}	288	mJ
Thermal Resistance			$^\circ\text{C}/\text{W}$
– Junction-to-Case	$R_{\theta JC}$	1.67	
– Junction-to-Ambient	$R_{\theta JA}$	100	
– Junction-to-Ambient (Note 1.)	$R_{\theta JA}$	71.4	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	$^\circ\text{C}$

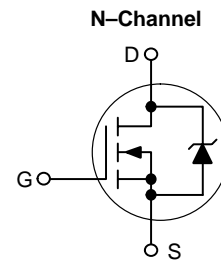
1. When surface mounted to an FR4 board using the minimum recommended pad size and repetitive rating; pulse width limited by maximum junction temperature.



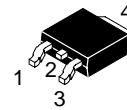
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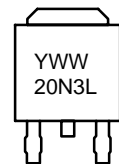
20 AMPERES
30 VOLTS
 $R_{DS(on)} = 27\text{ m}\Omega$



MARKING DIAGRAM

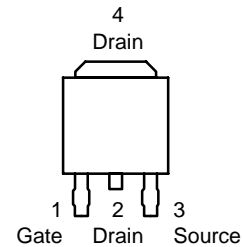


CASE 369A
DPAK
STYLE 2



20N3L = Device Code
Y = Year
WW = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
NTD20N03L27	DPAK	75 Units/Rail
NTD20N03L27-1	DPAK	75 Units/Rail
NTD20N03L27T4	DPAK	2500 Tape & Reel

NTD20N03L27

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-to-Source Breakdown Voltage (Note 2.) (V _{GS} = 0 Vdc, I _D = 250 μAdc) Temperature Coefficient (Positive)	V _{(BR)DSS}	30 –	– 43	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 30 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 30 Vdc, V _{GS} = 0 Vdc, T _J = 150°C)	I _{DSS}	– –	– –	10 100	μAdc
Gate-Body Leakage Current (V _{GS} = ±20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	–	–	±100	nAdc

ON CHARACTERISTICS (Note 2.)

Gate Threshold Voltage (Note 2.) (V _{DS} = V _{GS} , I _D = 250 μAdc) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	1.0 –	1.6 5.0	2.0 –	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 2.) (V _{GS} = 4.0 Vdc, I _D = 10 Adc) (V _{GS} = 5.0 Vdc, I _D = 10 Adc)	R _{DS(on)}	– –	28 23	31 27	mΩ
Static Drain-to-Source On-Resistance (Note 2.) (V _{GS} = 5.0 Vdc, I _D = 20 Adc) (V _{GS} = 5.0 Vdc, I _D = 10 Adc, T _J = 150°C)	V _{DS(on)}	– –	0.48 0.40	0.54 –	Vdc
Forward Transconductance (Note 2.) (V _{DS} = 5.0 Vdc, I _D = 10 Adc)	g _{FS}	–	21	–	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 25 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	–	1005	1260	pF
Output Capacitance		C _{oss}	–	271	420	
Transfer Capacitance		C _{rss}	–	87	112	

SWITCHING CHARACTERISTICS (Note 3.)

Turn-On Delay Time	(V _{DD} = 20 Vdc, I _D = 20 Adc, V _{GS} = 5.0 Vdc, R _G = 9.1 Ω) (Note 2.)	t _{d(on)}	–	17	25	ns
Rise Time		t _r	–	137	160	
Turn-Off Delay Time		t _{d(off)}	–	38	45	
Fall Time		t _f	–	31	40	
Gate Charge	(V _{DS} = 48 Vdc, I _D = 15 Adc, V _{GS} = 10 Vdc) (Note 2.)	Q _T	–	13.8	18.9	nC
		Q ₁	–	2.8	–	
		Q ₂	–	6.6	–	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I _S = 20 Adc, V _{GS} = 0 Vdc) (Note 2.) (I _S = 20 Adc, V _{GS} = 0 Vdc, T _J = 125°C)	V _{SD}	– –	1.0 0.9	1.15 –	Vdc
Reverse Recovery Time	(I _S = 15 Adc, V _{GS} = 0 Vdc, di _S /dt = 100 A/μs) (Note 2.)	t _{rr}	–	23	–	ns
		t _a	–	13	–	
		t _b	–	10	–	
Reverse Recovery Stored Charge		Q _{RR}	–	0.017	–	μC

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

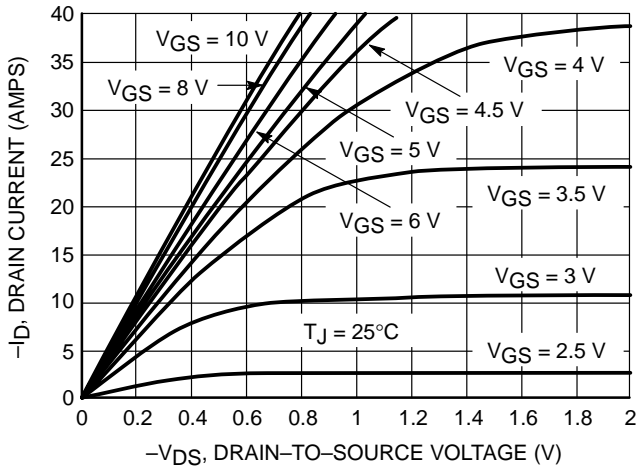


Figure 1. On-Region Characteristics

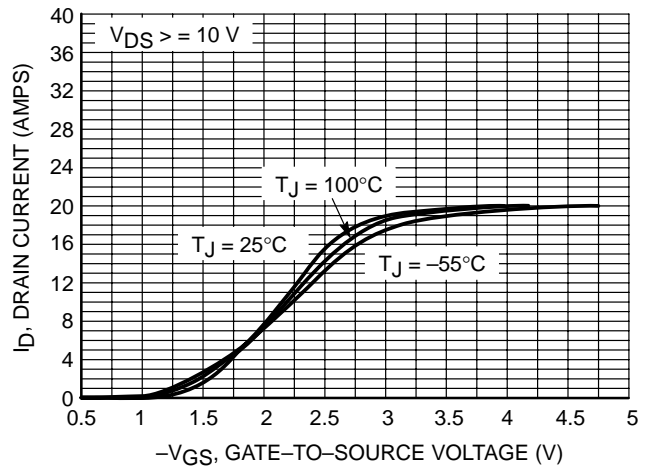


Figure 2. Transfer Characteristics

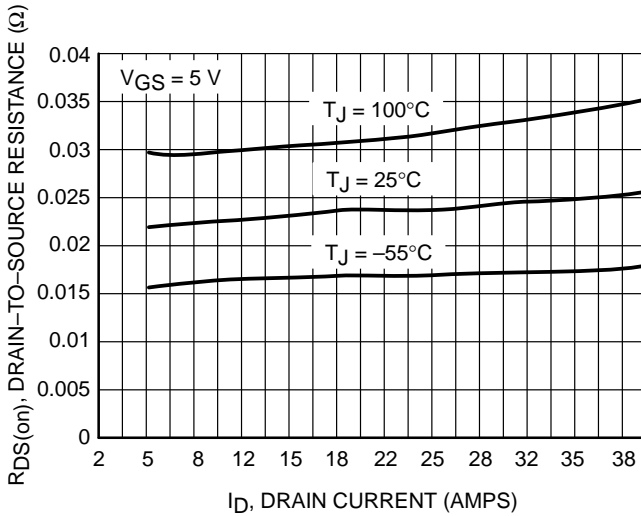


Figure 3. On-Resistance vs. Drain Current and Temperature

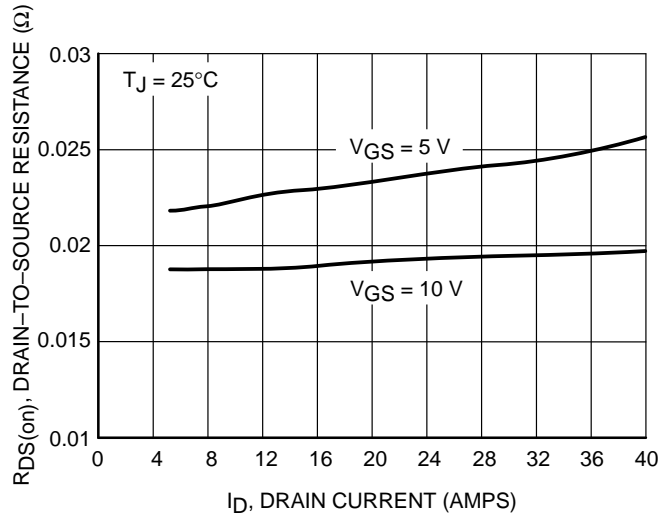


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

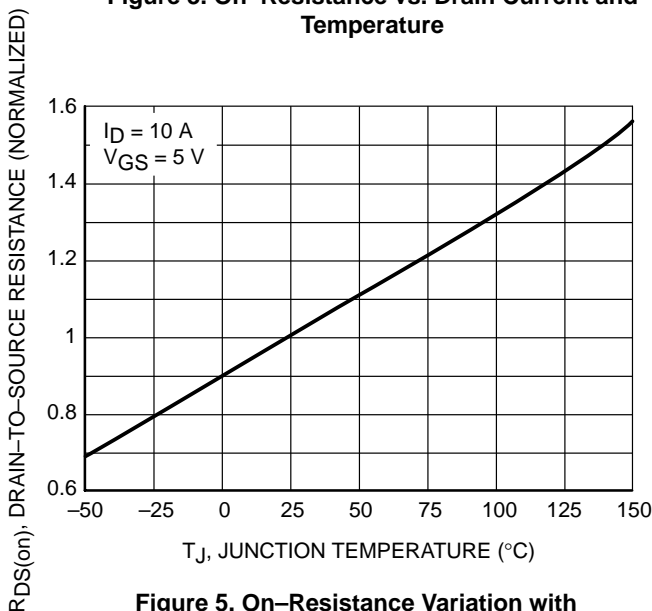


Figure 5. On-Resistance Variation with Temperature

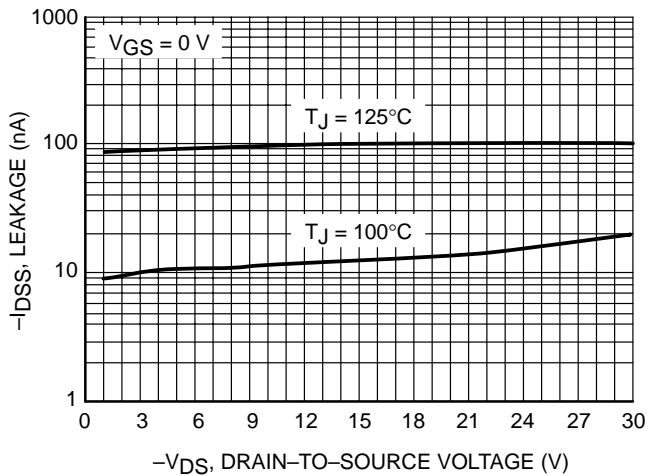


Figure 6. Drain-to-Source Leakage Current vs. Voltage

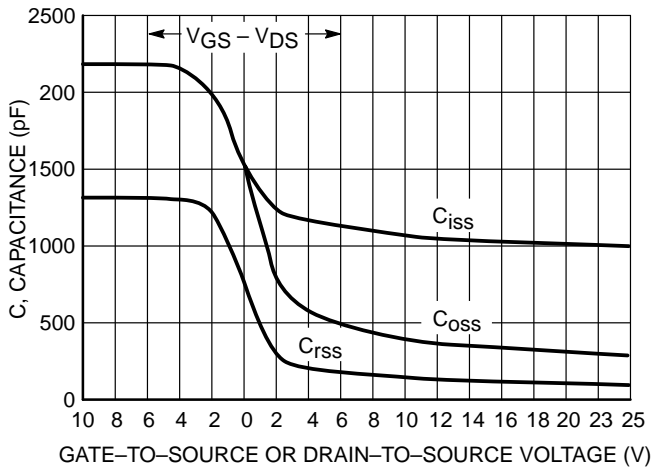


Figure 7. Capacitance Variation

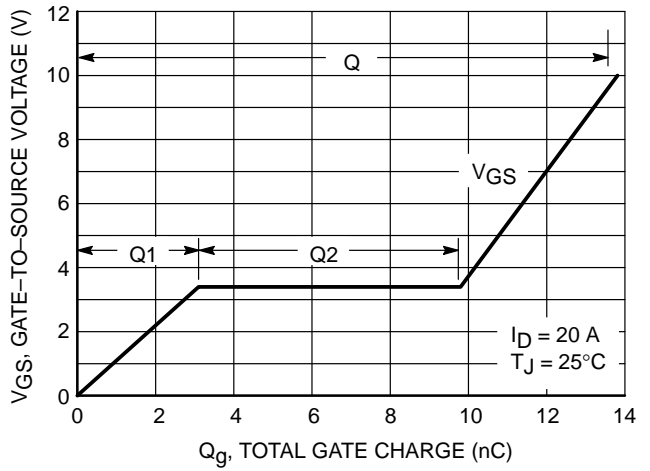


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

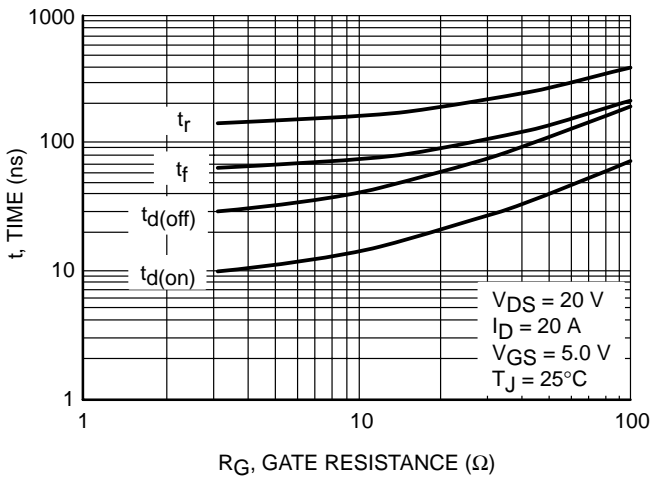


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

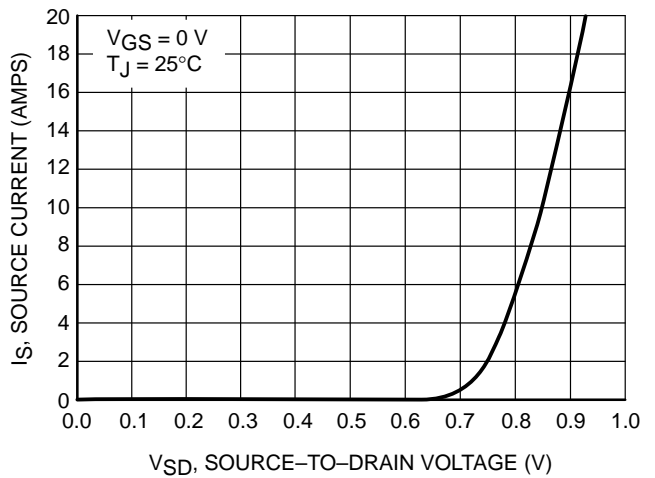


Figure 10. Diode Forward Voltage vs. Current

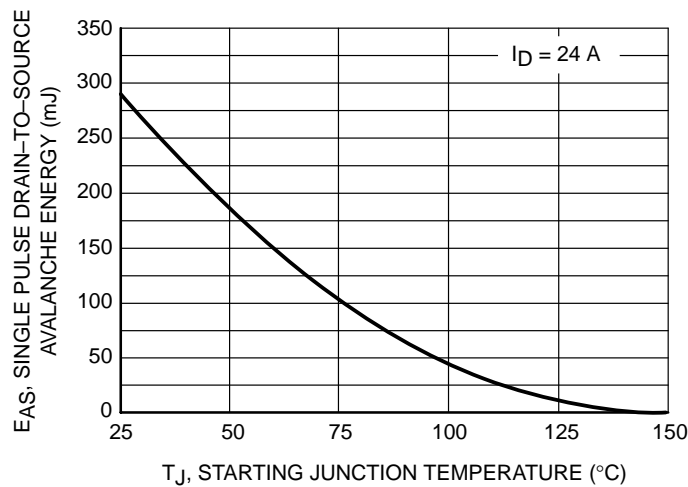
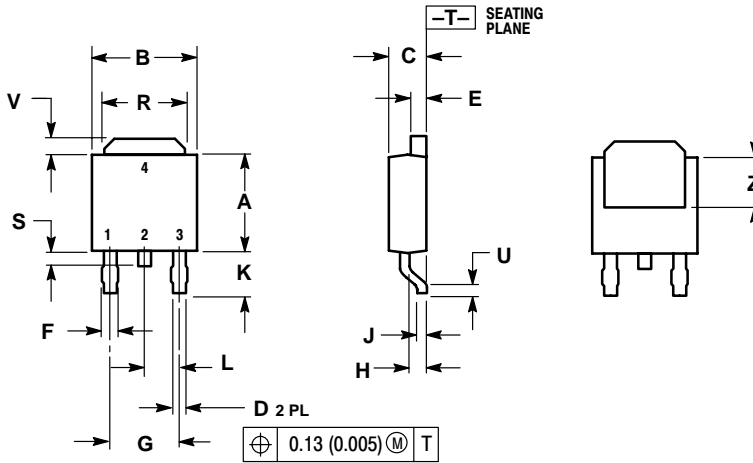


Figure 11. Maximum Avalanche Energy vs. Starting Junction Temperature

NTD20N03L27

PACKAGE DIMENSIONS

DPAK
CASE 369A-13
ISSUE AA



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	----	0.51	----
V	0.030	0.050	0.77	1.27
Z	0.138	----	3.51	----

- STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

Notes

Notes

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