Rockwell

RC288ACL/VFC, RC240ACL/VFC and RC192ACL/VFC Integrated V.Fast Class™(V.FC™) Low Power Data and Fax Modem Device Set Family

INTRODUCTION

The Rockwell V.Fast Class™ (V.FC™) integrated modem device set family supports ultra high speed data and high speed fax operation. Models are provided that meet different requirements for data throughput and options (Table 1). Each model consists of modem data pump and controller devices and supporting firmware.

As a data modem, the modem operates at line speeds to 28800 bps (RC288ACL/VFC), 24000 bps (RC240ACL/VFC), or 19200 bps (RC192ACL/VFC). Error correction (V.42/MNP 2–4) and data compression (V.42 bis/MNP 5) maximize data transfer integrity and boost data throughput up to 115.2 kbps, 96 kbps, or 76.8 kbps. The modem also operates in non-error-correcting mode.

As a fax modem, the modem supports Group 3 send and receive rates up to 14400 bps and supports T.30 protocol. Extended "AT" commands provide data, fax class 1 and class 2, MNP 10, and world-class functions while using minimal external ROM, RAM, and optional NVRAM. Models supporting US/Canada and multiple countries with different memory requirements are available (Table 1).

The modem operates over a dial-up telephone line, can auto-dial and auto-answer, and can operate in both synchronous and asynchronous modes. Configuration information can be stored in non-volatile memory.

A PC-based "ConfigurACE™" utility program can be used to customize the MCU firmware to specific application and country requirements.

The MCU is packaged in an 80-pin plastic quad flat pack (PQFP). The MDP is available in two PQFPs (one 100-pin and one 80-pin) or in a 68-pin plastic leaded chip carrier (PLCC).

With low power consumption and small footprint, low profile PQFP packages meeting PCMCIA Type II envelope requirements, this modem is ideal for PCMCIA PC Cards or inclusion on motherboards for battery-powered portable applications such as notebook computers.

Accelerator kits are available to minimize application design time and costs.

FEATURES

- Data modem throughput up to 115.2 kbps
  - —V.Fast Class (V.FC), V.32 bis, V.32, V.22 bis, V.22A/B, V.23, and V.21; Bell 212A and 103
  - —V.42 LAPM and MNP 2-4 error correction
  - —V.42 bis and MNP 5 data compression
- MNP 10 data throughput enhancement (to V.32 bis)
- Fax modem send and receive rates up to 14400 bps
  - —V.17, V.29, V.27 ter, and V.21 channel 2
- World-class operation (option)
  - —V.25 bis commands (asynchronous only)
  - —Call progress and blacklisting parameters
  - —Multiple country support
- Hayes AutoSync (option)
- ConfigurACE utility program
- Communication software compatible command sets
  - —AT, fax class 1, and fax class 2 commands
  - —S registers
- Built-in DTE interfaces
  - —DTE speed up to 115.2 kbps
  - —Parallel 16550A UART-compatible interface
  - —Serial CCITT V.24 (EIA/TIA-232-E)
- Line quality monitoring and auto retrain
- NVRAM directory and stored profiles
- Flow control and speed buffering
- Automatic format/speed sensing
- Serial synchronous and asynchronous data
- Parallel asynchronous data
- Auto dial and auto answer
- Tone, pulse, and adaptive dialing
- Calling Number Delivery (Caller ID) detect
- Diagnostics
- Extended operating temperature models available
- +5V operation
- Typical power consumption:

Mode	Power
Normal	
RC288ACL/VFC	790 mW
RC240ACL/VFC	710 mW
RC192ACL/VFC	600 mW
Sleep	20.0 mW
Stop	9.8 mW

- CMOS VLSI devices
  - —MCU: One 80-pin PQFP
  - —MDP: Two PQFPs (a 100-pin and an 80-pin) or one 68-pin PLCC

Data Sheet
(Preliminary)

Order No. MD113
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Table 1. Modem Models, Functions, and Memory Requirements

Model[1]	Supported Functions[2]					External ROM (Bytes)
	Fax	MNP10	W-Class	AutoSync	Country	
RC288ACL-D/VFC	–	–	–	–	US/Can	64k
RC288ACL/VFC	S	–	–	–	US/Can	64k
RC288ACL(/A)/VFC	S	S	–	A	US/Can	128k
RC288ACLW-D/VFC	–	S	S	S	Multiple	128k
RC288ACLW(E)/VFC	S	S	S	S	Multiple	128k
RC240ACL-D/VFC	–	–	–	–	US/Can	64k
RC240ACL/VFC	S	–	–	–	US/Can	64k
RC240ACL(/A)/VFC	S	S	–	A	US/Can	128k
RC240ACLW-D/VFC	–	S	S	S	Multiple	128k
RC240ACLW(E)/VFC	S	S	S	S	Multiple	128k
RC192ACL-D/VFC	–	–	–	–	US/Can	64k
RC192ACL/VFC	S	–	–	–	US/Can	64k
RC192ACL(/A)/VFC	S	S	–	A	US/Can	128k
RC192ACLW-D/VFC	–	S	S	S	Multiple	128k
RC192ACLW/VFC	S	S	S	S	Multiple	128k

Notes:

1. Option notations:
   - -D Data only (no fax).
   - W World class support.
   - (/A) Optional AutoSync support.
   - (E) Optional industrial temperature range.
2. Supported functions (A = Optionally supported; S = Supported; – = Not supported):
   - Fax Fax class 1 and class 2 command functions.
   - MNP 10 Data throughput enhancement functions.
   - W-Class World class functions supporting multiple country requirements.
   - AutoSync Hayes AutoSync available with 128k-byte ROM installed.

TECHNICAL OVERVIEW

GENERAL DESCRIPTION

The modem device set provides the processing core of the modem. The OEM adds external memory, crystal, discrete components, and a digital access arrangement (DAA) circuit to complete the modem system.

System Configuration

The modem device set consists of a Microcontroller (MCU) and a Modem Data Pump (MDP).

The OEM provides external memory for the MCU (64k/128k bytes ROM and 32k bytes RAM).

Modem Data Pump (MDP)

The MDP is a Rockwell RC288DPL/VFC, RC240DPL/VFC, or RC192DPL/VFC 2-wire data/fax modem data pump packaged in two PQFPs (a 100-pin PQFP and an 80-pin PQFP) or one 68-pin PLCC.

As a data modem, the MDP can operate in full-duplex, synchronous/asynchronous modes at line rates up to 28800 bps. Using a proprietary scheme to optimize modem configuration for line conditions, the MDP can connect at the highest data rate that the channel can support from 28800 bps (RC288DPL/VFC), 24000 bps (RC240DPL/VFC), or 19200 bps (RC192DPL/VFC) to 14400 bps with automatic fallback. Automode operation in V.32 bis is provided in accordance with EIA/TIA-PN2330.

As a fax modem, the MDP fully supports Group 3 facsimile send and receive speeds of 14400, 12000, 9600, 7200, 4800, and 2400 bps.

Microcontroller (MCU)

The MCU is a Rockwell L39 microcomputer packaged in a 80-pin PQFP.

MCU performs the command processing and host interface functions.

The MCU connects to the host via a V.24 (EIA/TIA-232-E) serial interface or a parallel microcomputer bus. The MCU connects to the MDP via dedicated lines and the external bus. The MCU external bus also connects to OEM-supplied ROM and RAM. The MCU external memory is 64k or 128k bytes ROM (45 ns) and 32k bytes RAM (45 ns). For W-class models, buffered switch inputs and latched indicator/control outputs can optionally be connected to the MCU external bus.

For all models, 256 bytes NVRAM can optionally be connected to the MCU over a dedicated serial interface.

The MCU crystal frequency is 14.7456 MHz.

MCU Firmware

MCU firmware performs processing of general modem control, command sets, error correction, MNP 10, fax class 1 and class 2, and DTE interface functions. The MCU firmware is provided by Rockwell in object code form for the OEM to program into external ROM. The MCU firmware may also be provided in source code form under a source code addendum license agreement.

SUPPORTED INTERFACES

The major hardware signal interfaces of the modem device set are illustrated in Figure 1.

Parallel Host Bus Interface

A 16550A UART-compatible parallel interface is provided.

Eight data lines, three address lines, and nine control lines are supported.

Serial/Switch/Indicator Interface

A DTE serial interface, direct connect and bit mapped switch inputs, and indicator/control outputs are supported.

Serial Interface. A 16-line V.24 and EIA/TIA-232-E logic-compatible serial interface to the DTE is supported. A clock stop output signal is provided which can be used to turn off transmitter and receiver clocks to the DTE in asynchronous modes.

Switch Interface. A direct connect strap input can be sampled. Thirteen switch inputs, bit-mapped through an external three-state buffer, can be sampled in the world-class (W-class) configuration.

Indicator Interface. Four direct connect indicator outputs are supported. Six indicator outputs, bit-mapped through an external latch, are supported in W-class configurations.

Stop Mode Control

The $\overline{\text{STPMODE}}$ input is supported which controls modem entry into Stop Mode.

NVRAM Interface

A serial interface to the optional OEM-supplied 256-byte non-volatile RAM (NVRAM) is provided. Data stored in NVRAM can take precedence over the factory default settings. The 256-byte NVRAM can store up to two user-selectable configurations and can store up to four 45-digit dial strings.

Speaker Interface

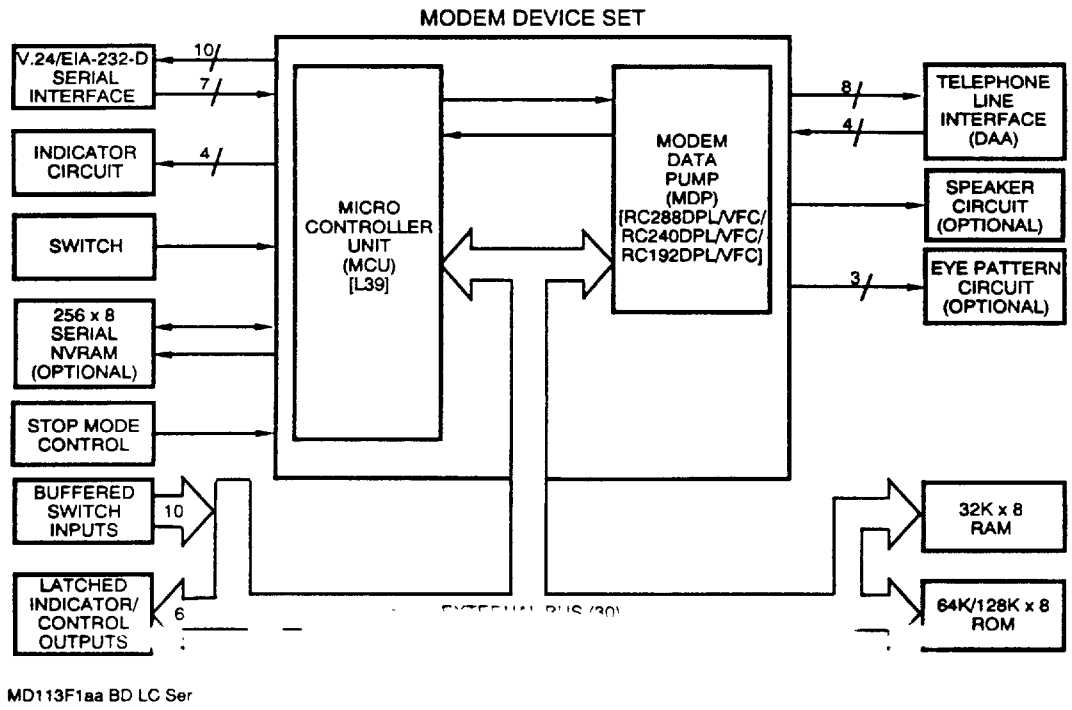
A speaker output, controlled by AT or V.25 bis commands, is provided for an optional OEM-supplied speaker circuit.

MCU External Bus Interface

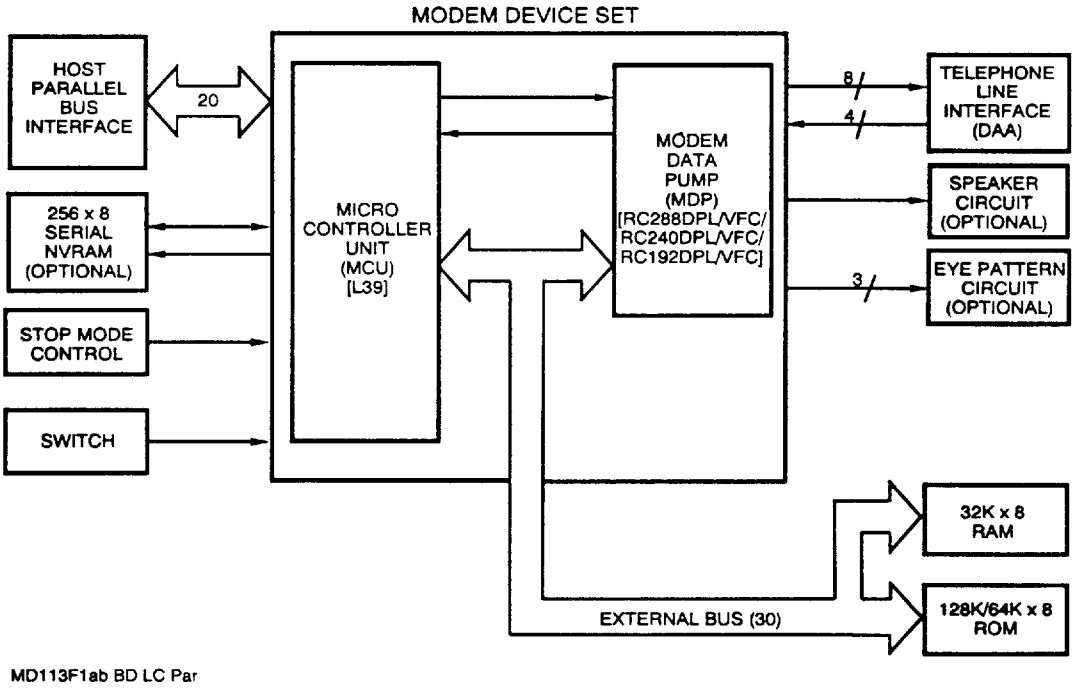
The MCU external bus connects to the MDP, ROM, RAM, and, for W-class configuration, a switch input buffer and indicator output latches. The non-multiplexed bus supports eight bidirectional data lines and 17 address lines. Dedicated MDP, ROM, and RAM chip select and control outputs as well as indicator/control device chip select outputs are also provided.

Line Interface

MDP. The MDP connects to the line interface circuitry via a receive analog input, two transmit analog outputs, a relay driver output, and a ring signal input. The relay output may be used to drive the Caller ID relay.



a. Serial Interface Selected



b. Parallel Interface Selected

Figure 1. Modem General Interface

MCU. The MCU provides four relay control outputs to the line interface. These outputs may be used to control relays such as off-hook, pulse, mute, A/A1, earth, and talk/data. The MCU accepts ring signal and line current sense from the line interface.

Eye Pattern Generator Interface

Eye pattern data, clock, and sync interface signals are provided to allow an external eye pattern generator circuit to be easily added in order to observe modem performance relative to line impairments.

COMMANDS

The modem supports data modem, fax class 1 and 2, MNP 10, and W-class commands and S Registers (see Tables 2 and 3, respectively) depending on the modem model.

Data Modem Operation. Data modem functions operate in response to the basic AT commands when +FCLASS=0. Default parameters support US/Canada operation.

MNP 10 Operation (Option). MNP 10 functions operate in response to MNP 10 commands.

AutoSync Operation (Option). AutoSync operates in response to the &Q4 command.

World Class (W-Class) Operation. W-class functions operate in response to W-class AT and V.25 bis commands.

Fax Modem Operation (Option). Facsimile functions operate in response to fax class 1 commands when +FCLASS=1 or to fax class 2 commands when +FCLASS=2.

DATA MODEM OPERATION

Automatic Speed/Format Sensing (Serial Interface)

The modem can automatically determine the speed and format of the data sent from the DTE (serial interface only). The modem can sense speeds of 300, 600, 1200, 2400, 4800, 7200, 9600, 12000, 14400, 16800, 19200, 21600, 24000, 26400, 28800, 38400, 57600, and 115200 bps and the following data formats:

Parity	Data Length (No. of Bits)	No. of Stop Bits	Character Length (No. of Bits)
None	7	2	10
Odd	7	1	10
Even	7	1	10
None	8	1	10
Odd	8	1	11 *
Even	8	1	11 *

* 11-bit characters are sensed, but the parity bits are stripped off during data transmission in Normal and Error Correction modes. Direct mode does not strip off the parity bits.

The modem can speed sense data with mark or space parity and configures itself as follows:

DTE Configuration	Modem Configuration
7 mark	7 none
7 space	8 none
8 mark	8 none
8 space	8 even

ESTABLISHING DATA MODEM CONNECTIONS

Note: Default parameter values support modem operation in the U.S. For modem use in a different country, parameter values can be changed using ConfigureACE.

Telephone Number Directory

The modem supports four telephone number entries in a directory that can be saved in a serial NVRAM. Each telephone number can be up to 45 characters in length. A telephone number can be saved using the &Zn=x command and a saved telephone number can be dialed using the DS=n command.

Dialing

DTMF Dialing. DTMF dialing using DTMF tone pairs is supported in accordance with CCITT Q.23. The transmit tone level complies with Bell Publication 47001.

Pulse Dialing. Pulse dialing is supported in accordance with EIA/TIA-496-A.

Adaptive Dialing. If DTMF dialing is selected (T command) and the telephone network will not recognize DTMF tones, the modem will switch to pulse dialing. If pulse dialing is selected (P command), pulse dialing will be used.

Blind Dialing. The modem can blind dial in the absence of a dial tone if enabled by the X0, X1, or X3 command.

Modem Handshaking Protocol

If a tone is not detected within the time specified in the S7 register after the last digit is dialed, the modem aborts the call attempt.

Call Progress Tone Detection

Ringback, equipment busy, and progress tones can be detected in accordance with the applicable standard.

Answer Tone Detection

Answer tone detection can be detected over the frequency range of 2100 ± 40 Hz in CCITT modes and 2225 ± 40 Hz in Bell modes.

Ring Detection

A ring signal can be detected from a TTL-compatible 15.3 Hz to 68 Hz square wave input.

Billing Protection

When the modem goes off-hook to answer an incoming call, both transmission and reception of data are prevented for 2 seconds (data modem) or 4 seconds (fax adaptive answer) to allow transmission of the billing signal.

Connection Speeds

The modem functions as a data modem when the +FCLASS=0 command is active. The possible data connection modes/speeds are listed in Table 4. Two methods of establishing a connection are supported: use of the F command and use of N command, speed sense, and S37 register combination.

Table 2. AT Commands

Command	Function
	Basic AT Commands
A/	Re-execute command
A	Answer a call
Bn	Set CCITT or Bell Mode
Cn	Carrier control
Dn	Dial (originate a call)
E	Command echo
Fn	Select line modulation
Hn	Disconnect (hang-up)
In	Identification
Ln	Speaker volume
Mn	Speaker control
Nn	Automode enable
On	Return to on-line data mode
P	Set pulse dial default
Qn	Quiet results codes control
Sn=x	Write to S Register
Sn?	Read S Register
T	Set tone dial default
Vn	Result code form
Wn	Error correction message control
Xn	Extended result codes
Yn	Long space disconnect
Zn	Soft reset and restore profile
&Cn	RLSD (DCD) option
&Dn	DTR option
&F	Restore factory configuration (profile)
&Gn	Select guard tone
&Jn	Telephone jack control
&Kn	Flow control
&Mn	Asynchronous/synchronous mode selection
&Pn	Select pulse dial make/break ratio
&Qn	Asynchronous/synchronous mode selection
&Rn	RTS/CTS option
&Sn	DSR override
&Tn	Test and diagnostic
&V	Display current configuration and stored profiles
&Wn	Store current configuration
&Xn	Select synchronous clock source
&Yn	Designate a default reset profile
&Zn=x	Store phone number
%En	Enable/disable line quality monitor and auto-retrain or fallback/fall forward
%L	Report line signal level
%Q	Report line signal quality
%TTn	PTT testing utilities
\Gn	Modem-to-modem flow control (XON/XOFF)
\Kn	Break control
\Nn	Operating mode
#CID	Caller ID detection and reporting
**	Download to flash memory

Table 2. AT Commands (Cont'd)

Command	Function
	ECC AT Commands
%C	Select data compression
\An	Maximum MNP block size
\Bn	Transmit BREAK to remote
\Ln	MNP block transfer control
	MNP 10 AT Commands
)Mn	Enable cellular power level adjustment
* Hn	Set link negotiation speed
-Kn	MNP extended services
-Qn	Enable fallback to V.22 bis/V.22
@Mn	Select initial transmit level
:E	Compromise equalizer enable
	Fax Class 1 AT+F Commands
+FCLASS=n	Service class
+FTS=n	Stop transmission and wait
+FRS=n	Receive silence
+FTM=n	Transmit data
+FRM=n	Receive data
+FTH=n	Transmit data with HDLC framing
+FRH=n	Receive data with HDLC framing
	Fax Class 2 AT+F Commands
+FCLASS=n	Service class
	Class 2 Action Commands
+FCIG	Set the polled station identification
+FDT	Data transmission
+FET=N	Transmit page punctuation
+FDR	Begin or continue Phase C receive data
+FK	Terminate session
+FLPL	Document for polling
+FSPL	Enable polling
	Class 2 DCE Responses
+FCIG:	Report the polled station identification
+FCON	Facsimile connection response
+FDCS:	Report current session
+FDIS:	Report remote capabilities
+FDTC:	Report the polled station capabilities
+FCFR	Indicate confirmation to receive
+FTSI:	Report the transmit station ID
+FCSI:	Report the called station ID
+FPTS:	Page transfer status
+FET:	Post page message response
+FHNG:	Call termination with status
+FPOLL	Indicates polling request
	Class 2 Session Parameters
+FMFR?	Identify manufacturer
+FMDL?	Identify model
+FREV?	Identify revision
+FDCC	DCE capabilities parameters
+FDIS	Current sessions parameters
+FDCS	Current session results
+FLID	Local ID string
+FPTS	Page transfer status
+FCR	Capability to receive
+FAA	Adaptive answer
+FBUF?	Buffer size (read only)
+FPHCTO	Phase C time out
+FAXERR?	Fax error value
+FBOR	Phase C data bit order

Table 2. AT Commands (Cont'd)

Command	Function
	W-Class AT Commands
%Fn	Split-speed direction select
\S	Display active configuration
\W	Split-speed operation
*B	Display blacklisted numbers
*D	Display delayed numbers
*NCnn	Country select
	W-Class V.25 bis Commands
CIC	Connect incoming call
CNL	Execute AT command (if permitted)
CRN	Call request with number
CRS	Call request with memory address
DIC	Disregard incoming call
PRN	Program normal
RLD	Request list of delayed call numbers
RLF	Request list of forbidden call numbers
RLN	Request stored number list (dial strings)

Table 3. S Registers

Register	Function
S0	Rings to auto-answer
S1	Ring counter
S2	Escape character
S3	Carriage return character
S4	Line feed character
S5	Backspace character
S6	Maximum time to wait for dial tone
S7	Wait for carrier
S8	Pause time for dial delay modifier
S9	Carrier detect response time
S10	Carrier loss disconnect time
S11	DTMF Tone Duration
S12	Escape code guard time
S13	Reserved
S14	General bit mapped options
S15	Reserved
S16	Test mode bit mapped options (&T)
S17	Reserved
S18	Test timer
S19-S20	Reserved
S21	V24/general bit mapped options
S22	Speaker/results bit mapped options
S23	General bit mapped options
S24	Sleep inactivity timer
S25	Delay to DTR (CT108) off
S26	RTS-to-CTS (CT105-to-CT106) delay
S27	General bit mapped options
S28	General bit-mapped options
S29	Flash modifier time
S30	Inactivity timer
S31	General bit-mapped options
S32	XON character
S33	XOFF character
S34-S35	Reserved
S37	Line connection speed
S38	Delay before forced hangup
S39	Flow control
S40	General bit-mapped options
S41	General bit-mapped options
S42-S45	Reserved
S91	PSTN transmit attenuation level
S92	Fax transmit attenuation level
S95	Result code messages control
	ECC S Registers
S36	LAPM failure control
S46	Data compression control
S48	V.42 negotiation control
S82	Break handling control
S86	Call failure reason code
	W-Class S Registers
S80	Soft-switch functions
	Cellular Registers
S201	Cellular transmit level

Automode

Automode detection can be enabled by the N1 or F0 commands to allow the modem to connect to a remote modem in V.FC mode or in accordance with EIA/TIA-PN2330. Automode is disabled on a leased line.

DATA MODE

Data mode exists when a telephone line connection has been established between modems and all handshaking has been completed.

Speed Buffering (Normal Mode)

Speed buffering allows a DTE to send to, and receive data from, a modem at a speed different than the line speed. The modem supports speed buffering at all line speeds.

Flow Control

DTE-to-Modem Flow Control. If the modem-to-line speed is less than the DTE-to-modem speed, the modem supports XOFF/XON or RTS/CTS flow control with the DTE to ensure data integrity.

Modem-to-Modem Flow Control. When enabled by the \G1 command, the modem supports XON/XOFF flow control with the remote modem to ensure data integrity. Modem-to-modem flow control is not used in error correction mode. In this case, flow control is accomplished within the error-correction protocol.

Escape Sequence Detection

The "+++" escape sequence with guard time can be used to return control to the command mode from the data mode. Escape sequence detection is disabled by a S2 Register value greater than 127. Escape sequence detection is disabled in synchronous mode.

BREAK Detection

The modem can detect a BREAK signal from either the DTE or the remote modem. The \Kn command determines the modem response to a received BREAK signal.

Telephone Line Monitoring

GSTN Cleardown (V.FC, V.32 bis, V.32). Upon receiving GSTN Cleardown from the remote modem in a non-error correcting mode, the modem cleanly terminates the call.

Loss of Carrier. If carrier is lost for a time greater than specified by the S10 register, the modem will disconnect.

Receive Space Disconnect. If selected by the Y1 command in non-error-correction mode, the modem will disconnect after receiving 1.6 ± 10% seconds of continuous SPACE.

Send SPACE on Disconnect

If selected by the Y1 command in non-error-correction mode, the modem will send 4 ± 10% seconds of continuous SPACE when a locally commanded hang-up is issued by the &Dn or H command.

Fall Forward/Fallback (V.FC, V.32 bis/V.32)

During initial handshake, the modem will fallback to the optimal line connection within V.FC mode if the remote modem is a V.FC modem, or within V.32 bis/V.32 mode if the remote modem is a V.32 bis/V.32 modem, depending upon signal quality if automode is enabled by the N1 command.

When connected in V.FC or V.32 bis/V.32 mode, the modem will fall forward or fallback to the optimal line speed within the connected mode depending upon signal quality if fall forward/fallback is enabled by the %E2 command.

Retrain

The modem may lose synchronization with the received line signal under poor line conditions. If this occurs, retraining may be initiated to attempt recovery depending on the type of connection.

The modem initiates a retrain if line quality becomes unacceptable if enabled by the %E command. The modem continues to retrain until an acceptable connection is achieved or until 30 seconds elapse which will result in telephone line disconnect.

Synchronous Data Mode (Serial Interface Only)

The modem can establish a synchronous connection in accordance with the &Mn or &Qn commands. Upon completing the physical handshake, the modem enters synchronous data mode. The inactivity timer is not used during synchronous data mode.

Direct Mode (Serial Interface Only)

The Direct mode allows data to be transmitted and received directly from the DTE and remote modem. The Direct mode is selected with the &Q0 or \N1 command. In Direct mode, no flow control characters are recognized or transmitted, the modem cannot execute error correction, and the inactivity timer is not used. Speed buffering is disabled in Direct mode.

Table 4. Connection Speed Options

Configuration	Rate
V.FC	28800[1], 26400[1], 24000[2], 21600[2], 19200, 16800, or 14400 bps
V.32 bis	14400, 12000, 9600, 7200, or 4800 bps
V.32	9600 or 4800 bps
V.22 bis	2400 or 1200 bps
V.22	1200 bps
V.23	1200Tx/75Rx or 75Tx/1200Rx
V.21	0-300 bps
Bell 212A	1200 bps
Bell 103	0-300 bps

Notes:
1. RC288ACL/VFC.
2. RC288ACL/VFC and RC240ACL/VFC.

Programmable Inactivity Timer

The modem will disconnect from the line if data is not sent or received for a specified length of time. In normal or error-correction mode, this inactivity timer is reset when data is received from either the DTE or from the line. This timer can be set to a value between 0 and 2550 seconds by register S30. A value of 0 disables the inactivity timer.

DTE Signal Monitoring

$\overline{\text{DTR}}$. When $\overline{\text{DTR}}$ is asserted, the modem responds in accordance with the &Dn and &Qn commands.

$\overline{\text{RTS}}$. $\overline{\text{RTS}}$ is used for flow control if enabled by the &K command in normal or error-correction mode, or to affect the $\overline{\text{CTS}}$ output if enabled by the &R command in synchronous mode.

$\overline{\text{RDL}}$. When $\overline{\text{RDL}}$ is asserted, the modem requests a remote digital loop if connected in non-error-correction mode (serial interface only).

$\overline{\text{AL}}$. When $\overline{\text{AL}}$ is asserted, the modem disconnects and enters analog loop (serial interface only).

ERROR CORRECTION AND DATA COMPRESSION

V.42 Error Correction

V.42 supports two methods of error correction: LAPM and, as a alternative, MNP 4. The modem provides a detection and negotiation technique for determining and establishing the preferred method of error correction between two modems.

MNP 2-4 Error Correction

MNP 2-4 is a data link protocol that uses error correction algorithms to ensure data integrity. MNP block or stream mode operation may be selected by the \Ln command.

In stream mode, the modem sends data frames in varying lengths depending on the amount of time between characters coming from the DTE.

In block mode, the modem sends data frames of 256 characters in length. Special communication software must be used when using block mode.

V.42 bis Data Compression

V.42 bis data compression mode, enabled by the %Cn or S46 command, operates when a LAPM or MNP 10 connection is established.

The V.42 bis data compression employs a "string learning" algorithm in which a string of characters from the DTE is encoded as a fixed length codeword. Two 2k-byte dictionaries are used to store the strings. These dictionaries are dynamically updated during normal operation.

MNP 5 Data Compression

MNP 5 data compression mode, enabled by the %Cn command, operates during an MNP connection.

In MNP 5, the modem increases its throughput by compressing data into tokens before transmitting it to the remote modem, and by decompressing encoded received data before sending it to the DTE.

MNP 10 DATA THROUGHPUT ENHANCEMENT (TO V.32 BIS)

MNP10 protocol, cellular functionality, and MNP Extended Services enhance performance under adverse channel conditions such as those found in rural, long distance, or cellular environments. An MNP 10 connection is established when either an MNP 2-4 connection is negotiated with a remote modem supporting MNP 10 or MNP 10 extended services is enabled as described below. MNP 10 functions include:

Robust Auto-Reliability. Higher connection success rate is achieved by attempting to overcome channel interference during the modem negotiation phase while maintaining backward compatibility with non-MNP 10 modems.

Negotiated Speed Upshift. Initial connection and MNP handshake is performed at the most dependable speed, then the connection upshifts to the highest supported modem/channel speed. This function is particularly useful in channel conditions with high connection failure rates.

Aggressive Adaptive Packet Assembly. Frame size is dynamically changed to quickly adapt to varying levels of interference.

Dynamic Speed Shifting. Connection speed is shifted upward or downward to optimize data throughput for the channel conditions by continuously monitoring the line quality and link performance.

Dynamic Transmit Level Adjustment. Transmit level is dynamically adjusted to adapt to the varying cellular network environment and to prevent "clipping," which causes data corruption, due to the Preemphasis and Compander effect.

MNP 10 Extended Services. The modem can quickly switch to MNP 10 operation when the remote modem supports MNP 10 and both modems are configured to operate in V.42.

V.42 bis/MNP 5 Support. MNP 10 can operate with V.42 bis or MNP 5 data compression.

FAX CLASS 1 AND CLASS 2 OPERATION

The modem operates as a facsimile (fax) DCE whenever the +FCLASS=1 or +FCLASS=2 command is active. In the fax mode, the on-line behavior of the modem is different from the data (non-fax) mode. After dialing, modem operation is controlled by the fax commands. Some AT commands are still valid but may operate differently from data modem mode.

Calling Tone

Calling tone is generated in accordance with T.30.

WORLD CLASS COUNTRY SUPPORT

The W-class models include functions which support modem operation in multiple countries. The following capabilities are provided in addition to the data modem functions previously described. Country dependent parameters are all programmable by ConfigurACE.

V.25 bis Commands

V.25 bis commands (Table 2) are available in asynchronous modes when enabled by the AT/V25B bit in the External Buffer 1 inputs.

Blacklist Parameters

The modem can operate in accordance with requirements of individual countries to prevent misuse of the network by limiting repeated calls to the same number when previous call attempts have failed. Call failure can be detected for reasons such as no dial tone, number busy, no answer, no ringback detected, voice (rather than modem) detected, and key abort (dial attempt aborted by user). Actions resulting from such failures can include specification of minimum inter-call delay, extended delay between calls, and maximum numbers of retries before the number is permanently forbidden ("blacklisted"). Up to bers may be tabulated. The blacklist parameters are established by ConfigurACE.

Dialing

Dial Tone Detection. Dial tone detection levels and frequency ranges are programmable by ConfigurACE.

DTMF Dialing. Transmit output level, DTMF signal duration, and DTMF interdigit interval parameters are programmable by ConfigurACE.

Pulse Dialing. Parameters such as make/break times, set/clear times, and dial codes are programmable by ConfigurACE.

Ring Detection. The frequency range is programmable by ConfigurACE.

Adaptive Dialing. Adaptive dialing can be disabled by ConfigurACE.

Blind Dialing. Blind dialing, permitted only in some countries, can be enabled or disabled by setting or resetting a flag bit in the corresponding country file using ConfigurACE. If enabled, blind dialing can be invoked using the ATX command; if disabled, blind dialing is not available.

Carrier Transmit Level

The carrier transmit level is programmable by ConfigurACE to match specific country and DAA characteristics.

Calling Tone

Calling tone is generated in accordance with V.25. Calling tone may be toggled (enabled/disabled) by inclusion of a "A" character in a dial string. It may also be enabled or disabled by programming a country specific parameter using ConfigurACE.

Call Progress Tone Detection

Frequency and cadence of tones for busy, ringback, congested, dial tone 1, and dial tone 2 are programmable by ConfigurACE.

Answer Tone Detection

The answer tone detection period is programmable by ConfigurACE.

Relay Control

On-hook/off-hook, make/break, and set/clear relay control parameters are programmable by ConfigurACE.

Automatic Country Code Recognition

Automatic country code recognition is supported in conjunction with country identification code circuitry provided in the DAA. Automatic country code recognition is enabled using the AT*NCnn command with nn = 0. Automatic country code recognition is disabled using the AT*NCnn command with nn = any valid country code other than 0. parameters in Table 9.)

Once enabled, the MCU interrogates the DAA circuit upon reset (POR or the ATZ command) or attempt to go off-hook. An 8-bit country code is shifted in from the DAA and is used to look up the corresponding country code parameters loaded in ROM. If country code parameters are present for the shifted-in country code and the country is different from the active country, the country code parameters are loaded. If the shifted-in country code does match a country with stored parameters in ROM, the modem issues an ERROR message.

Note that when automatic country code recognition is enabled, the country code can be changed at any time before going off-hook (e.g., by changing the DAA or selecting a different country code on the DAA). Upon going off-hook, the MCU will then load the country code parameters corresponding to the new DAA country code.

ConfigurACE UTILITY PROGRAM

The ConfigurACE utility program allows the OEM to customize the MCU firmware to suit specific application and country requirements. ConfigurACE allows programming of functions such as:

- —Loading of multiple sets of country parameters
- —Call progress and blacklisting parameters
- —Entry of S register maximum/minimum values
- —Use of "soft switches" instead of panel switches
- —Modification/limitation of transmit levels
- —Modification of result codes
- —Modification of factory default values
- —Customization of the ATI4 response
- —Customization of fax OEM messages

This program, which runs on a PC-compatible computer, modifies the hex object code which can be programmed

directly into the system ROM. Lists of the generated parameters can be displayed or printed.

Rockwell-provided country parameter files allow a complete set of country-specific call progress and blacklisting parameters to be selected.

DIAGNOSTICS

Commanded Tests

Diagnostics are performed in response to &T commands, serial interface control signals, or switch inputs per V.54.

Analog Loopback. Data from the local DTE is sent to the modem, which loops the data back to the local DTE.

Analog Loop Self Test. An internally generated test pattern of alternating 1s and 0s (reversals) is sent to the modem. An error detector within the modem checks for errors in the string of reversals.

Remote Digital Loopback (RDL). Data from the local DTE is sent to the remote modem which loops the data back to the local DTE.

Remote Digital Loopback with Self Test. An internally generated pattern is sent from the local modem to the remote modem which loops the data back to the local modem.

Local Digital Loopback. When local digital loop is requested from the local DTE, two data paths are set up in the local modem. Data from the local DTE is looped back to the local DTE (path 1) and data received from the remote modem is looped back to the remote modem (path 2).

Power On Reset Tests

Upon power on, or receipt of the Z command, the modem performs tests of the MDP, RAM, ROM, and NVRAM.

LOW POWER MODES

Sleep Mode

Entry. The modem will enter the low power sleep mode when no line connection exists and no host activity occurs for the period of time specified in the S24 register. All MCU circuits are turned off except the internal MCU clock circuitry in order to consume lower power but be able to immediately wake up and resume normal operation.

Wake-Up. Wakeup occurs when a ring is detected on the telephone line, the host writes to the modem (parallel interface version) or the DTE sends a character to the modem (serial interface version).

Stop Mode

Entry. The modem will enter the low power stop mode when the $\overline{\text{STPMODE}}$ input is asserted. All MCU circuits are turned off including the internal MCU clock circuitry in order to consume lower power than sleep mode. The modem will enter stop mode immediately, terminating a line connection, terminating any test in process, and allowing any data in the Receive Buffer Register to clear.

$\overline{\text{STPMODE}}$ must be returned high before the modem can wake-up.

Wake-Up. Wakeup occurs when a ring is detected on the telephone line, the host writes to the modem (parallel interface version) or the DTE sends a character to the modem (serial interface version). Since the modem requires more time to attain normal operation when waking up from Stop mode rather than from Sleep mode, the host must send a character to the modem before issuing the first AT command.

CALLER ID

Caller ID can be enabled/disabled using the #CID command. When enabled, caller ID information (date, time, caller code, and name) can be passed to the DTE in formatted or unformatted form. Inquiry support allows the current caller ID mode and mode capabilities of the modem to be retrieved from the modem.

ADDITIONAL INFORMATION

Additional information is described in the RC288ACL/VFC Modem Designer's Guide (Order No. 1032) and the AT Command Reference Manual for RC288ACL/VFC and RC288ACi/VFC Modem Families (Order No. 1034).

HARDWARE INTERFACE

HARDWARE INTERFACE SIGNALS

The modem hardware interface signals for serial and parallel interface configurations are shown in Figures 2 and 3, respectively.

The MCU pin assignments for serial interface firmware are shown in Figure 4 and are listed in Table 5.

The MCU pin assignments for parallel interface firmware are shown in Figure 5 and are listed in Table 6.

The MDP pin assignments are shown in Figure 6 and are listed in Table 7.

The MCU hardware interface signals are defined in Table 8.

The MDP hardware interface signals are defined in Table 9.

The digital electrical characteristics for the hardware interface signals are listed in Table 10.

The analog electrical characteristics for the hardware interface signals are listed in Table 11.

The current and power requirements are listed in Table 12.

The absolute maximum ratings are listed in Table 13.

Table 14 shows the parallel interface registers and the corresponding bit assignments.

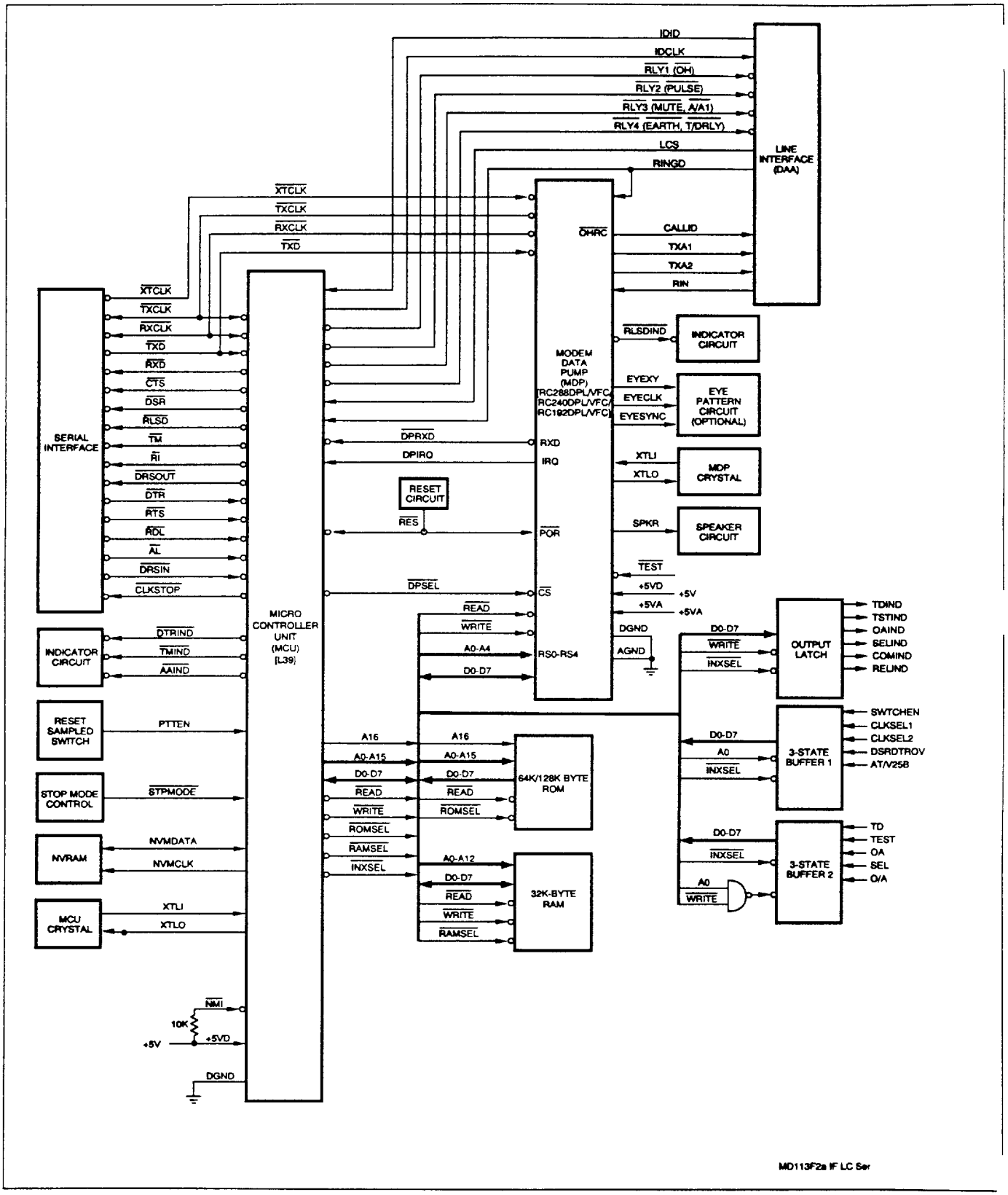


Figure 2. Hardware Signals-Serial Interface

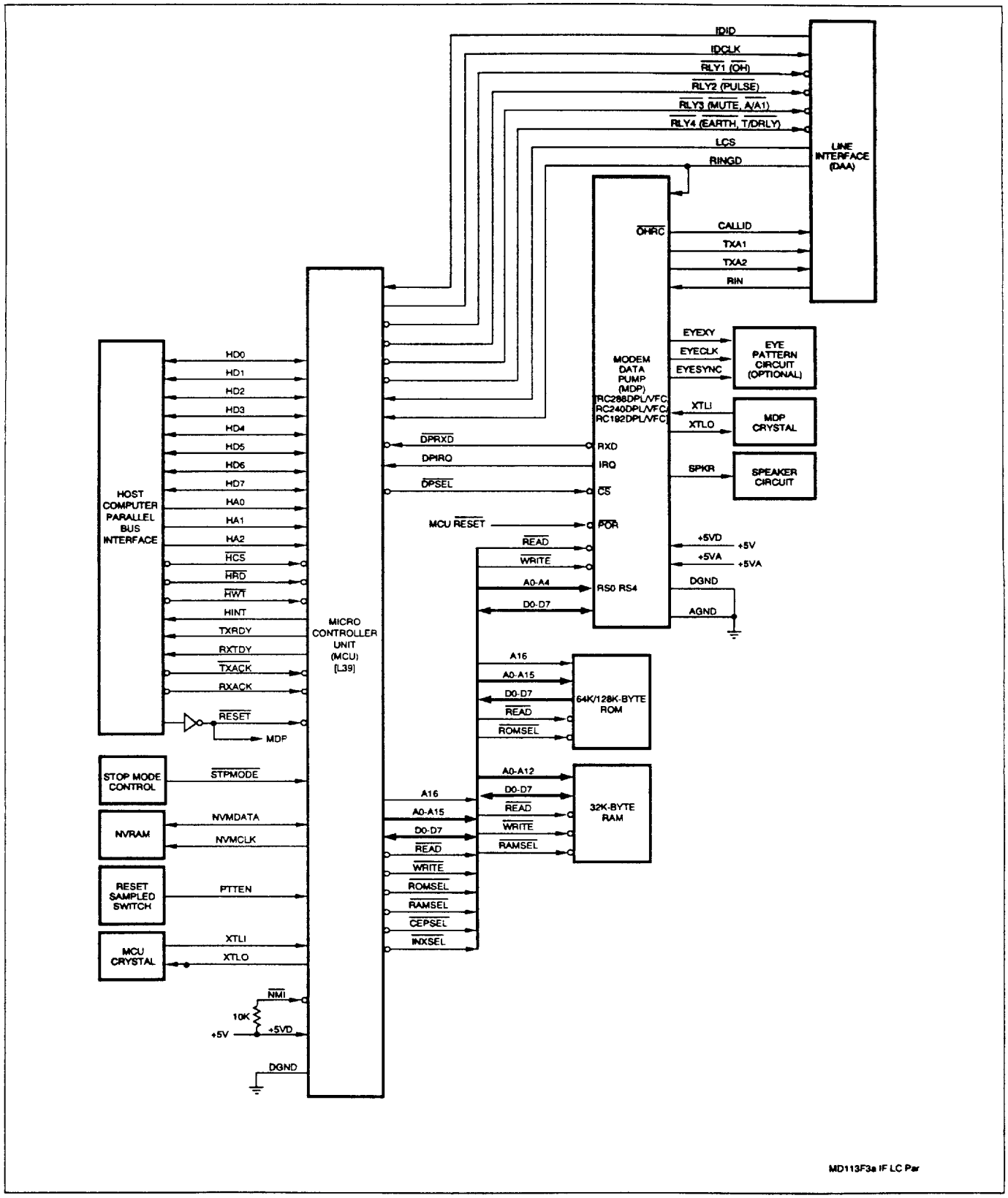


Figure 3. Hardware Signals-Parallel Interface

Table 5. MCU Pin Signals - Serial I/F - 80-Pin PQFP

Pin	MCU Signal	I/O Type	Modem Signal
1	RES	IC	RES
2	NMI		NMI (Note 4)
3	WT	OA	WRITE
4	RD	OA	READ
5	PE2	OA	RLY3 (MUTE, A/A1)
6	PE3	OA	RLY4 (EARTH, T/DRLY)
7	PSC	IA	PSC
8	VCC1	PWR	VCC
9	XTLI	IE	XTLI
10	XTLO	OE	XTLO
11	GND	GND	GND
12	GND	GND	GND
13	PC0	OA	DSR
14	PC1	OA	CTS
15	PC2	OA	RLSD
16	PC3	OA	DRSOUT
17	PC4	OA	DRSIN
18	PC5	OA	RI
19	PC6	OA	TM
20	PC7	IA	RDL
21	PD0	OA	DTRIND
22	PD1		NC
23	PD2	IA	NC
24	PD3	IA	STPMODE
25	PD4	IA	DTR
26	PD5	IA	AL
27	PD6	IA	RTS
28	PD7	IA	DPIRQ
29	GND	GND	GND
30	PE4	IA	LCS
31	PE5	OA [IA]	CLKSTOP [PTTEN]
32	PA0	IA	RINGD
33	PA1	OA	NVMDATA (Note 4)
34	PA2	IA	TXD
35	PA3	IA	TXCLK
36	PA4	IA	RXCLK
37	PA5	MI	DPRXD
38	PA6	OA	RXD
39	PA7	OA	NVMCLK
40	TST		TST (Note 5)
41	D0	IA/OA	D0
42	D1	IA/OA	D1
43	D2	IA/OA	D2
44	D3	IA/OA	D3
45	D4	IA/OA	D4
46	D5	IA/OA	D5
47	D6	IA/OA	D6
48	D7	IA/OA	D7
49	PE6	OA	IDCLK
50	PE7	IA	IDID
51	VCC2	PWR	VCC
52	GND	GND	GND
53	GND	GND	GND
54	A0	OA	A0
55	A1	OA	A1
56	A2	OA	A2
57	A3	OA	A3
58	A4	OA	A4
59	A5	OA	A5
60	A6	OA	A6

Table 5. MCU Pin Signals-Ser I/F-80-Pin PQFP (Cont'd)

Pin	MCU Signal	I/O Type	Modem Signal
61	A7	OA	A7
62	A8	OA	A8
63	A9	OA	A9
64	A10	OA	A10
65	A11	OA	A11
66	A12	OA	A12
67	A13	OA	A13
68	A14	OA	A14
69	A15	OA	A15
70	PE0	OA	RLY1 (OH)
71	PE1	OA	RLY2 (PULSE)
72	GND	GND	GND
73	PB0	OA	A16
74	PB1	MI	DPSEL
75	PB2	OA	ROMSEL
76	PB3	OA	RAMSEL
77	PB4	OA	INXSEL
78	PB5	OA	CEPSEL
79	PB6	OA	AAIND
80	PB7	OA	TMIND

Notes:
1. MI = Modem interconnect.
2. NC = No external connection.
3. NU = Not used; connect as noted.
4. Connect to VCC through 10 KΩ.
5. Connect to GND.

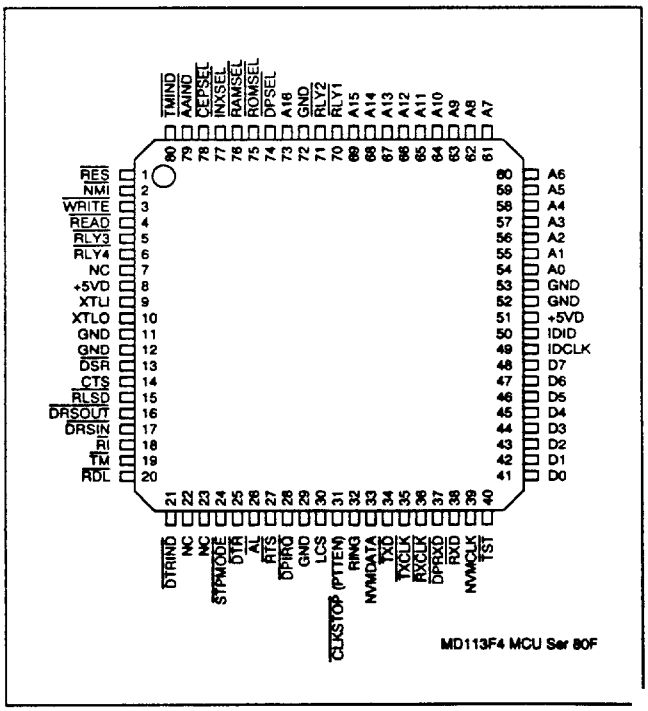


Figure 4. MCU Pin Signals - Serial I/F - 80-Pin PQFP

Table 6. MCU Pin Signals - Parallel I/F - 80-Pin PQFP

Pin	MCU Signal	I/O Type	Modem Signal
1	RES	IC	RES
2	NMI		NMI (Note 4)
3	WT	OA	WRITE
4	RD	OA	READ
5	PE2	OA	RLY3 (MUTE, A/A1)
6	PE3	OA	RLY4 (EARTH, T/DRLY)
7	PSC	IA	PSC
8	VCC1	PWR	VCC
9	XTLI	IE	XTLI
10	XTLO	OE	XTLO
11	GND	GND	GND
12	GND	GND	GND
13	PC0	IA/OA	HD0
14	PC1	IA/OA	HD1
15	PC2	IA/OA	HD2
16	PC3	IA/OA	HD3
17	PC4	IA/OA	HD4
18	PC5	IA/OA	HD5
19	PC6	IA/OA	HD6
20	PC7	IA/OA	HD7
21	PD0	IA	HA0
22	PD1	IA	HA1
23	PD2	IA	HA2
24	PD3	IA	STPMODE
25	PD4	IA	HCS
26	PD5	IA	HWT
27	PD6	IA	HRD
28	PD7	IA	DPIRQ
29	GND	GND	GND
30	PE4	IA	LCS
31	PE5	IA	PTTEN
32	PA0	IA	RINGD
33	PA1	OA	NVMDATA (Note 4)
34	PA2		NC
35	PA3	IA	TXACK
36	PA4	IA	RXACK
37	PA5	OA	TXRDY
38	PA6	OA	RXRDY
39	PA7	OA	NVMCLK
40	TST		TST (Note 5)
41	D0	IA/OA	D0
42	D1	IA/OA	D1
43	D2	IA/OA	D2
44	D3	IA/OA	D3
45	D4	IA/OA	D4
46	D5	IA/OA	D5
47	D6	IA/OA	D6
48	D7	IA/OA	D7
49	PE6	OA	IDCLK
50	PE7	IA	IDID
51	VCC2	PWR	VCC
52	GND	GND	GND
53	GND	GND	GND
54	A0	OA	A0
55	A1	OA	A1
56	A2	OA	A2
57	A3	OA	A3
58	A4	OA	A4
59	A5	OA	A5
60	A6	OA	A6

Table 6. MCU Pin Signals-Par I/F-80-Pin PQFP (Cont'd)

Pin	MCU Signal	I/O Type	Modem Signal
61	A7	OA	A7
62	A8	OA	A8
63	A9	OA	A9
64	A10	OA	A10
65	A11	OA	A11
66	A12	OA	A12
67	A13	OA	A13
68	A14	OA	A14
69	A15	OA	A15
70	PE0	OA	RLY1 (OH)
71	PE1	OA	RLY2 (PULSE)
72	GND	GND	GND
73	PB0	OA	A16
74	PB1	MI	DPSEL
75	PB2	OA	ROMSEL
76	PB3	OA	RAMSEL
77	PB4		NC
78	PB5	OA	CEPSEL
79	PB6		NC
80	PB7	OA	HINT

Notes:
1. MI = Modem interconnect.
2. NC = No external connection.
3. NU = Not used; connect as noted.
4. Connect to VCC through 10 KΩ.
5. Connect to GND.

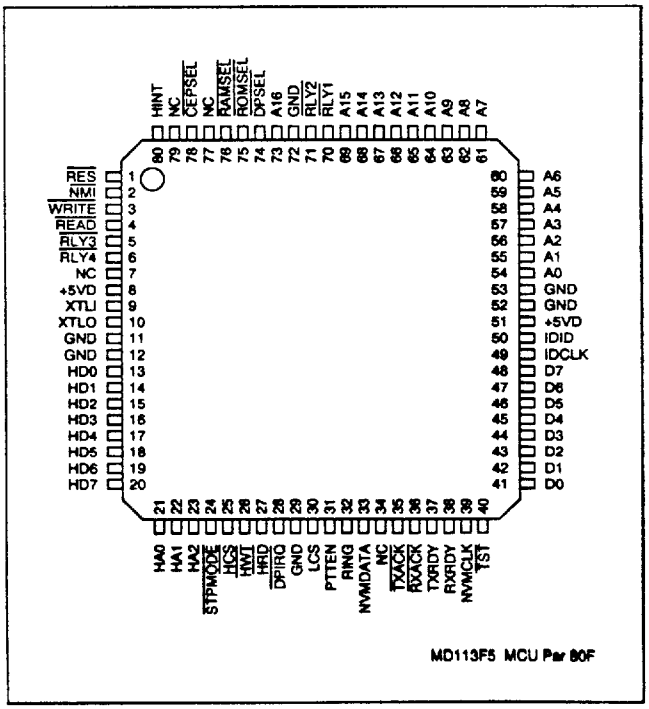
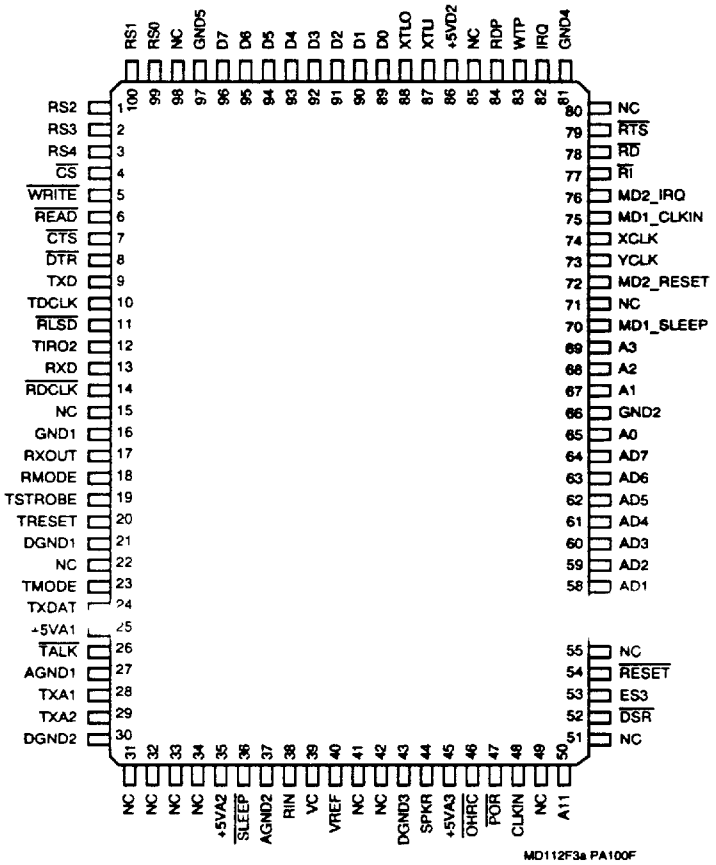
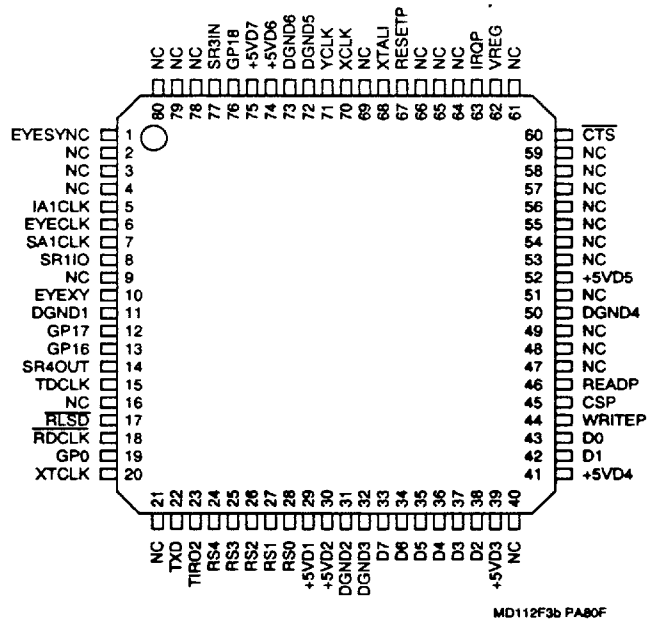


Figure 5. MCU Pin Signals - Parallel I/F - 80-Pin PQFP



a. 100-Pin PQFP (MD1)



b. 80-Pin PQFP (MD2)

Figure 6a. Pin Signals - 100-Pin and 80-Pin PQFPs

Table 7a. MDP Pin Signals - 100-Pin PQFP (MD1)

Pin	Signal Label	I/O Type	Interface
1	RS2	IA	Host Parallel Interface
2	RS3	IA	Host Parallel Interface
3	RS4	IA	Host Parallel Interface
4	CS	IA	Host Parallel Interface
5	WRITE	IA	Host Parallel Interface
6	READ	IA	Host Parallel Interface
7	CTS	OA	DTE Serial Interface
8	DTR	IA	DTE Serial Interface
9	TXD	IA	DTE Serial Interface
10	TDCLK	OA	DTE Serial Interface
11	RLSD	OA	DTE Serial Interface
12	TIRO2	MI	MD2: TIRO2
13	RXD	OA	DTE Serial Interface
14	RDCLK	OA	DTE Senal Interface
15	NC		
16	GND1	GND	
17	RXOUT	MI	MD2: SR3IN
18	RMODE	MI	MD1: TMODE/MD2: SR1IO
19	TSTROBE	MI	MD2: IA1CLK
20	TRESET	MI	MD2: SA1CLK
21	DGND1	GND	
22	NC		
23	TMODE	MI	MD1: RMODE/MD2: SR1IO
24	TXDAT	MI	MD2: SR4OUT
25	+5VA1	PWR	
26	TALK	OD	Line Interface
27	AGND1	GND	
28	TXA1	O(DD)	Line Interface
29	TXA2	O(DD)	Line Interface
30	DGND2	GND	
31	NC		
32	NC		
33	NC		
34	NC		
35	+5VA2	PWR	
36	SLEEP	MI	MD1: MD1_SLEEP
37	AGND2	GND	
38	RIN	I(DA)	Line Interface
39	VC	MI	To GND through capacitors
40	VREF	MI	To VC through capacitors
41	NC		
42	NC		
43	DGND3	GND	
44	SPKR	O(DF)	Speaker Circuit
45	+5VA3	PWR	
46	OHRC	OD	Line Interface
47	POR	MI	Connect to MCU RES
48	CLKIN	MI	MD1: MD1_CLKIN
49	NC		
50	A11	MI	MD2: RS4 (Note 3)
51	NC		
52	DSR	OA	DTE Serial Interface
53	ES3	MI	MD2: CSP
54	RESET	IA	MD1: POR
55	NC		
56	+5VD1	PWR	
57	AD0	MI	MD2: D0
58	AD1	MI	MD2: D1
59	AD2	MI	MD2: D2
60	AD3	MI	MD2: D3

Table 7a. MDP Pin Signals - 100-Pin PQFP (MD1) (Cont'd)

Pin	Signal Label	I/O Type	Interface
61	AD4	MI	MD2: D4
62	AD5	MI	MD2: D5
63	AD6	MI	MD2: D6
64	AD7	MI	MD2: D7
65	A0	MI	MD2: RS0
66	GND2	GND	
67	A1	MI	MD2: RS1
68	A2	MI	MD2: RS2
69	A3	MI	MD2: RS3
70	MD1_SLEEP	MI	MD1: SLEEP
71	NC		
72	MD2_RESET	MI	MD2: RESETP
73	YCLK	MI	MD2: YCLK
74	XCLK	MI	MD2: XCLK
75	MD1_CLKIN	MI	MD1: CLKIN
76	MD2_IRQ	MI	MD2: IRQP
77	RI	OA	DTE Serial Interface
78	RD	IA	Line Interface
79	RTS	IA	DTE Serial Interface
80	NC		(See Note 4.)
81	GND4	GND	
82	IRQ	OA	Host Parallel Interface
83	WTP	MI	MD2: WTP
84	RDP	MI	MD2: RDP
85	NC		
86	+5VD2	PWR	
87	XTLI	I	Crystal/Clock Circuit
88	XTLO	O	Crystal/Clock Circuit
89	D0	IA/OA	Host Parallel Interface
90	D1	IA/OA	Host Parallel Interface
91	D2	IA/OA	Host Parallel Interface
92	D3	IA/OA	Host Parallel Interface
93	D4	IA/OA	Host Parallel Interface
94	D5	IA/OA	Host Parallel Interface
95	D6	IA/OA	Host Parallel Interface
96	D7	IA/OA	Host Parallel Interface
97	GND5	GND	
98	NC		
99	RS0	IA	Host Parallel Interface
100	RS1	IA	Host Parallel Interface

Notes:

1. I/O Type:
   - MI = Modem interconnect.
   - IA, IB = Digital input.
   - OA, OB, OD = Digital output.
   - I(DA)] = Analog input.
   - O(DD), O(DF) = Analog output.
2. NC = no external connection.
3. Pin 50 (A11) is functionally compatible with RC144DPL 100-pin PQFP pin 50 (A13).
4. Pin 80 (NC internally) can be connected to GND for functional compatibility with RC144DPL 100-pin PQFP pin 80 (GND3).

Table 7b. MDP Pin Signals - 80-Pin PQFP (MD2)

Pin	Signal Label	I/O Type	Interface
1	EYESYNC	OA	Eye Pattern Test Circuit
2	NC		
3	NC		
4	NC		
5	IA1CLK	MI	MD1: TSTROBE
6	EYECLK	MI	Eye Pattern Test Circuit
7	SA1CLK	MI	MD1: TRESET
8	SR1IO	MI	MD1: TMODE
9	NC		
10	EYEXY	OA	Eye Pattern Test Circuit
11	DGND1	GND	
12	GP17	MI	Connect to DGND
13	GP16	MI	Connect to DGND
14	SR4OUT	MI	MD1: TXDAT
15	TDCLK	IA	DTE: Serial Interface
16	NC		
17	$\overline{\text{RLSD}}$	IA	DTE: Serial Interface
18	RDCLK	IA	DTE: Serial Interface
19	GP0	MI	Connect to EYESYNC
20	XTCLK	IA	DTE: Serial Interface
21	NC		
22	TXD	IA	DTE: Serial Interface
23	TIRO2	MI	MD1: TIRO2
24	RS4	MI	MD1: A11
25	RS3	MI	MD1: A3
26	RS2	MI	MD1: A2
27	RS1	MI	MD1: A1
28	RS0	MI	MD1: A0
29	+5VD1	PWR	
30	+5VD2	PWR	
31	DGND2	GND	
32	DGND3	GND	
33	D7	MI	MD1: AD7
34	D6	MI	MD1: AD6
35	D5	MI	MD1: AD5
36	D4	MI	MD1: AD4
37	D3	MI	MD1: AD3
38	D2	MI	MD1: AD2
39	+5VD3	PWR	
40	NC		
41	+5VD4	PWR	
42	D1	MI	MD1: AD1
43	D0	MI	MD1: AD0
44	WRITEP	MI	MD1: WTP
45	CSP	MI	MD1: ES3
46	READP	MI	MD1: RDP
47	NC		
48	NC		
49	NC		
50	DGND4	GND	
51	NC		
52	+5VD5	PWR	
53	NC		
54	NC		
55	NC		
56	NC		
57	NC		
58	NC		
59	NC		
60	$\overline{\text{CTS}}$	MI	DTE: Serial Interface

Table 7b. MDP Pin Signals - 80-Pin PQFP (MD2) (Cont'd)

Pin	Signal Label	I/O Type	Interface
61	NC		
62	VREG	MI	To GND thru 0.1 µF[3]
63	IRQP	MI	MD1: MD2_IRQ
64	NC		
65	NC		
66	NC		
67	RESETP	MI	MD1: MD2_RESET
68	XTALI	I	Connect to DGND
69	NC		
70	XCLK	MI	MD1: XCLK
71	YCLK	MI	MD1: YCLK
72	DGND5	GND	
73	DGND6	GND	
74	+5VD6	PWR	
75	+5VD7	PWR	
76	GP18	MI	Connect to DGND
77	SR3IN	MI	MD1: RXOUT
78	NC		
79	NC		
80	NC		

Notes:

1. I/O Type:
   MI = Modem interconnect
   OA = Digital output.
   IA = Digital input.
2. NC = no external connection.
3. VREG on the RC288DPL/VFC must be connected to GND through a 0.1 µF capacitor; VREG on the RC288DPi/VFC can be connected to GND through a 0.1 µF capacitor or can be left open (NC).

Table 7c. MDP Pin Signals - 68-Pin PLCC

Pin	Signal Label	I/O Type	Interface
1	VREG	MI	To GND through 0.1 µF[3]
2	DSP_RESET	MI	Output to $\overline{RES}$
3	IA_CLKIN	MI	Output to CLKIN
4	DSP_IRQ	MI	Input from $\overline{IRQ}$
5	$\overline{RI}$/TXRQ	OA	DTE Serial/DMA Interface
6	RINGD	IA	Line Interface
7	$\overline{RTS}$	IA	DTE Serial Interface
8	IRQ	OA	Host Parallel Interface
9	D1	IA/OA	Host Parallel Interface
10	DGND1	GND	
11	+5VD1	PWR	
12	XTLI	I	Crystal/Clock Circuit
13	XTLO	O	Crystal/Clock Circuit
14	D0	IA/OA	Host Parallel Interface
15	D2	IA/OA	Host Parallel Interface
16	D3	IA/OA	Host Parallel Interface
17	D5	IA/OA	Host Parallel Interface
18	D7	IA/OA	Host Parallel Interface
19	DGND2	GND	
20	RS0	IA	Host Parallel Interface
21	+5VA	PWR	
22	AGND1	GND	
23	RIN	I(DA)	Line Interface
24	VC	MI	To GND through capacitors
25	VREF	MI	To VC through capacitors
26	TXA2	O(DD)	Line Interface
27	TXA1	O(DD)	Line Interface
28	$\overline{TALK}$	OA	Line Interface
29	SPKR	O(DF)	Speaker Circuit
30	AGND2	GND	
31	$\overline{OHRC}$	OD	Line Interface
32	$\overline{POR}$	MI	Connect to MCU $\overline{RES}$
33	CLKIN	MI	Output from IA_CLKOUT
34	$\overline{DTR}$	IA	DTE Serial Interface
35	RXD	OA	DTE Serial Interface
36	+5VD2	PWR	
37	$\overline{CTS}$	OA	DTE Serial Interface
38	$\overline{IRQ}$	MI	Output to DSP_IRQ
39	$\overline{RES}$	MI	Input from DSP_RESET
40	DGND3	GND	
41	+5VD3	PWR	
42	RXOUT		NC
43	DGND4	GND	
44	RMODE	MI	Connect to TMODE
45	TMODE	MI	Connect to RMODE
46	EYESYNC	OA	Eye Pattern Test Circuit
47	EYECLK	OA	Eye Pattern Test Circuit
48	EYEXY	OA	Eye Pattern Test Circuit
49	TXDAT		NC
50	TDCLK	OA	DTE Serial Interface
51	$\overline{RLSD}$	OA	DTE Serial Interface
52	$\overline{RDCLK}$	OA	DTE Serial Interface
53	GP0	MI	Connect to EYESYNC
54	XTCLK	IA	DTE Serial Interface
55	DGND5	GND	
56	+5VD4	PWR	
57	TXD	IA	DTE Serial Interface
58	$\overline{DSR}$/RXRQ	OA	DTE Serial/DMA Interface
59	$\overline{RESET}$	IA	Connect to MDP $\overline{POR}$
60	$\overline{READ}$	IA	Host Parallel Interface

Table 7c. MDP Pin Signals - 68-Pin PLCC (Cont'd)

Pin	Signal Label	I/O Type	Interface
61	$\overline{WRITE}$	IA	Host Parallel Interface
62	$\overline{CS}$	IA	Host Parallel Interface
63	RS4	IA	Host Parallel Interface
64	RS3	IA	Host Parallel Interface
65	RS2	IA	Host Parallel Interface
66	RS1	IA	Host Parallel Interface
67	D6	IA/OA	Host Parallel Interface
68	D4	IA/OA	Host Parallel Interface

Notes:

1. I/O Type:
   - MI = Modem interconnect.
   - IA, IB = Digital input.
   - OA, OB, OD = Digital output.
   - I(DA)] = Analog input.
   - O(DD), O(DF) = Analog output.
2. NC = No external connection allowed.
3. VREG on the RC288DPL/VFC must be connected to GND through 0.1 µF capacitor; VREG on the RC288DPi/VFC can be connected to GND through 0.1 µF capacitor or can be left open (NC).

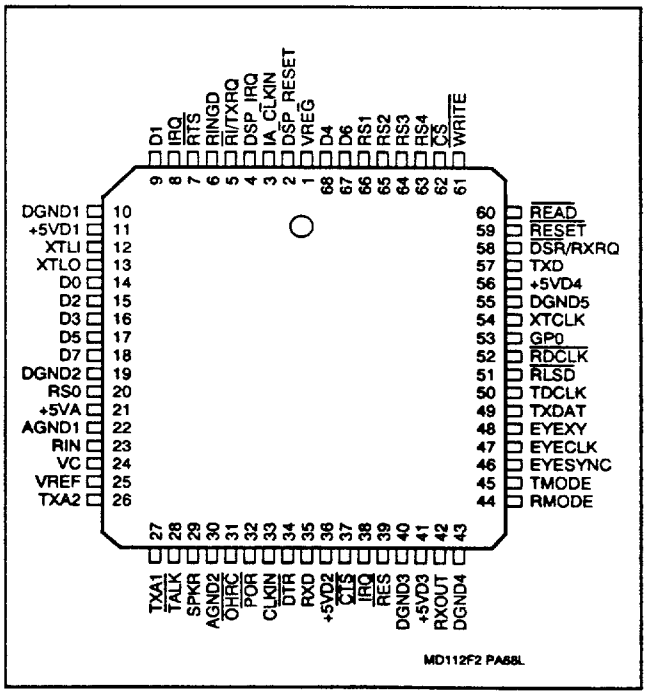


Figure 6b. MDP Pin Signals- 68-Pin PLCC

Table 8. MCU Signal Definitions

Label	I/O Type	Signal Name/Description
		MCU SYSTEM
XTLI, XTLO	IE, OE	**MCU Crystal/Clock In and Crystal Out.** Connect to an external crystal circuit consisting of a 14.7456 MHz crystal and a capacitance network.
$\overline{RES}$	IC	**MCU Reset.** The active low $\overline{RES}$ input resets the MCU logic, and restores the saved configuration from NVRAM, or returns the modem to the factory default values if NVRAM is not present. For serial interface, the $\overline{RES}$ input is typically connected to MDP $\overline{POR}$ pin and a reset circuit. For parallel interface, the $\overline{RES}$ input is connected to the MDP $\overline{POR}$ pin and the host bus RESET line through an inverter.
$\overline{DPIRQ}$	IA	**MDP Interrupt Request.** Connect to the MDP IRQ output.
$\overline{DPRXD}$	IA	**MDP Received Data.** Connect to the MDP MRXD output.
VCC1, VCC2	PWR	**+ 5V Digital Supply.** +5V ± 5%.
GND1-GND8	GND	**Digital Ground.** Connect to ground.
		LINE INTERFACE
$\overline{RLY1}$	OA	**Relay 1 Control** ($\overline{OH}$). The active low $\overline{RLY1}$ output can be used to control the normally open off-hook relay.
$\overline{RLY2}$	OA	**Relay 2 Control** ($\overline{PULSE}$). The active low $\overline{RLY2}$ output can be used to control the normally open pulse dial relay.
$\overline{RLY3}$	OA	**Relay 3 Control** ($\overline{MUTE}$, $\overline{A/A1}$). The active low $\overline{RLY3}$ output can be used to control the normally open mute relay or the normally open key telephone hold indicator (A/A1) relay.
$\overline{RLY4}$	OA	**Relay 4 Control** ($\overline{EARTH}$, $\overline{T/DRLY}$). The active low $\overline{RLY4}$ output can be used to control the normally open earthing relay or the normally closed talk/data relay.
LCS	IA	**Line Current Sense.** LCS is an active high input that indicates an handset off-hook status.
RINGD	IA	**Ring Frequency.** A high-going edge on the RINGD input initiates an internal ring frequency measurement. The RINGD input from an external ring detect circuit is monitored to determine when to wake up from sleep or stop mode. The RINGD input is typically connected to the output of an optoisolator or equivalent. The idle state (no ringing) output of the ring detect circuit should be low.
IDCLK	OA	**Country Identifier Clock.** IDCLK is an output clock to the country identifier shift register.
IDID	IA	**Country Identifier Code.** IDID is an input serial stream from the country identifier shift register.
		NVRAM INTERFACE
NVMCLK	OA	**NVRAM Clock.** NVMCLK output high enables the NVRAM.
NVMDATA	IA/OA	**NVRAM Data.** The NVMDATA pin supplies a serial data interface to the NVRAM.
		EXTERNAL MEMORY BUS INTERFACE
A0-A15	OA	**Address Lines 0-15.** A0-A15 are the external memory bus address lines.
A16	OA	**Address Line 16.** A16 is a bank select line.
D0-D7	IA/OA	**Data Line 0-7.** D0-D7 are the external memory bus data lines.
$\overline{READ}$	OA	**Read Enable.** $\overline{READ}$ output low enables data transfer from the selected device to the D0-D7 lines.
$\overline{WRITE}$	OA	**Write Enable.** $\overline{WRITE}$ output low enables data transfer from the D0-D7 lines to the selected device.
$\overline{DPSEL}$	OA	**Modem Data Pump Select.** $\overline{DPSEL}$ output low selects the MDP.
$\overline{RAMSEL}$	OA	**RAM Select.** $\overline{RAMSEL}$ output low selects the external RAM.
$\overline{ROMSEL}$	OA	**ROM Select.** $\overline{ROMSEL}$ output low selects the external 64k/128k-byte ROM.
$\overline{INXSEL}$	OA	**Input Buffer Select.** $\overline{INXSEL}$ output low and A0 high select external input buffer 1. $\overline{INXSEL}$ output low and a low from A0 NANDed with $\overline{WRITE}$ select external input buffer 2. $\overline{INXSEL}$ output low clocked by $\overline{WRITE}$ select the external latch. (Serial interface selected only.)

Table 8. MCU Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
		V.24 (EIA-232-D) SERIAL INTERFACE (SERIAL INTERFACE SELECTED)
		The serial interface signals correspond functionally to V.24/EIA-232-D signals. The signals levels are TTL compatible and are inverted from V.24/EIA-232-D levels.
$\overline{TXD}$	IA	**Transmitted Data (EIA BA/CCITT CT103).** The DTE uses the $\overline{TXD}$ line to send data to the modem for transmission over the telephone line or to transmit commands to the modem.
$\overline{RXD}$	OA	**Received Data (EIA BB/CCITT CT 104).** The modem uses the $\overline{RXD}$ line to send data received from the telephone line to the DTE and to send modem responses to the DTE. During command mode, $\overline{RXD}$ data represents the modem responses to the DTE.
$\overline{CTS}$	OA	**Clear To Send (EIA CB/CCITT CT106).** The $\overline{CTS}$ output informs the DTE when the modem is ready to accept data from the DTE. In asynchronous operation, $\overline{CTS}$ is always ON (low) indicating that the modem can accept data at any time. In error correction or normal mode, $\overline{CTS}$ is also ON unless RTS/CTS flow control is selected by the &Kn command. In synchronous operation, the modem also holds $\overline{CTS}$ ON during asynchronous command state. The modem turns $\overline{CTS}$ OFF immediately upon going off-hook and holds $\overline{CTS}$ OFF until both $\overline{DSR}$ and $\overline{RLSD}$ are ON and the modem is ready to transmit and receive synchronous data. The modem can also be commanded by the &Rn command to turn $\overline{CTS}$ ON in response to an $\overline{RTS}$ OFF-to-ON transition.
$\overline{DSR}$	OA	**Data Set Ready (EIA CC/CCITT CT107).** $\overline{DSR}$ indicates modem status to the DTE. $\overline{DSR}$ OFF (high) indicates that the DTE is to disregard all signals appearing on the interchange circuits except Ring Indicator ($\overline{RI}$). $\overline{DSR}$ output is controlled by the AT&Sn command.
$\overline{RLSD}$	OA	**Received Line Signal Detector (EIA CF/CCITT CT109).** When AT&C0 command is not in effect, $\overline{RLSD}$ output is ON when a carrier is detected on the telephone line or OFF when carrier is not detected.
$\overline{TM}$	OA	**Test Mode Indicate (EIA TM/CCITT CT142).** The $\overline{TM}$ output indicates the modem is in test mode (low) or in any other mode (high).
$\overline{RI}$	OA	**Ring Indicator (EIA CE/CCITT CT125).** $\overline{RI}$ output ON (low) indicates the presence of an ON segment of a ring signal on the telephone line.
$\overline{DRSOUT}$	OA	**Data Signalling Rate Indicator (EIA CI/CCITT CT112).** $\overline{DRSOUT}$ is ON (low) when the modem desires or is engaged in the high speed (2400 bps or higher) mode. $\overline{DRSOUT}$ is OFF (high) otherwise.
$\overline{DTR}$	IA	**Data Terminal Ready (EIA CD/CCITT CT108).** The $\overline{DTR}$ input is turned ON (low) by the DTE when the DTE is ready to transmit or receive data. $\overline{DTR}$ ON prepares the modem to be connected to the telephone line, and maintains the connection established by the DTE (manual answering) or internally (automatic answering). $\overline{DTR}$ OFF places the modem in the disconnect state under control of the &Dn and &Qn commands.
$\overline{RTS}$	IA	**Request To Send (EIA CA/CCITT CT105).** The $\overline{RTS}$ input informs the modem when the DTE is ready to accept data from the modem. In asynchronous operation, $\overline{RTS}$ is always ON (low) indicating that the modem can send data at any time. In error correction or normal mode, $\overline{RTS}$ is also ON unless RTS/CTS flow control is selected by the &Kn command. In synchronous on-line operation, the modem can be commanded by the &Rn command to ignor $\overline{RTS}$ or respond to $\overline{RTS}$ by turning on $\overline{CTS}$ after the delay specified by Register S26. In the command state, the modem ignors $\overline{RTS}$.
$\overline{RDL}$	IA	**Remote Digital Loop Select (EIA RL/CCITT CT140).** $\overline{RDL}$ input low activates remote digital loop request. The loop is executed at the speed for which the modem is currently configured.
$\overline{AL}$	IA	**Analog Loop (EIA LL/CCITT CT141).** The $\overline{AL}$ input low causes the modem to assume the analog loop test mode.
$\overline{DRSIN}$	IA	**Data Signalling Rate Select (EIA CI/CCITT CT111).** This signal, relevant only in Central Europe, applies only to V.22 bis and V.22 modes. $\overline{DRSIN}$ ON (low) will result in a 2400 bps connection. $\overline{DRSIN}$ OFF (high) will force a 1200 bps connection, or will result in a fallback from 2400 bps to 1200 bps if already on-line.

Table 8. MCU Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
		LED INDICATOR CIRCUIT INTERFACE (SERIAL INTERFACE SELECTED)
$\overline{\text{AAIND}}$	OA	**Auto Answer Indicator.** $\overline{\text{AAIND}}$ output ON (low) corresponds to the indicator on. $\overline{\text{AAIND}}$ output is active when modem will answer the ring automatically (ATS0 command ≠ 0).
$\overline{\text{TMIND}}$	OA	**Test Mode Indicator.** $\overline{\text{TMIND}}$ output ON (low) corresponds to the indicator on. $\overline{\text{TMIND}}$ output pulses (LED flashes) when modem is in test mode and if an error is detected.
$\overline{\text{DTRIND}}$	OA	**DTR Indicator.** $\overline{\text{DTRIND}}$ output ON (low) corresponds to the indicator on. The $\overline{\text{DTRIND}}$ state reflects the $\overline{\text{DTR}}$ output state except when the &D0 command is active, in which case $\overline{\text{DTRIND}}$ is low.
		AUXILIARY CIRCUITS (SERIAL INTERFACE SELECTED)
$\overline{\text{CLKSTOP}}$	OA	**Clock Stop.** Active low output that can be used to force the $\overline{\text{RXCLK}}$ and $\overline{\text{TXCLK}}$ outputs high to the DTE.
		RESET SAMPLED DIRECT SWITCH INPUT TO MCU
		This switch input can be read upon power up or after a warm reset.
PTTEN	IA	**PTT Test Enable.** The PTTEN input enables (high) or disables (low) the use of the PTT test commands. PTTEN is checked only for countries which do not permit the use of the %TT command at the approval site (e.g., Germany).
		EXT[illegible]N [illegible] E SELECTED)
		Switch inputs are available via external bu[illegible] as enabled by ConfigurACE. These inputs are sampled onto the data bus, typically via a 74HCT541 three-state buffer (see INXSEL). The data bus bit number for each signal is defined below.
SWTCHEN	Bus	**Switch Enable.** The SWTCHEN input (bit 0) enables (high) or disables (low) use of external switch inputs to invoke AT commands and S Register functions rather than default values from ROM.
CLKSEL1/2	Bus	**Clock Select 1 and 2.** The CLKSEL1 and CLKSEL2 inputs (bits 1 and 2, respectively) select async/sync operation and the clock source for synchronous operation. The selectable options are:

Mode/Clock Source	CLKSEL1	CLKSEL2
Asynchronous	L	L
Synchronous with Internal clock	L	H
Synchronous with External clock	H	L
Synchronous with Slave clock	H	H

DSRDTROV	Bus	**DSR/DTR Override.** The DSRDTROV input (bit 3) enables (high) or disables (low) override of DSR and DTR from the EIA (V.24) interface.
AT/V25B	Bus	**AT/V.25 bis Commands Select.** The AT/V25B input (bit 5) selects V.25 bis (high) or AT command (low) operation.

Table 8. MCU Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
		EXTERNAL BUFFER 2 INPUTS TO MCU (SERIAL INTERFACE SELECTED) Four momentary switch (TD, TEST, OA, and SEL) and one discrete switch (O/A) inputs are available via external buffer 2 as enabled by ConfigurACE. These inputs are sampled onto the data bus, typically via a 74HCT541 three-state buffer (see INXSEL). The momentary switch inputs are asserted upon the ON-to-OFF transition. The data bus bit number for each signal is defined below.
TD	Bus	**Data/Talk.** TD input (bit 0) operation depends upon the SELIND, TDIND, and TSTIND outputs. a. If SELIND is ON, the TD input ON-to-OFF transition steps the selected directory to the next entry (see SELIND output). b. If SELIND is OFF and TDIND is ON, the TD input ON-to-OFF transition will cause the modem to disconnect from the line. c. If SELIND is OFF and TDIND is OFF, the telephone set may be used for voice communication. If a directory entry has been selected, TD ON-to-OFF transition will cause the modem to dial the telephone number from the selected directory entry. If no directory entry has been selected, the modem will go off-hook and attempt a handshake depending upon the OAIND output state.
TEST	Bus	**Test.** TEST input (bit 1) operation depends upon the SELIND, TDIND, and TSTIND outputs. a. If SELIND is ON, the TEST input is not operative. b. If SELIND is OFF and TSTIND is ON, the modem is in a test mode. The TEST ON-to-OFF transition will cause the modem to exit the test mode and to turn TSTIND OFF. c. If SELIND is OFF, TSTIND is OFF, and TDIND is OFF, the TEST ON-to-OFF transition will cause the modem to enter local analog loopback (V.54 loop 3) and to turn the TSTIND ON. d. If SELIND is OFF, TSTIND is OFF, and TDIND is ON, the TEST ON-to-OFF transition will cause the modem to establish remote digital loopback (V.54 loop 2) in the remote modem and turn TSTIND ON. If the remote end does not accept the RDL then TSTIND will not be turned ON and the modem will remain in data mode.
OA	Bus	**Answer/Originate.** If SELIND is OFF, the OA input (bit 2) ON-to-OFF transition will toggle the OAIND output to answer (ON) or originate (OFF). If SELIND is ON, the OA input is not operative.
SEL	Bus	**Select.** The SEL ON-to-OFF transition will toggle the SELIND output to ON or OFF.
O/A	Bus	**Originate/Answer.** The O/A input selects answer (ON) or originate (OFF) mode.
		EXTERNAL LATCHED OUTPUTS FROM MCU (SERIAL INTERFACE SELECTED) Outputs are available via an external output latch as enabled by ConfigurACE. These outputs are extracted from the data bus, typically by a 74HCT377 data latch (see INXSEL). The data bus bit number for each signal is defined below.
SELIND	Bus	**Select Indicate.** SELIND output (bit 3) toggles in response to the SEL input ON-to-OFF transition to reflect the directory entry (SELIND ON) or normal (SELIND OFF) operation. If SELIND is ON, the TD input ON-to-OFF transition steps the selected directory to the next entry. The selected entry is indicated by the TDIND, OAIND, and TSTIND outputs as follows: **TDIND / OAIND / TSTIND / Selection** 0 / 0 / 0 / No selection 0 / 0 / 1 / Entry 1 0 / 1 / 0 / Entry 2 . . . 1 / 1 / 1 / Entry 7
TDIND	Bus	**Talk/Data Indicate.** When SELIND is OFF, the TDIND output (bit 0) reflects the state of the off-hook relay. When SELIND is ON, the TDIND output reflects the state of bit 2 of the directory entry selection (see SELIND output).

Table 8. MCU Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
TSTIND	Bus	**Test Indicate.** When SELIND is OFF, the TSTIND output (bit 1) is ON during modem test (see TEST input). When SELIND is ON, the TSTIND output reflects the state of bit 0 of the directory entry selection (see SELIND output).
OAIND	Bus	**Originate/Answer Indicate.** When SELIND is OFF, OAIND output (bit 2) reflect the originate (OFF) or answer (ON) state when connected or toggles to originate (OFF) or answer (ON) in response to the OA input ON-to-OFF transition. When SELIND is ON, the OAIND output reflects the state of bit 1 of the directory entry selection (see SELIND output).
COMIND	Bus	**Compressed Indicate.** COMIND output (bit 4) indicates data compression (MNP 5, V.42 bis) is in effect (high) or is not in effect (low).
RELIND	Bus	**Reliable Connection Indicate.** RELIND output (bit 5) indicates that a reliable connection (MNP, LAPM) is in effect (high) or a non-error-connected connection exists or the modem is off-line (low).
		PARALLEL HOST INTERFACE (PARALLEL INTERFACE SELECTED)
		The parallel interface emulates a 16450/16550A UART interface. The parallel interface is compatible with communications software designed to operate with a 16450/16550A interface.
HA0-HA2	IA	**Host Bus Address Lines 0-2.** During a host read or write operation, HA0-HA2 select an internal MCU 16450/16550A-compatible register.
HD0-HD7	IA/OA	**Host Bus Data Lines 0-7.** HD0-HD7 are comprised of eight three-state input/output lines providing bidirectional communication between the host and the MCU. Data, control words, and status information are transferred through HD0-HD7.
$\overline{HCS}$	IA	**Host Bus Chip Select.** $\overline{HCS}$ input low selects the host bus.
$\overline{HRD}$	IA	**Host Bus Read.** $\overline{HRD}$ is an active low, read control input. When $\overline{HCS}$ is low, $\overline{HRD}$ low allows the host to read status information or data from a selected MCU register.
$\overline{HWT}$	IA	**Host Bus Write.** $\overline{HWT}$ is an active low, write control input. When $\overline{HCS}$ is low, $\overline{HWT}$ low allows the host to write data or control words into a selected MCU register.
HINT	OA	**Host Bus Interrupt.** HINT output is set high when the receiver error flag, received data available, transmitter holding register empty, or modem status interrupt has an active high condition. HINT is reset low upon the appropriate interrupt service or master reset operation.
$\overline{TXACK}$	IA	**Host Transmit Acknowledge.** $\overline{TXACK}$ is an active low transmit acknowledge input acknowledging that the DMA controller received the Transmit Ready (TXRDY) data transfer request output.
$\overline{RXACK}$	IA	**Host Receive Acknowledge.** $\overline{RXACK}$ is an active low receive acknowledge input acknowledging that the DMA controller received the Receiver Ready (RXRDY) data transfer request output.
TXRDY	OA	**Transmitter Ready.** TXRDY is an active high transmit ready output in the FIFO mode (FCR0 = 1). When asserted, TXRDY indicates that the TX FIFO is not full, i.e., the TX FIFO can accept data to be transmitted.
RXRDY	OA	**Receiver Ready.** RXRDY is an active high receiver ready output in the FIFO mode (FCR0 = 1). When asserted, RXRDY indicates that the RX FIFO is not empty, i.e., the RX FIFO has received data ready for transfer.
		STOP MODE CONTROL
$\overline{STPMODE}$	IA	**Stop Mode.** $\overline{STPMODE}$ low causes the modem to enter the stop mode immediately after terminating a line connection if connected, terminating any test in process, and allowing any data in the receive buffer to clear. $\overline{STPMODE}$ must be high before the modem can attain normal operation after power turn-on, reset, or wake-up from sleep or stop mode.

Table 9. MDP Signal Definitions

Label	I/O Type	Signal/Definition
		OVERHEAD SIGNALS
XTLI, XTLO	I, O	**Crystal In and Crystal Out.** Connect to an external crystal circuit consisting of a crystal, three capacitors, and an inductor, or to a square wave generator/sine wave oscillator. The crystal frequency is 36.288 MHz for the RC288DPL/VFC, 32.256 MHz for the RC240DPL/VFC, or 24.192 MHz for the RC192DPL/VFC.
$\overline{POR}$	IA	**Power-on Reset.** Connect to MCU $\overline{RES}$.
$\overline{RESET}$	IA	**Reset.** Connect to MDP $\overline{POR}$.
+5VD	PWR	**+ 5V Digital Supply.** +5V ± 5%.
+5VA	PWR	**+ 5V Analog Supply.** +5V ± 5%.
DGND	GND	**Digital Ground.** Connect to ground.
AGND	GND	**Analog Ground.** Connect to ground.
VC	MI	**Low Voltage Reference.** Connect to analog ground through 10 µF (polarized, + terminal to VC) and 0.1 µF (ceramic) in parallel.
VREF	MI	**High Voltage Reference.** Connect to VC through 10 µF (polarized, + terminal to VREF) and 0.1 µF (ceramic) in parallel.
VREG	MI	**Voltage Regulator.** Connect to digital ground through 0.1 µF.
		SERIAL INTERFACE (SERIAL INTERFACE SELECTED)
$\overline{TXD}$	IA	**Transmitted Data.** The MDP obtains serial data to be transmitted from the DTE on the TXD input.
$\overline{RXD}$	OA	**Received Data.** The MDP presents received serial data to the DTE on the RXD output.
$\overline{TDCLK}$	OA	**Transmit Data Clock.** The modem outputs a synchronous Transmit Data Clock ($\overline{TDCLK}$) for USRT timing. The $\overline{TDCLK}$ frequency is the data rate (±0.01%) with a duty cycle of 50 ±1%.
$\overline{XTCLK}$	IA	**External Transmit Clock.** In synchronous communication, an external transmit data clock can be connected to the MDP $\overline{XTCLK}$ input. The clock supplied at $\overline{XTCLK}$ must exhibit the same characteristics as $\overline{TDCLK}$.
$\overline{RDCLK}$	OA	**Receive Data Clock.** The modem outputs a synchronous Receive Data Clock ($\overline{RDCLK}$) for USRT timing.
$\overline{RTS}$	IA	**Request to Send.** Not used; pull up to VCC through 10k Ω.
$\overline{DTR}$	IA	**Data Terminal Ready.** Not used; pull up to VCC through 10k Ω.
$\overline{CTS}$	OA	**Clear to Send.** Not used; leave open.
$\overline{DSR}$	OA	**Data Set Ready**. Not used; leave open.
		INDICATOR SIGNALS (SERIAL INTERFACE SELECTED)
$\overline{RLSDIND}$	OA	**Received Line Signal Detector.** $\overline{RLSDIND}$ active indicates that energy above the receive level threshold is present on the receiver input, and that the energy is not a training sequence.
		SERIAL/INDICATOR INTERFACE (PARALLEL INTERFACE SELECTED)
$\overline{TXD}$	IA	**Transmitted Data.** Not used; pull up to VCC through 10k Ω.
$\overline{RXD}$	OA	**Received Data.** Not used; leave open.
$\overline{TDCLK}$	OA	**Transmit Data Clock.** Not used; leave open.
$\overline{XTCLK}$	IA	**External Transmit Clock.** Not used; leave open.
$\overline{RDCLK}$	OA	**Receive Data Clock.** Not used; leave open.
$\overline{RLSDIND}$	OA	**Received Line Signal Detector.** Not used, leave open.
$\overline{RTS}$	IA	**Request to Send.** Not used; pull up to VCC through 10k Ω.
$\overline{DTR}$	IA	**Data Terminal Ready.** Not used; pull up to VCC through 10k Ω.
$\overline{CTS}$	OA	**Clear to Send.** Not used; leave open.
$\overline{DSR}$	OA	**Data Set Ready**. Not used; leave open.

Table 9. MDP Signal Definitions (Cont'd)

Label	I/O Type	Signal/Definition
		MCU INTERFACE
D0–D7	IA/OB	**Data Lines.** Connect to the MCU D0-D7, respectively.
RS0–RS4	IA	**Register Select Lines.** Connect to the MCU A0–A4, respectively.
$\overline{CS}$	IA	**Chip Select.** Connect to MCU $\overline{DPSEL}$ output.
$\overline{READ}$	IA	**Read Enable.** Connect to MCU $\overline{READ}$.
$\overline{WRITE}$	IA	**Write Enable.** Connect to MCU $\overline{WRITE}$.
IRQ	OA	**Interrupt Request.** Connect to MCU $\overline{DPIRQ}$.
		LINE INTERFACE
TXA1, TXA2	O(DF)	**Transmit Analog 1 and 2.** The TXA1 and TXA2 outputs are differential outputs 180 degrees out of phase with each other.
RIN	I(DA)	**Receive Analog.** RIN is a single-ended receive data input from the external hybrid in the telephone line interface circuit.
RINGD	IA	**Ring Frequency Detect.** A high-going edge on the RINGD input initiates an internal ring frequency measurement. The RINGD input is typically connected to the output of an optoisolator or equivalent. The idle state (no ringing) output of the ring detect circuit should be low.
CALLID	OD	**Caller ID Relay Control (MDP $\overline{OHRC}$).** Typically, the MDP CALLID output is connected to the normally open Caller ID relay. When the modem detects a Calling Number Delivery (CND) message, the CALLID output is asserted to close the CALLID relay in order to AC couple the CND information to the modem RIN input (without closing the off-hook relay and allowing loop current flow which would indicate an off-hook condition). The MDP CALLID output can each directly drive a +5V reed relay coil with a minimum resistance of 360 ohms and having a must-operate voltage of no greater than 4.0 Vdc. A clamp diode, such as a 1N4148, should be installed across the relay coil. An external transistor, such as an MPSA20, can be used to drive heavier loads (e.g., electro-mechanical relays).
		SPEAKER INTERFACE
SPKR	O(DF)	**Speaker Analog Output.** The SPKR output reflects the received analog input signal. The SPKR is controlled by the ATMn command. The SPKR output can drive an impedance as low as 300 ohms. In a typical application, the SPKR output is an input to an external LM386 audio power amplifier.
		DIAGNOSTIC SIGNALS Three signals provide the timing and data necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By observing this constellation, common line disturbances can usually be identified.
EYEXY	OA	**Serial Eye Pattern X/Y Output.** EYEXY is a serial output containing two 15-bit diagnostic words (EYEX and EYEY) for display on the oscilloscope X axis (EYEX) and Y axis (EYEY). EYEX is the first word clocked out; EYEY follows. Each word has 8-bits of significance. Each 15-bit data word is shifted out most significant bit first with the seven most significant bits set to zero. EYEXY is clocked by the rising edge of $\overline{EYECLK}$. This serial digital data must be converted to parallel digital form by a serial-to-parallel converter and then to analog form by two digital-to-analog (D/A) converters.
$\overline{EYECLK}$	OA	**Serial Eye Pattern Clock.** $\overline{EYECLK}$ is a 288 kHz output clock for use by the serial-to-parallel converters. The low-to-high transitions of RDCLK coincide with the low-to-high transitions of $\overline{EYECLK}$. $\overline{EYECLK}$, therefore, can be used as a receiver multiplexer clock.
EYESYNC	OA	**Serial Eye Pattern Strobe.** EYESYNC is a strobe for loading the D/A converters.

Table 10. Digital Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions[1]
Input High Voltage	V_{IH}				Vdc	
Type IA		2.0	–	V_{CC}		
Type IC		0.7 V_{CC}	–	V_{CC} + 0.3		
Type IE		–	4.0	–		Note 2.
Input Low Voltage	V_{IL}				Vdc	
Type IA and 1C		–0.3		0.8		
Type IE		–	1.0	–		Note 2.
Input Leakage Current	I_{IN}				µAdc	V_{IN} = 0 to V_{CC}
$\overline{RES}$ and PD0-PD7		–	–	±2.5		
XTLI		–	–	±10		
$\overline{NMI}$ and $\overline{TST}$		–	–	±100		
Output High Voltage	V_{OH}				Vdc	
Type OA and OB		2.4	–	–		I_{LOAD} = – 100 µA
Type OD		–	–	V_{CC}		I_{LOAD} = 0 mA
Type OE						Note 3.
Output Low Voltage	V_{OL}				Vdc	
Type OA		–	–	0.4		I_{LOAD} = 1.6 mA
Type OB		–	–	0.4		I_{LOAD} = 0.8 mA
Type OD		–	–	0.75		I_{LOAD} = 15 mA
Three-State (Off) Current	I_{TSI}			±10	µAdc	V_{IN} = 0 V to V_{CC}

Notes:
1. Test Conditions: V_{CC} = 5V ± 5%, T_A = 0°C to 70°C, (unless otherwise stated).
   Output loads: Data bus (D0-D7), address bus (A0-A15), chip selects, $\overline{READ}$, and $\overline{WRITE}$ loads = 70 pF + one TTL load.
   Other = 50 pF + one TTL load.
2. Type IE inputs are centered approximately 2.5 V and swing 1.5 V_{PEAK} in each direction.
3. Type OE outputs provide oscillator feedback when operating with an external crystal.

Table 11. Analog Characteristics

Name	Type	Characteristic	Value
RIN	I (DA)	Input Impedance	> 70K Ω
		Voltage Range	2.5 ±1.6 V
TXA1, TXA2	O (DD)	Minimum Load	300 Ω
		Maximum Capacitive Load	0.01 µF
		Output Impedance	10 Ω
		Output Voltage	2.5 ± 1.6 V
		D.C. Offset	< 200 mV
SPKR	O (DF)	Minimum Load	300 Ω
		Maximum Capacitive Load	0.01 µF
		Output Impedance	10 Ω
		Output Voltage	2.5 ± 1.6 V
		D.C. Offset	< 20 mV

Table 12. Current and Power Requirements

Mode	Current (I_D)			Power (P_D)			Notes
	Typical Current @ 25°C (mA)	Maximum Current @ 0°C (mA)	Maximum Current @ -40°C[1] (mA)	Typical Power @ 25°C (mW)	Maximum Power @ 0°C (mW)	Maximum Power @ -40°C[1] (mW)	
MCU -L39							f_{IN} = 14.7456 MHz
Normal mode	34	41	51	170	214	268	
Sleep mode	2.20	2.70	2.80	11.00	14.20	14.70	
Stop mode	0.15	0.20	0.20	0.80	1.10	1.10	
MDP							
Normal mode -RC288DPL/VFC	124	161	198	620	845	1040	f_{IN} = 36.288 MHz
Normal mode -RC240DPL/VFC	108	140	172	540	735	903	f_{IN} = 32.256 MHz
Normal mode -RC192DPL/VFC	86	112	138	430	588	725	f_{IN} = 24.192 MHz
Sleep mode	1.80	2.30	2.90	9.00	12.30	15.10	
Total							
Normal mode -RC288ACL/VFC	158	202	249	790	1059	1308	f_{IN} = 36.288 MHz
Normal mode -RC240ACL/VFC	142	181	223	710	949	1171	f_{IN} = 32.256 MHz
Normal mode -RC192ACL/VFC	120	153	189	600	802	993	f_{IN} = 24.192 MHz
Sleep mode	4.00	5.00	5.70	20.00	26.50	29.80	
Stop mode	1.95	2.50	3.10	9.80	13.40	16.20	

Notes:
1. Maximum power @ -40°C sp[illegible]d only [illegible]ex
2. Test conditions: VCC = 5.0 VDC for typical values, VCC = 5.25 VDC for maximum val[illegible]

Table 13. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	V_{DD}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to +5VD +0.5	V
Operating Temperature Range	T_A		°C
Commercial		-0 to +70	
Extended		-40 to +85	
Storage Temperature Range	T_{STG}	-55 to +125	°C
Analog Inputs	V_{IN}	-0.3 to +5VA + 0.3	V
Voltage Applied to Outputs in High Impedance (Off) State	V_{HZ}	-0.5 to +5VD + 0.5	V
DC Input Clamp Current	I_{IK}	±20	mA
DC Output Clamp Current	I_{OK}	±20	mA
Static Discharge Voltage (25°C)	V_{ESD}	±3000	V
Latch-up Current (25°C)	I_{TRIG}	±200	mA

Table 14. Parallel Interface Registers

Register No.	Register Name	Bit No.							
		7	6	5	4	3	2	1	0
7	Scratch Register (SCR)	Scratch Register							
6	Modem Status Register (MSR)	Data Carrier Detect (DCD)	Ring Indicator (RI)	Data Set Ready (DSR)	Clear to Send (CTS)	Delta Data Carrier Detect (DDCD)	Trailing Edge of Ring Indicator (TERI)	Delta Data Set Ready (DDSR)	Delta Clear to Send (DCTS)
5	Line Status Register (LSR)	RX FIFO Error	Transmitter Empty (TEMT)	Transmitter Buffer Register Empty (THRE)	Break Interrupt (BI)	Framing Error (FE)	Parity Error (PE)	Overrun Error (OE)	Receiver Data Ready (DR)
4	Modem Control Register (MCR)	0	0	0	Local Loopback	Out 2	Out 1	Request to Send (RTS)	Data Terminal Ready (DTR)
3	Line Control Register (LCR)	Divisor Latch Access Bit (DLAB)	Set Break	Stick Parity	Even Parity Select (EPS)	Parity Enable (PEN)	Number of Stop Bits (STB)	Word Length Select Bit 1 (WLS1)	Word Length Select Bit 0 (WLS0)
2	Interrupt Identify Register (IIR) (Read Only)	FIFOs Enabled	FIFOs Enabled	0	0	Pending Interrupt ID Bit 2	Pending Interrupt ID Bit 1	Pending Interrupt ID Bit 0	"0" if Interrupt Pending
2	FIFO Control Register (FCR) (Write Only)	Receiver Trigger MSB	Receiver Trigger LSB	Reserved	Reserved	DMA Mode Select	TX FIFO Reset	RX FIFO Reset	FIFO Enable
1 DLAB = 0	Interrupt Enable Register (IER)	0	0	0	0	Enable Modem Status Interrupt (EDSSI)	Enable Receiver Line Status Interrupt (ELSI)	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Enable Received Data Available Interrupt (ERBFI)
0 DLAB = 0	Transmitter Buffer Register (THR)	Transmitter FIFO Buffer Register (Write Only)							
0 DLAB = 0	Receiver Buffer Register (RBR)	Receiver FIFO Buffer Register (Read Only)							
1 DLAB = 1	Divisor Latch MSB Register (DLM)	Divisor Latch MSB							
0 DLAB = 1	Divisor Latch LSB Register (DLL)	Divisor Latch LSB							