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SSI 32M593A
Three-Phase Delta Motor Speed Controller

July 1990

DESCRIPTION

The SSI 32M593A is a motor speed control IC designed to provide all timing and control functions necessary to start, drive, and brake a 3-phase, 4 or 8 pole brushless DC spindle motor. External Darlington power transistors or external power FETs may be used by the SSI 32M593A to drive the spindle motor.

The motor Hall sensors are directly driven and decoded by the device. The controller is optimized for a 3600 rpm motor using a 2 MHz clock. Motor protection features include jammed platter shutdown, supply and clock fault detection, all of which are indicated by a FAULT signal, and coil over-current detection and control. A LOCK signal is provided to indicate that the motor is at speed. The device's linear control loop controls the power drivers using Pulse Amplitude Modulation.

The SSI 32M593A requires a +12V power supply, and is available in 20-pin DIP or SO packages.

FEATURES

- **3-phase bipolar or unipolar operation**
- **4 or 8-pole operation**
- **3600 rpm speed control using a 2 MHz clock**
- **Highly accurate speed regulation of ±0.037%**
- **At speed indication provided**
- **Active braking function**
- **Output pre-driver for center tap or non-center tap windings**
- **Drives complementary Darlington power transistors or complementary power FETs**
- **Power supply fault protection**
- **Motor over-current protection**
- **Multiple retry on jammed spindle**
- **Single +12 volt power supply**

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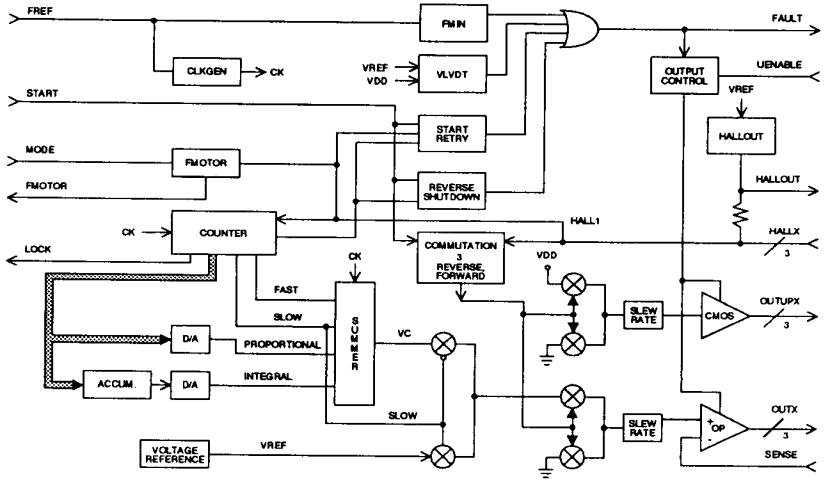
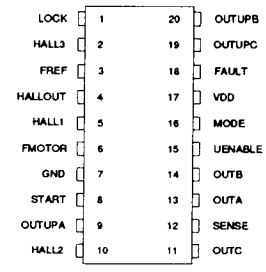
BLOCK DIAGRAM



PIN DIAGRAM



20-PIN DIP or SOL

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 32M593A uses a mix of analog and digital techniques to accomplish speed control. The control signal is generated by analog conversion of a digital speed error term developed by examining the contents of a count-down counter once per motor revolution. The sign and magnitude of the remainder controls the amplitude of a correction signal applied to the motor. Commutation timing, developed from motor generated HALL signals, applies the correction in the proper phase sequence.

The device uses a Pulse Amplitude Modulation (PAM) scheme rather than Pulse Width Modulation (PWM) to avoid the switching transients and torque ripple inherent in PWM.

In operation, the SSI 32M593A is installed in a closed loop control system that maintains the speed of a 3-Phase Brushless DC motor. By monitoring the HALL signal outputs of the motor, a control voltage is developed using both digital and analog techniques. The analog portion of the control loop uses switched capacitor techniques to eliminate the need for any external passive components required for loop compensation. An operation description of the circuit follows.

CONTROL LOOP

Referring to the block diagram, the major sections of the control loop are a 19-stage Counter, Integral and Proportional channels, D/A's and a Summer.

The speed error is determined by examining the contents of the counter once per revolution. The counter is preset once per revolution by an INDEX signal developed from the HALL1 input, at the same time any remainder resulting from a 500 kHz count-down rate is loaded into a latch.

The lower LSB's of the latch, except for the LSB, are used to drive the Proportional D/A while the entire contents of the latch are accumulated to control the Integral Channel. The MSB's of the accumulator drive the Integral D/A.

If the contents of the counter indicate that the speed is outside the linear regulation range (±0.037%), this is decoded as a "FAST" or "SLOW" condition. Under these conditions the Proportional D/A output is driven to either end of its range, as appropriate. Under a slow condition, a fixed reference voltage is supplied to the output drives.

The Summer then outputs a control voltage (VC) consisting of a bias voltage plus or minus the sum of the two D/A outputs.

The Integral and Proportional channels perform several functions related to the operation of the control loop. One function is to control loop stability by maintaining the loop zero at 1 Hz. In operation this translates to the Integral channel responding to major bias point changes while the Proportional channel takes care of minor perturbations to the loop.

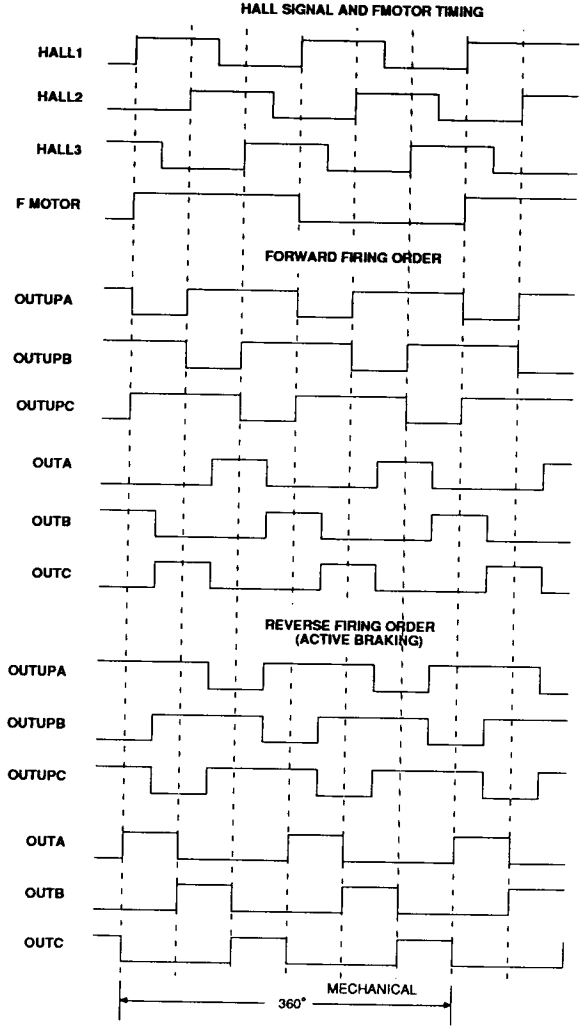
COMMUTATION

The summer output is channeled to the appropriate OUTA, B, C output according to the timing shown in Figure 1. To reduce switching transients, the outputs are slew rate controlled during each transition.

OUTUPA, B, C outputs cycle between approximately VDD in the OFF state and GND in the ON state also according to Figure 1. Again, rise and fall times are controlled during transitions.

MOTOR COIL OVER-CURRENT

Refer to SENSE input description. Sense voltage is generated by current through Re shown in the typical application. The SENSE input threshold limits the maximum coil current.



NOTE: Figure shows commutation of a 4-pole device. 8-pole devices apply same firing order twice per revolution.

FIGURE 1: Commutation Timing Diagram

FUNCTIONAL DESCRIPTION (Continued)

FAULT CONDITIONS

Four conditions cause an active high on the FAULT output pin, also disabling all drivers except as noted :

(1) Low power supply - VDD < Vlvdt

(2) No FREF clock - FREF < Fmin

(3) Stalled motor. If the delay from power onset to a positive HALL index transition or the time interval between successive HALL index transitions is greater than the specified time, the device interprets this delay as a stalled motor, reduces the motor current to zero and performs three retry cycles. If the motor continues to be stalled after three retries, then motor current is reduced to zero until such time as one positive HALL index transition is detected, the START pin is toggled, or power or FREF is removed and re-applied. After the fourth try, FAULT goes high. (See Figure 2.)

(4) Reverse shutdown speed. During active braking (START=0) the HALL sensor's phasing is changed to apply a reverse torque to the motor until the motor speed drops below the reverse shutdown speed at which time the drivers turn off to deny power to the motor and FAULT goes high. If UENABLE is high (non-center tapped motor) the device will perform passive braking after the motor speed drops below the reverse shutdown speed by enabling the lower drivers, OUTX, to dissipate any remaining coil energy. The upper drivers OUTUPX are off. (See Figure 3.)

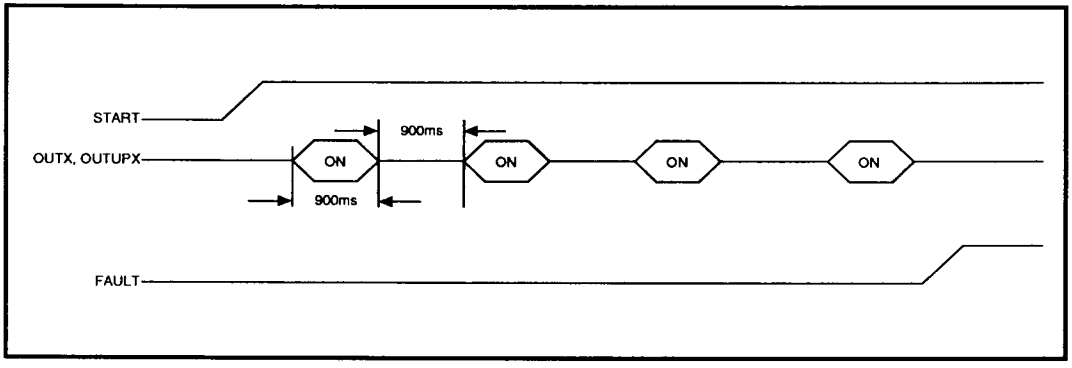


FIGURE 2: Jammed Platter Sequence

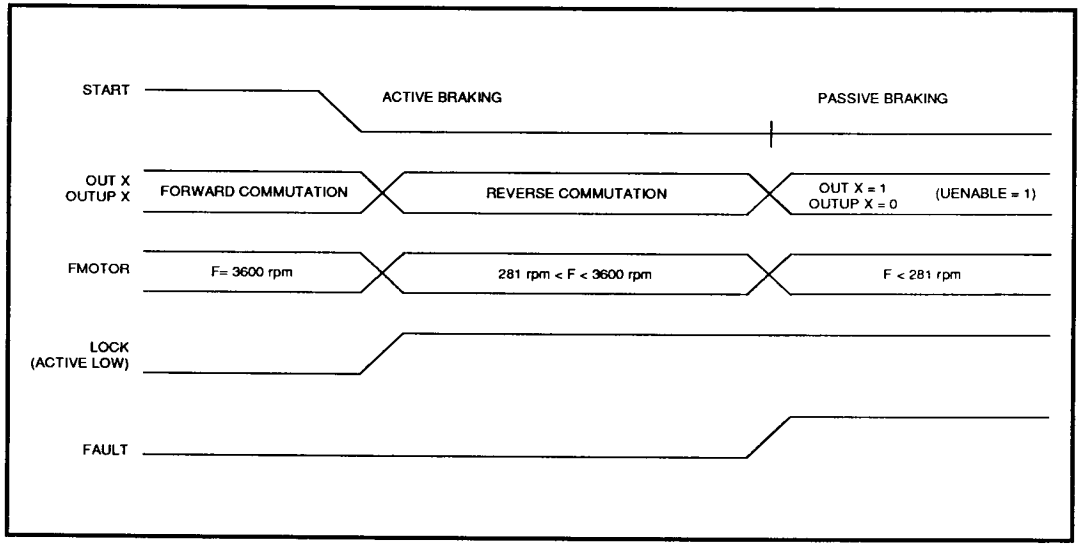


FIGURE 3: Active Braking Sequence

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VDD	I	+12V Power Supply
GND	I	Ground
FREF	I	The reference clock input used to set motor speed and operate circuit blocks.
START	I	A high level on this pin enables the motor. The START input must be low during power-up and should conform to Ts set-up time. Active braking is enabled by applying a logic "zero". During active braking the commutation is changed to apply a reverse torque to the motor until the motor velocity drops below 281 rpm.
MODE	I	Mode Control. When tied high (to VDD) selects 8-pole operation where HALL1 signal is divided by four to generate an index signal. When left open, 4-pole operation is selected and HALL1 is divided by two.
UENABLE	I	Tying UENABLE to GND forces all upper outputs to their off state and disables passive braking. UENABLE must be tied to GND for unipolar center-tapped motors. Tied high or floating, UENABLE = 1 and drives bipolar motors.
FAULT	O	FAULT goes active high indicating low VDD, no FREF, a stalled motor, or motor velocity below the reverse shutdown speed.
LOCK	O	LOCK goes active low when the motor frequency is within a specified lock range.
FMOTOR	O	FMOTOR frequency indicates the motor speed, nominally 3600 rpm. FMOTOR is derived from HALL1.
SENSE	I	Coil Current Sense Input. Senses the coil current and limits the sense voltage to the specified threshold by limiting the voltage from the lower drivers. (OUTX)
HALLOUT	O	Hall Sensor Bias Output. Provides a regulated bias voltage for the hall effect sensors.
HALL1, 2, 3	I	Hall Sensor inputs that determine commutation. The TTL open-collector type motor outputs drive these inputs, which have internal resistor pullups referenced to the HALLOUT bias voltage.
OUTUPA, B, C	O	Upper motor CMOS level outputs that drive either Darlingtons or PFETs.
OUTA, B, C	O	Lower Driver Outputs. These three driver outputs drive external Bipolar or NFET power transistors to control the motor current through the current setting resistor Re. The motor current is V(sense)/Re. During normal operation, the drive voltages are adjusted as necessary to maintain the proper motor speed and drive current.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VDD Supply Voltage	-0.5 to +14	V
Storage Temperature	-65 to +150	°C
Lead Temperature, PDIP (10 sec. soldering)	260	°C
Package Temperature, SO (20 sec. reflow)	215	°C
Input, Output pins	-0.3 to VDD +0.3	V
Inputs and outputs are protected from static charge using built-in ESD and Latchup protection devices.		

ELECTRICAL CHARACTERISTICS (Unless otherwise specified Vlvdt <Vdd<13.2V.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VDD supply voltage		10.8	12	13.2	V
IDD supply current	includes output driver current	-	20	38	mA
PDD power dissipation	IoutA or B, or C = -10 mA IoutupA, or B, or C = 10 mA IHALLOUT = -10 mA	-	240	375	mW
FREF clock frequency		1.998	2	2.002	MHz
TA ambient temperature		0	-	70	°C
TTL Inputs START, FREF, UENABLE					
Vil input low voltage	Iil ≤500 µA	-	-	0.8	V
Vih input high voltage	Iih ≤100 µA	2.0	-	-	V
START set-up time (Ts)	FREF active to START ↑	100			µs
MODE Input					
Vil input low voltage		-	-	0.5	V
Vih input high voltage	Iih ≤500 µA	VDD-.5	-	-	V
HALLX Input					
Vil input low voltage		-	-	0.8	V
Vih input high voltage	External pullup current ≤1.7 mA	3.0	-	-	V
Input Pullup-Pulldown Resistance					
Internal pullup resistance	START, FREF, UENABLE	40	-	-	kΩ
Internal pullup resistance	HALLX inputs	5	-	20	kΩ
Internal pulldown resistance	MODE input	40	-	-	kΩ
Input capacitance	All inputs	-	-	25	pF

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
SENSE Input						
SENSE voltage threshold		if exceeded, driver voltage is limited	0.9	1.0	1.1	V
Input current			-100	-	+100	µA
Open Drain Outputs LOCK, FMOTOR, FAULT						
Vol output low voltage		I_{OL} = 2 mA	-	-	0.5	V
Typical external pullup resistor			-	10	-	kΩ
FAULT Indication						
Vlvdt, low voltage			7.0	-	9.5	V
Fmin, loss of FREF			-	-	100	Hz
Stuck motor, start pulses		drivers on, drivers off	-	0.90	-	sec
Number of start pulses			-	4	-	-
Reverse shutdown speed		START = 0	-	281	-	rpm
LOCK Indication						
Lock range		Measure at FMOTOR, FREF =	3594	3600	3607	rpm
Speed error		2 MHz, 10.8 < V_{DD} < 13.2	-.037		+.037	%
HALL Sensor Interface						
HALLOUT bias voltage		10.8 < VDD < 13.2, Iload = -5 mA	5.0		6.8	V
		10.8 < VDD < 13.2, Iload = -10 mA	5.0			V
Driver Outputs (FHALLX ≥ 100 Hz, V_{lvdt} < VDD ≤ 13.2, CL ≤ 500 pF unless otherwise specified.)						
Slew rate		All driver outputs	150	-	500	V/msec
OUTX	Voh	Iload = -5.0 mA	3.75	-	-	V
	Voh	Iload = -100 µA, 10.8 ≤ V_{DD} ≤ 13.2	8.0	-	-	V
	Vol off state	Iload = 3.4mA, 5.0 ≤ V_{DD} ≤ 13.2	-	-	0.5	V
OUTUPX	Vol	Iload = 10 mA	-	-	3.0	V
	Voh off state	Iload = -5 mA	V_{DD}-0.5	-	-	V
	Voh off state	Iload = -2 mA, 5.0 ≤ VDD ≤ V_{lvdt}	V_{DD}-0.5	-	-	V

APPLICATION INFORMATION

PARAMETER	RECOMMENDED	MIN	NOM	MAX	UNIT
Power Transistors					
Re, Emitter Resistor		.392	.4	.408	Ω
Power Darlington Vbe	Typical device: TIP 125, TIP 120	0.8	-	1.8	V
Power FET Vth	Typical device: IRFT 001	2	-	6	V
Power FET Rds (on)		-	-	0.4	Ω
Power FET BVds		30	-	-	V

Motor Parameters

The SSI 32M593A MSC is optimized for use with a 5 1/4" three-platter Winchester motor. The device will work for a range of motors near this nominal motor. Attempts to use a significantly different motor may require careful choice of a sense resistor for good spin-up and regulation.

KT, Torque Constant Range	(0.015 Nt-m/A nom.)	-10	-	+10	%
J, Inertia Range	(489 x 10^{-6} Nt-m-sec ^{2} nom.)	-33	-	+33	%
KD, Damping Factor Range	(31.8 x 10^{-6} Nt-m/rad/sec nom.)	-33	-	+33	%
Note: $\frac{\text{Motor Frequency (s)}}{\text{Motor Current (s)}} = \frac{KT}{Js + KD}$					

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Control Loop Parameters

The motor control loop consists of counter, logic, and digital-to-analog converters that provide loop time constants. The continuous time transfer function of the on-chip control can be modeled as follows:

$$H(s) = \frac{Vc(s)}{Fm(s)} = \frac{Ki}{s} + Kp$$

Where: Ki = Integral Channel Gain
Kp = Proportional Channel Gain

Vc(s) is the voltage applied to the external sense resistor (Re) by the modulator. By adjusting the value of Re, the gain the motor sees can be adjusted as can the starting current.

Loop Bandwidth	Nominal motor, Re= 0.40Ω		2		Hz
Loop Zero	Ki/Kp		1.0		Hz
Kp, Proportional Channel Gain		0.198	0.213	0.227	V/rad/s
Ki, Integral Channel Gain		1.23	1.33	1.42	V/rad
Start current	Re = 0.40Ω		2.5		Amps
Running current	Re = 0.40Ω		1.5		Amps

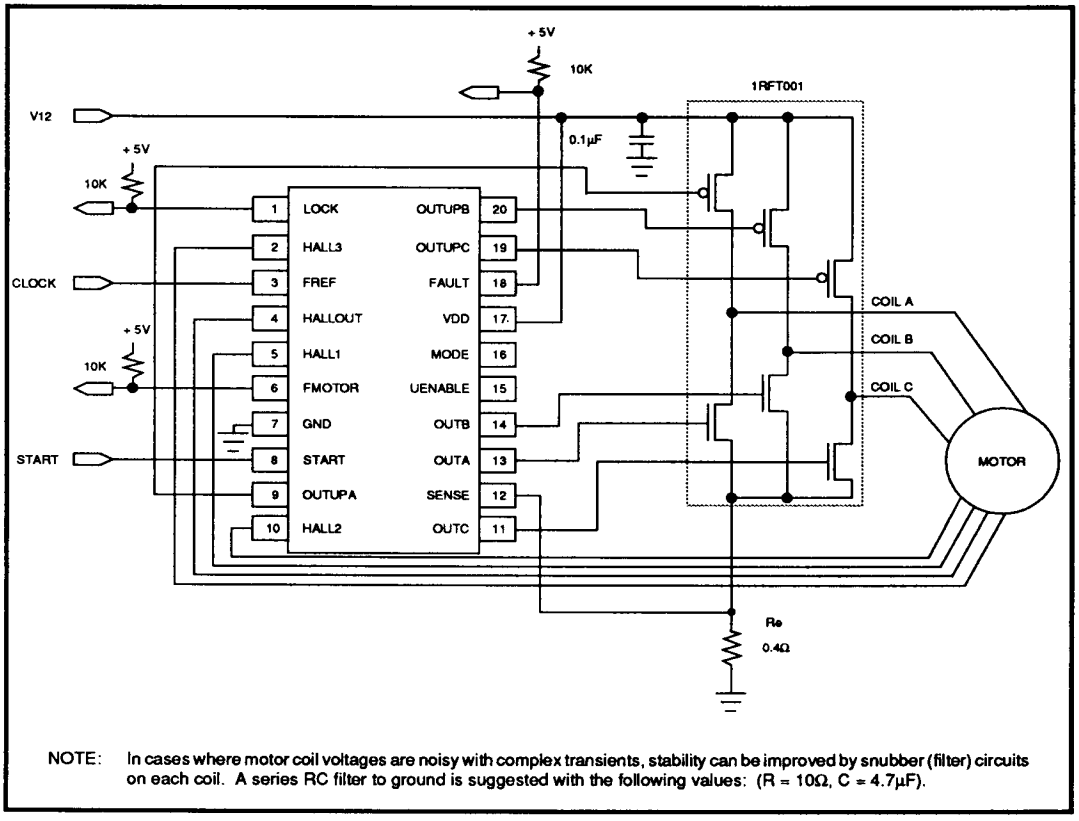

FIGURE 4:Typical Three-Phase, 4-Pole, Bipolar, Non-Center Tapped Motor Using A Power FET Module

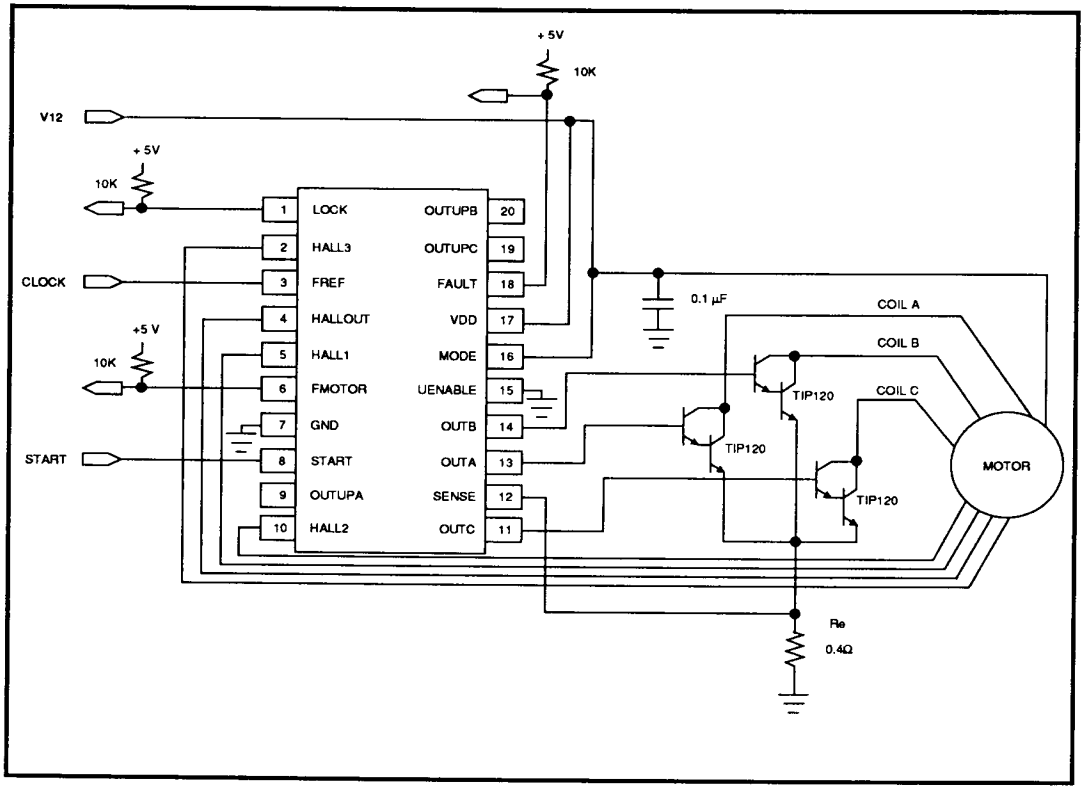

FIGURE 5:Typical Three-Phase, 8-Pole, Unipolar, Center Tapped Motor Using A Power Darlington. UENABLE Must be Tied to GND.

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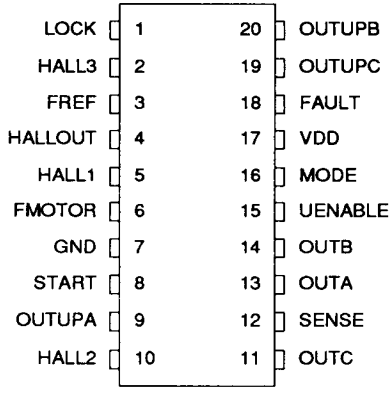
SSI 32M593A
Three-Phase Delta
Motor Speed Controller

PACKAGE PIN DESIGNATIONS

(TOP VIEW)



20-Pin DIP or SOL

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32M593A Three-Phase SOL	32M593A-CL	32M593A-CL
SSI 32M593A Three-Phase PDIP	32M593A-CP	32M593A-CP

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