Philips Components-Signetics

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Status	Product Specification
Memory Products	

82S25 / 3101A / 74S189

64-bit TTL bipolar RAM

DESCRIPTION

This family of Read/Write Random Access Memories is ideal for use in scratch pad and high-speed buffer memory applications.

These products are fully decoded memory arrays with separate input and output lines. They feature PNP inputs and 1 Chip Enable line for ease of memory expansion.

During Write, the outputs of each product assume the logic state defined in the truth table.

Ordering information can be found on the following page.

The 82S25 and 74S189 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information, consult the Signetics Military Data Handbook.

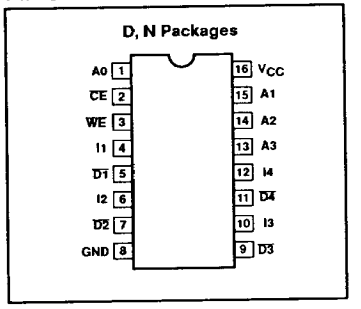
FEATURES

- Output access time:
  - N82S25: 50ns max
  - N3101A: 35ns max
  - N74S189: 35ns max
- Power dissipation: 6.25mW/bit, typ
- Input loading: -100μA max
- On-chip address decoding
- One Chip Enable input
- Output options:
  - N82S25: Open-Collector
  - N3101A: Open-Collector
  - N74S189: 3-State
- Schottky clamped
- TTL compatible

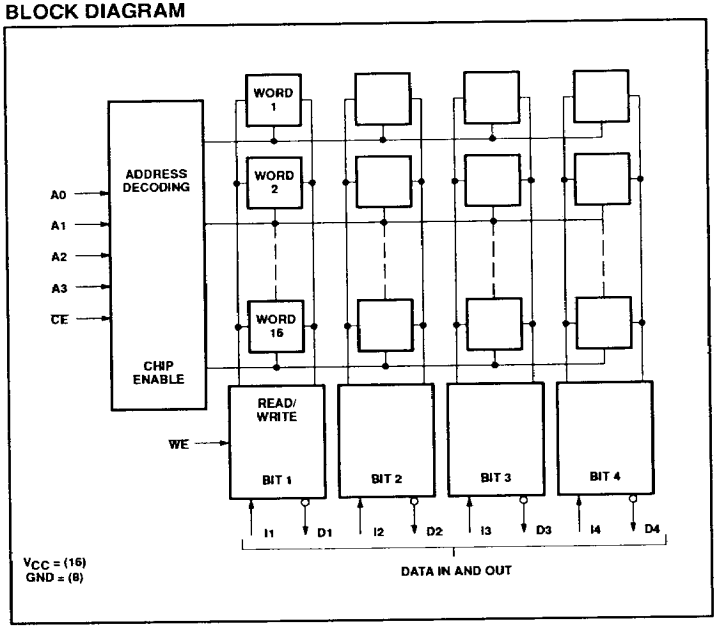
APPLICATIONS

- Scratch pad memory
- Buffer memory
- Push down stacks
- Control store

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Plastic Dual-In-Line 300mil-wide	N82S25 N, N3101A N, N74S189 N
16-Pin Plastic Small Outline 300mil-wide	N82S25 D, N3101A D, N74S189 D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OH}	Output voltage High	+5.5	V_{DC}
T_{amb}	Operating temperature range	0 to +75	°C
T_{stg}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
Input voltage[1]						
V_{IL}	Low	V_{CC} = 4.75V			0.8	V
V_{IH}	High	V_{CC} = 5.25V	2.0			V
V_{IC}	Clamp[4]	I_{IN} = -12mA, V_{CC} = 4.75V			-1.2	V
Output voltage[1]						
		$\overline{CE}$ = Low				
V_{OL}	Low[2,3]	I_{OUT} = 16mA, V_{CC} = 4.75V			0.45	V
V_{OH}	High (74S189)	I_{OUT} = -2.0mA	2.4			V
Input current[5]						
I_{IL}	Low	V_{IN} = 0.45V			-100	µA
I_{IH}	High	V_{IN} = 5.5V			10	µA
Output current[5]						
I_{OLK}	Leakage	$\overline{CE}$ = High, V_{OUT} = 5.5V, V_{CC} = 4.75V			100	µA
I_{OS}	Short circuit (74S189)	$\overline{CE}$ = Low, V_{OUT} = 0V			-100	mA
I_{OZ}	Hi-Z (74S189)	$2.4 \geq V_{OUT} \geq 0.4V$			±50	mA
Supply current[6]						
I_{CC}	82S25	V_{CC} = 5.25V			105	mA
	3101A	V_{CC} = 5.25V			105	mA
	74S189	V_{CC} = 5.25V			110	mA
Capacitance						
		V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V, $\overline{CE}$ = High		8		pF

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Output sink current is supplied through a resistor to V_{CC}.
3. All sense outputs in Low state.
4. Test each input one at a time.
5. Positive current is defined as into the terminal referenced.
6. I_{CC} is measured with the Write Enable and Memory Enable inputs grounded, all other inputs at 0.45V, and the outputs open.

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	D_{IN}	82S25	3101A	74S189
				Data Out		
Read	0	1	X	Stored $\overline{Data}$	Stored $\overline{Data}$	Stored $\overline{Data}$
Write "0"	0	0	0	1	1	Hi-Z
Write "1"	0	0	1	1	1	Hi-Z
Disable	1	X	X	1	1	Hi-Z

AC ELECTRICAL CHARACTERISTICS

$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	N82S25			N3101A, N74S189			UNIT
				Min	Typ	Max	Min	Typ	Max	
Access time										
t_{AA}	Address	Output	Address			50			35	ns
t_{CE}	Chip Enable	Output	Output			35			17	ns
Disable time[1]										
t_{CD}		Output	Chip Enable			35			17	ns
Response time[1]										
t_{WD}		Output	Write Enable			25			25	ns
Write recovery time										
t_{WR}						50			35	ns
Setup and hold time										
t_{WSA}[2]	Setup time	Write Enable	Address	5			0			ns
t_{WHA}[2]	Hold time	Write Enable	Address	5			0			ns
t_{WSD}	Setup time	Write Enable	Data in	30			0			ns
t_{WHD}	Hold time	Write Enable	Data in	5			0			ns
t_{WSC}	Setup time	Write Enable	$\overline{CE}$	0			0			ns
t_{WHC}	Hold time	Write Enable	$\overline{CE}$	5			0			ns
Pulse width[4]										
t_{WP}[3]	Write Enable			30			25			ns

NOTES:
1. Measured at a delta of 0.5V from the logic level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
2. Measured with minimum t_{WP}.
3. Measured with minimum t_{WSA}.
4. To gurarantee a Write into the slowest bit.

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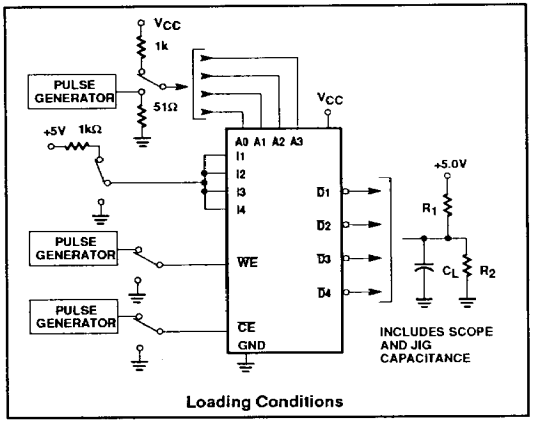
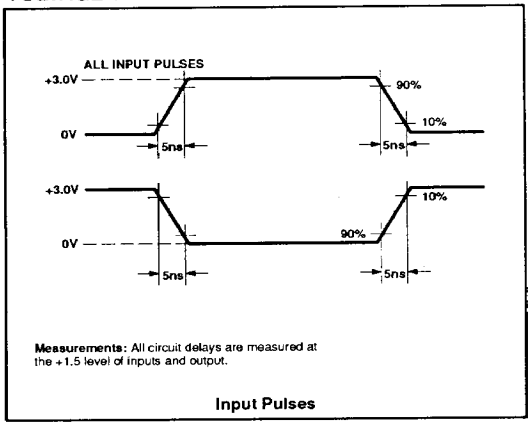
TEST LOAD CIRCUIT



Loading Conditions

VOLTAGE WAVEFORMS



Measurements: All circuit delays are measured at the +1.5 level of inputs and output.

Input Pulses

TIMING DIAGRAMS