REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
SHEET																								
REV																								
SHEET	22	23																						
REV STATUS OF SHEETS	REV																							
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21		

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Greg A. Pitz

CHECKED BY: Roy Monnin

APPROVED BY:

DRAWING APPROVAL DATE: 5 JANUARY 1989

REVISION LEVEL:

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, CMOS PARALLEL I/O CONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-89514
A	67268	

SHEET 1 OF 23

DESC FORM 193
SEP 87

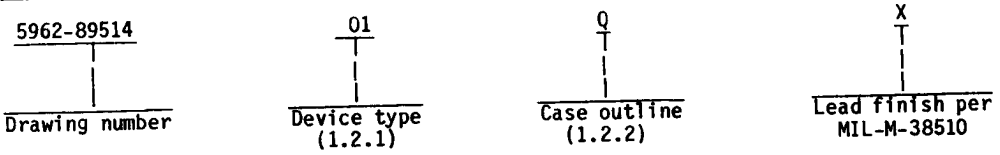
* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1144

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Frequency	Circuit function
01	Z84C2006	6.17 MHz	Parallel input/output controller

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 2.096" x .620" x .225"), dual-in-line package

1.3 Absolute maximum ratings.

V_{CC} supply voltage range (referenced to ground)	-0.3 to +7.0 V dc
Voltage on any pin (referenced to ground)	-0.3 to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation	1.0 W
Lead temperature (soldering, 10 seconds)	+270°C
Maximum junction temperature (T_J):	
At T_C = +125°C	+180°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C

1.4 Recommended operating conditions.

Supply voltage	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH}):	
Logic inputs	2.2 V dc
Clock input	V_{CC} - 0.6 V dc
Maximum low level input voltage (V_{IL}):	
Logic inputs	0.8 V dc
Clock input	0.45 V dc
Frequency of operation	DC to 6.17 MHz
Case operating temperature range (T_C)	-55°C to +125°C
Clock rise and fall times	20 ns maximum

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Block diagram. The block diagram shall be as specified on figure 2.

3.2.3 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C < T_C < +125°C$, $V_{CC} = 5.0\ V \pm 10\%$ unless otherwise specified	Group A subgroups	Reference number	Device type	Limits Min	Limits Max	Unit
Clock high input voltage	V_{IH1}		1,2,3		All	V_{CC} -0.6	V_{CC} +0.3 1/	V
Clock low input voltage	V_{IL1}		1,2,3		All	-0.3 1/	0.45	V
Logic input high voltage	V_{IH2}		1,2,3		All	2.2	V_{CC} 1/	V
Logic input low voltage	V_{IL2}		1,2,3		All	-0.3 1/	0.8	V
Logic low output voltage	V_{OL}	$I_{OL} = 2.0$ mA	1,2,3		All		0.4	V
Logic high output voltage	V_{OH1}	$I_{OH} = -1.6$ mA	1,2,3		All	2.4		V
Logic high output voltage	V_{OH2}	$I_{OH} = -250\ \mu A$	1,2,3		All	V_{CC} -.8		V
Power supply current	I_{CC1}	$V_{CC} = 5.0$ V, $V_{IH} = V_{CC} - 0.2$ V, $V_{IL} = 0.2$ V, $C_L = 100$ pF, CLK = 6 MHz	1,2,3		All		7	mA
Power supply current	I_{CC2}	$V_{CC} = 5.0$ V, CLK = 0 MHz	1,2,3		All		100	µA
Output leakage current low, open drain outputs	I_{LOL}	$V_{OUT} = 0.4$ V	1,2,3		All	-10	+10	µA
Output leakage current high, open drain outputs	I_{LOH}	$V_{OUT} = V_{CC}$	1,2,3		All	-10	+10	µA
Input low current (input and bidirectional)	I_{IL}	$V_{IN} = 0.4$ V	1,2,3		All	-10	+10	µA
Input high current (input and bidirectional)	I_{IH}	$V_{IN} = V_{CC}$	1,2,3		All	-10	+10	µA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C < T_C < +125°C$, $V_{CC} = 5.0\ V \pm 10\%$ unless otherwise specified	Group A subgroups	Reference number	Device type	Limits Min	Limits Max	Unit
Darlington drive current port B only 1/	I_{OH2}	$V_{CC} = 4.5\ V$, $V_{OH} = 1.5\ V$, $R_L = 1.1\ k\Omega$	1,2,3		All	-1.5	-5.0	mA
Clock input capacitance	C_{I1}	See 4.3.1c	4		All		10	pF
Logic input capacitance	C_{I2}		4		All		5	pF
Output and bidirectional capacitance	C_O		4		All		15	pF
Functional test		See 4.3.1d	7,8		All			
Maximum frequency 1/	f_{MAX}	See figure 3, $C_L = 100\ pF \pm 10\%$	9,10,11		All	6.17		MHz
Clock cycle time	t_{cyc} 2/		9,10,11	1	All	162		ns
Clock pulse width High	t_{PWH1}		9,10,11	2	All	65		ns
Clock pulse width Low	t_{PWL1}		9,10,11	3	All	65		ns
Clock time Fall 1/	t_{fc}		9,10,11	4	All		20	ns
Clock time Rise 1/	t_{rc}		9,10,11	5	All		20	ns
$\overline{CE}$, B/$\overline{A}$, C/$\overline{D}$ to $\overline{RD}$ $\overline{IORQ}$ setup time	t_{SHL1}		9,10,11	6	All	50 3/		ns
Any hold times for specified setup time 1/	t_{HLH1} t_{HHL1}		9,10,11	7	All	35		ns
$\overline{RD}$, $\overline{IORQ}$ to clock setup time	t_{SLH2} t_{SHL2}		9,10,11	8	All	70		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 5.0\ V \pm 10\%$ unless otherwise specified	Group A subgroups	Reference number	Device type	Limits Min	Limits Max	Unit
$\overline{RD}$, $\overline{IORQ}$ ↓ to data out delay	t_{PZL1} t_{PZH1}	See figure 3 C_L = 100 pF ±10%	9,10,11	9	All		300 4/	ns
$\overline{RD}$, $\overline{IORQ}$ ↑ to data out float delay 1/	t_{PLZ1} t_{PHZ1}		9,10,11	10	All		70	ns
Data in to clock ↑ setup time	t_{SZH1} t_{SZL1}	C_L = 50 pF ±10% See figure 3	9,10,11	11	All	40		ns
$\overline{IORQ}$ ↓ to data out delay (INTACK cycle)	t_{PZL2} t_{PZH2}	See figure 3 C_L = 100 pF ±10%	9,10,11	12	All	120 4/		ns
$\overline{MI}$ ↓ to clock ↑ setup time 5/	t_{SHL3}		9,10,11	13	All	70		ns
$\overline{MI}$ ↓ to clock ↑ setup time 5/ ($\overline{MI}$ cycle)	t_{SLH4}		9,10,11	14	All	0		ns
$\overline{MI}$ ↓ to IEO ↓ delay (interrupt-immediately preceeding $\overline{MI}$) 1/	t_{PHL1}		9,10,11	15	All		100 6/ 7/	ns
IEI to $\overline{IORQ}$ ↓ setup time (INTACK cycle) 1/	t_{SHL5}		9,10,11	16	All	100		ns
IEI ↓ to IEO ↓ delay	t_{PHL2}	C_L = 50 pF ±10% See figure 3	9,10,11	17	All		120 6/	ns
IEI ↓ to IEO ↑ delay (after ED decode)	t_{PLH3}	See figure 3 C_L = 100 pF ±10%	9,10,11	18	All		150 6/	ns
$\overline{IORQ}$ ↑ to clock ↓ setup time (to activate READY on next clock cycle) 1/	t_{SLH6}		9,10,11	19	All	170		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C < T_C < +125°C$, $V_{CC} = 5.0\ V \pm 10\%$ unless otherwise specified	Group A subgroups	Reference number	Device type	Limits Min	Limits Max	Unit
Clock ↓ to READY ↑ delay 1/	t_{PHL4}	C_L = 50 pF ±10% See figure 3	9,10,11	20	All	170 6/		ns
Clock ↓ to READY ↓ delay 1/	t_{PHL5}	See figure 3 C_L = 100 pF ±10%	9,10,11	21	All	120 6/		ns
$\overline{STROBE}$ pulse width 1/	t_{PWL2}		9,10,11	22	All	120 8/		ns
$\overline{STROBE}$ ↑ to clock ↓ setup time (to activate READY on next clock cycle) 1/	t_{SHL7}		9,10,11	23	All	150 6/		ns
$\overline{IORQ}$ ↓ to PORT DATA stable delay (mode 0)	t_{PZL3} t_{PZH3}		9,10,11	24	All		160 6/	ns
PORT DATA to $\overline{STROBE}$ ↑ setup time (mode 1)	t_{SLH8} t_{SHL8}		9,10,11	25	All	190		ns
$\overline{STROBE}$ ↓ to PORT DATA stable (mode 2)	t_{PZL4} t_{PZH4}		9,10,11	26	All		180 6/	ns
$\overline{STROBE}$ ↑ to PORT DATA delay (mode 2) 1/	t_{PLZ2} t_{PHZ2}	C_L = 50 pF ±10% See figure 3	9,10,11	27	All		160	ns
PORT DATA match to $\overline{INT}$↓delay (mode 3)	t_{PHL6}	See figure 3 C_L = 100 pF ±10%	9,10,11	28	All		430	ns
$\overline{STROBE}$ ↑ to $\overline{INT}$ ↓ delay	t_{PHL7}		9,10,11	29	All		350	ns

1/ Guaranteed, if not tested, to the limits specified herein.
2/ $t_{cyc} = t_{PWH1} + t_{rc} + t_{PWL1} + t_{fc}$.
3/ t_{SHL1} may be reduced, however, the time subtracted must be added to t_{PZL1} or t_{PZH1}.
4/ Increase by 10 ns for each 50 pF increase in load up to 200 pF maximum.
5/ To reset the PIO, $\overline{MI}$ must be active for a minimum of 2 clock cycles without an active $\overline{RD}$ or $\overline{IORQ}$ signal.
6/ Increase by 2 ns for each 10 pF increase in load up to 100 pF maximum.
7/ $2.5\ t_{cyc} > (N-2)\ t_{PHL2} + t_{PHL1} + t_{SHL5}$.
8/ For mode 2: $t_{PWL2} > t_{SLH8}$.

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Device type 01

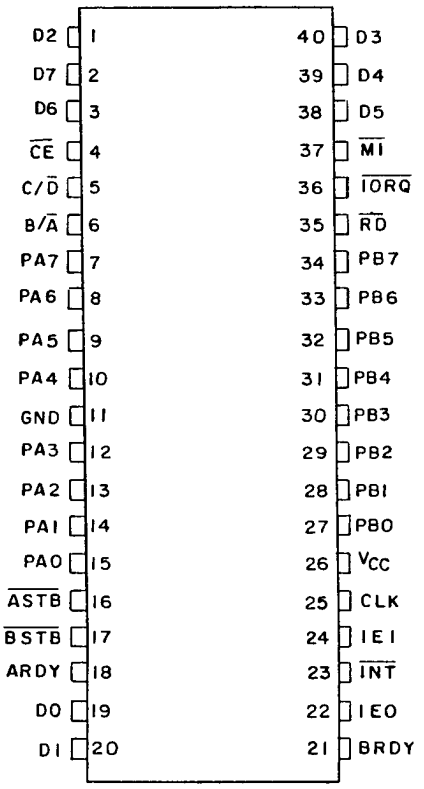


FIGURE 1. Terminal connections.

Device type 01

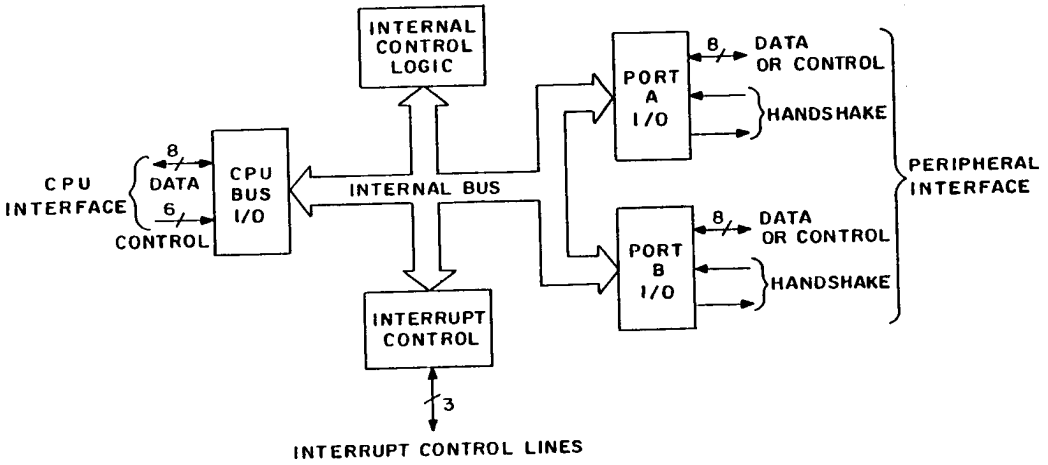
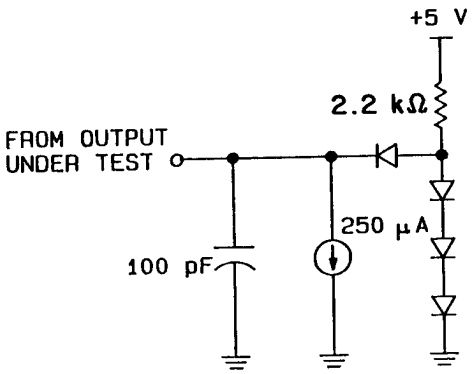


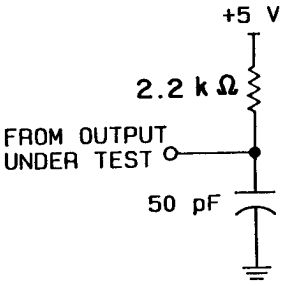
FIGURE 2. Block diagram.

Switching test circuits

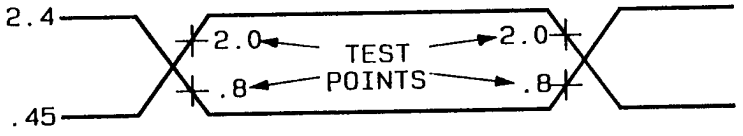
Standard test load



Open drain test load



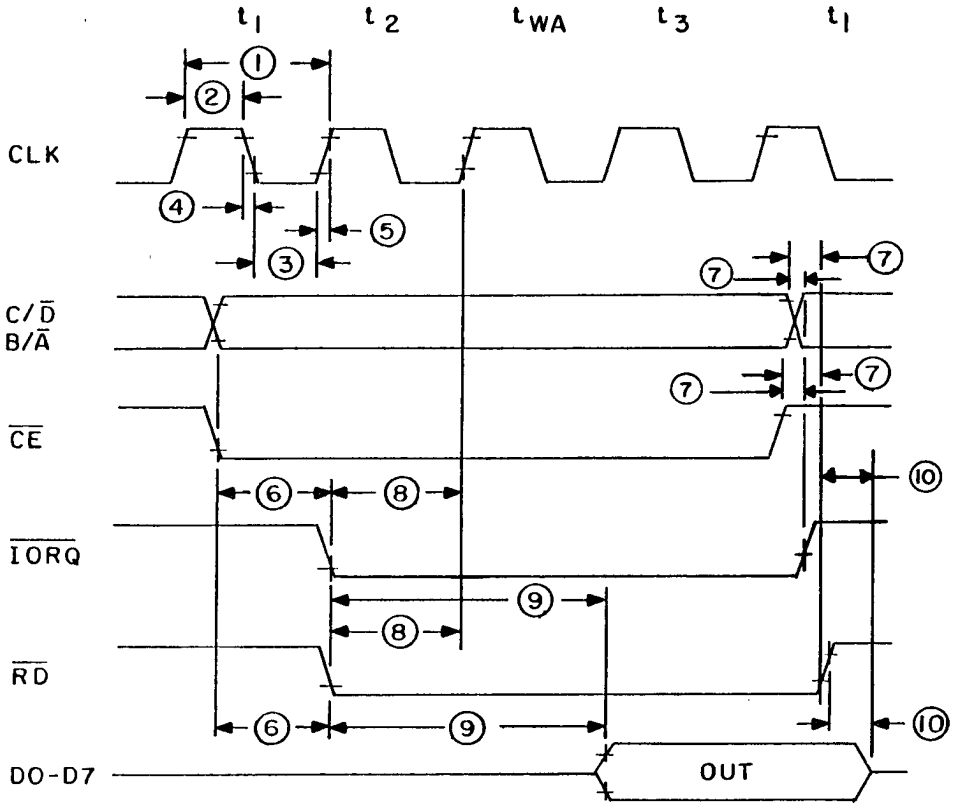
Switching test input/output waveform



AC testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for logic "0".

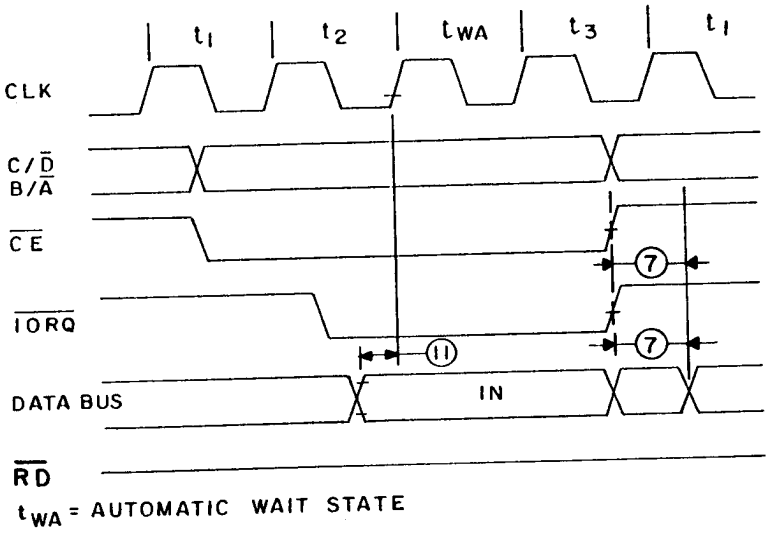
FIGURE 3. Timing diagram and test circuits.

Device type 01



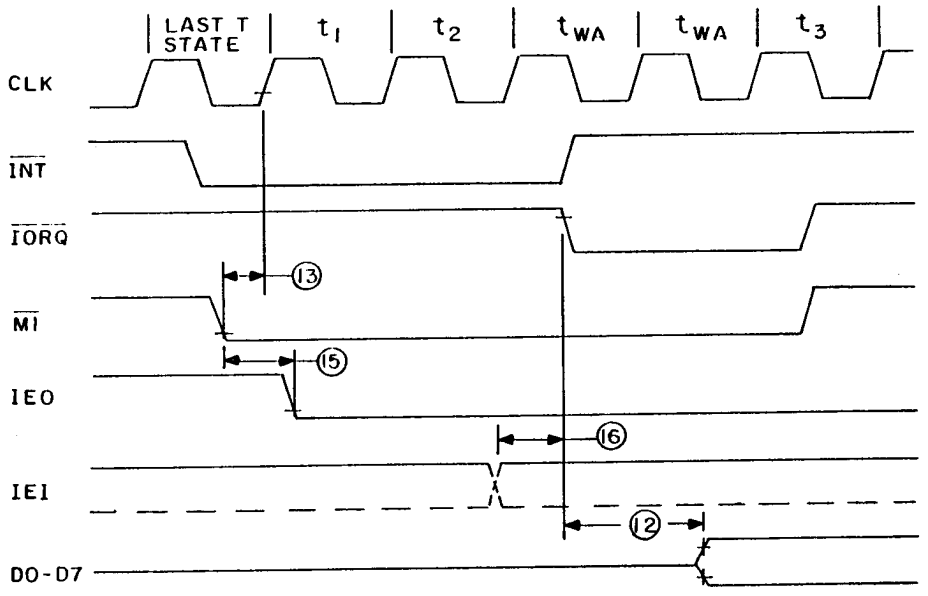
Read cycle timing

FIGURE 3. Timing diagram and test circuits - Continued.



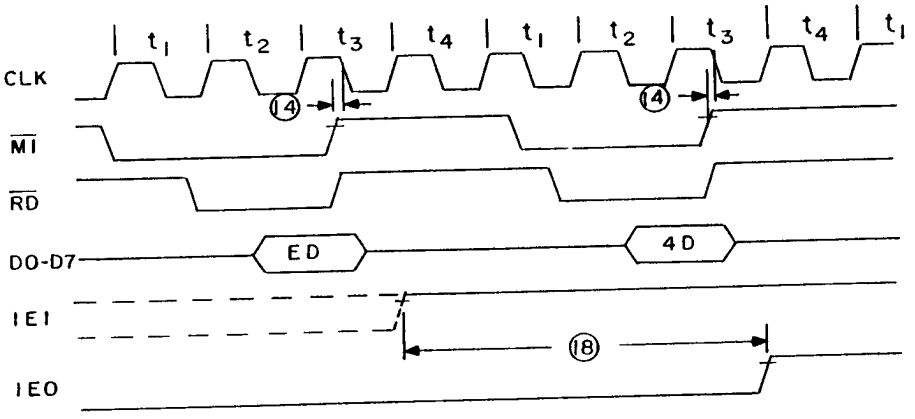
Write cycle timing

FIGURE 3. Timing diagram and test circuits - Continued.



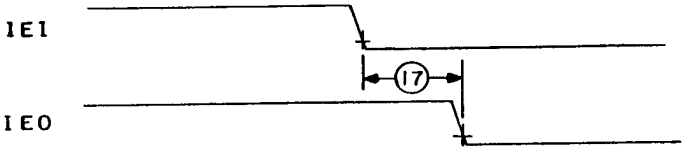
Interrupt acknowledge timing

FIGURE 3. Timing diagram and test circuits - Continued.



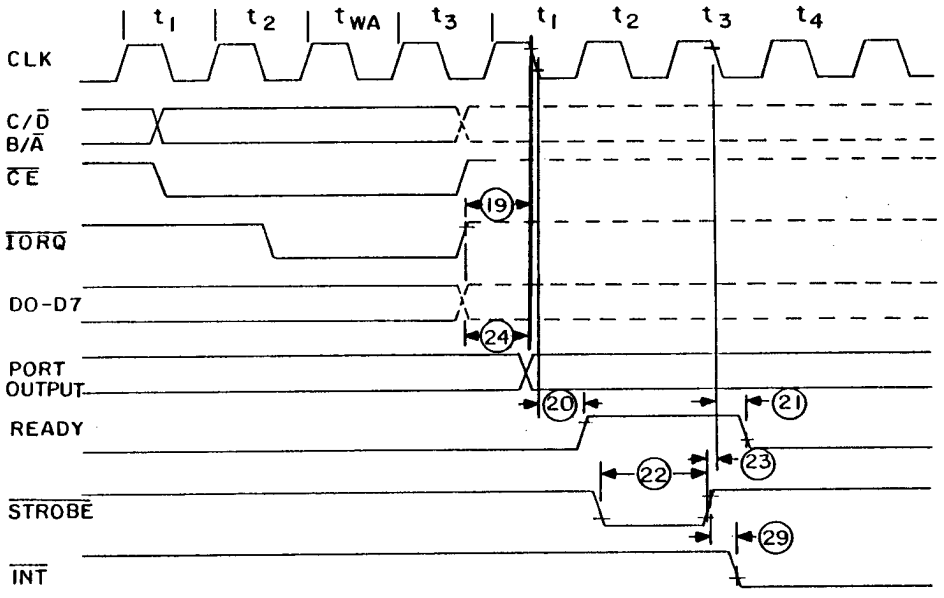
Return from interrupt timing

FIGURE 3. Timing diagram and test circuits - Continued.



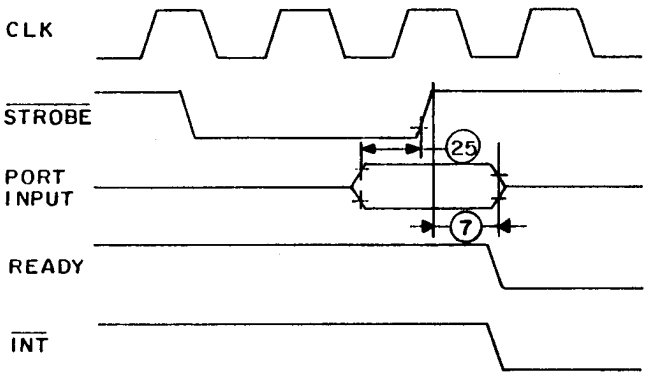
IEI/IEO timing

FIGURE 3. Timing diagram and test circuits - Continued.



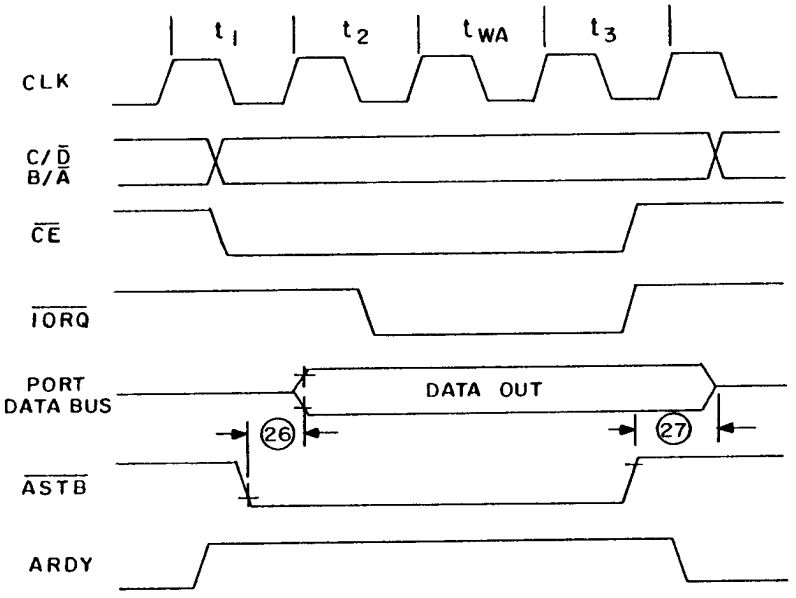
Mode 0 input timing

FIGURE 3. Timing diagram and test circuits - Continued.



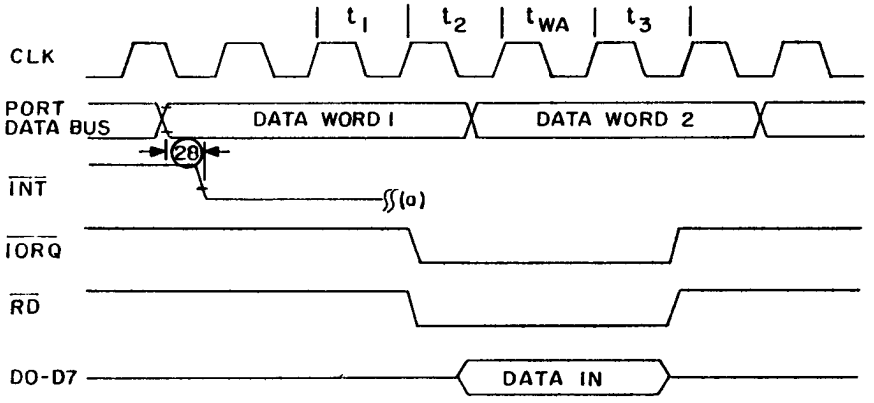
Mode 1 input timing

FIGURE 3. Timing diagram and test circuits - Continued.



Mode 2 bidirectional timing
write data to port A registers

FIGURE 3. Timing diagram and test circuits - Continued.



(a) $\overline{INT}$ GENERATED ONLY WHEN ENABLED

Mode 3 bit mode timing

FIGURE 3. Timing diagram and test circuits - Continued.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{I1}, C_{I2}, and C_O measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

d. Subgroup 7 and 8 functional testing shall include verification of instruction set. These tests form a part of the manufacturers test tape and shall be maintained and available from approved sources of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7,8,9, 10,11
Group A test requirements (method 5005)	1,2,3,4,7,8,9, 10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Terms and definitions. The abbreviations, terms, symbols, and definitions used herein (including terms and symbols for device terminals) are defined in MIL-M-38510, MIL-STD-1331, and as follows:

IEI	Interrupt enable in (input, active high). When this line is active, the PIO is able to interrupt the CPU.
IEO	Interrupt enable out (output, active high). This output is high only if IEI is high and the CPU is not servicing an interrupt from this PIO. In conjunction with IEI, this line can be used to implement a system-wide interrupt priority daisy chain.
A0-A7	Port A bus (bidirectional, three-state). This 8-bit bus is used to transfer data or status or control information between port A of the PIO and a peripheral device. A0 is the least significant bit.

$\overline{ASTB}$	Port A strobe pulse (input, active low). The meaning of this signal depends on the mode of operation selected for port A as follows: (1) Output mode: The positive edge of this strobe is issued by the peripheral to acknowledge the receipt of data from the PIO. (2) Input mode: The strobe is issued by the peripheral to load data from the peripheral into port A of the PIO. Data is loaded into the PIO when this signal is active. (3) Bidirectional mode: When this signal is active, data from the port A output register is gated onto the port A bidirectional bus. The positive edge of the strobe acknowledges the receipt of the data. (4) Control mode: The strobe is inhibited internally.
ARDY	Register A ready (output, active high). The meaning of this signal depends on the mode of operation selected for port A as follows: (1) Output mode: This signal goes active to indicate that the port A output register has been loaded and the peripheral data bus is stable and ready for transfer to the peripheral device. (2) Input mode: This signal is active when the port A input register is empty and is ready to accept data from the peripheral device. (3) Bidirectional mode: This signal is active when data is available in the port A output register for transfer to the peripheral device. In this mode data is not placed on the port A bus unless $\overline{ASTB}$ is active.
B0-B7	Port B bus (bidirectional, tristate). This 8-bit bus is used to transfer data and/or status or control information between port B of the PIO and a peripheral device. The port B bus is capable of supplying 1.5 mA at 1.5 V to drive Darlington transistors. B0 is the least significant bit of the bus.
$\overline{BSTB}$	Port B strobe pulse (input, active low). The meaning of this signal is similar to that of $\overline{ASTB}$ with the following exception: In the port A bidirectional mode, this signal strobes data from the peripheral device onto the port A input register.
BRDY	Register B ready (output, active high). The meaning of this signal is similar to that of A ready with the following exception: In the port A bidirectional mode this signal is high when the port A input register is empty and ready to accept data from the peripheral device.
D0-D7	CPU data bus (bidirectional, tristate). This bus is used to transfer all data and commands between the CPU and PIO. D0 is the least significant bit of the bus.
B/$\overline{A}$	Port B or A select (input, active high). This pin defines which port will be accessed during a data transfer between the CPU and PIO. A low level on this pin selects port A while a high level selects port B.
C/$\overline{D}$	Control or data select (input, active high). This pin defines the type of data transfer to be performed between the CPU and PIO. A high level on this pin during a CPU write to the PIO causes the data bus to be interpreted as a command for the port selected by the B/$\overline{A}$ SEL line. A low level on this pin means that the data bus is being used to transfer data between the CPU and the PIO.

$\overline{CE}$ Chip enable (input, active low). A low level on this pin enables the PIO to accept command or data inputs from the CPU during a write cycle, or to transmit data to the CPU during a read cycle.

CLK System clock (input). The PIO uses the standard system clock to synchronize certain signals internally. This is a single phase clock.

$\overline{MI}$ Machine cycle 1 (input, active low). This signal from the CPU is used as a sync pulse to control internal PIO operations. When $\overline{MI}$ is active and the $\overline{RD}$ signal is active, the CPU is fetching an instruction from memory. Conversely, when $\overline{MI}$ is active and $\overline{IORQ}$ is active, the CPU is acknowledging an interrrupt. In addition, the $\overline{MI}$ signal has two other functions within the PIO:

(1) $\overline{MI}$ synchronizes the PIO interrupt logic.

(2) When $\overline{MI}$ occurs without an active $\overline{RD}$ or $\overline{IORQ}$ signal the PIO enters a reset state.

6.5 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8951401QX	56708	Z84C2006CMB	---

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
56708	Zilog, Incorporated 210 Hacienda Avenue Campbell, CA 95008