16-bit buffer/line driver; with 30Ω series termination resistors; 5V input/output tolerant (3-State)

74LVC162244A/ 74LVCH162244A

FEATURES

- 5 volt tolerant inputs/outputs for interfacing with 5V logic
- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Bus Hold on data inputs (74LVCH162244A only)
- Integrated 30Ω termination resistors

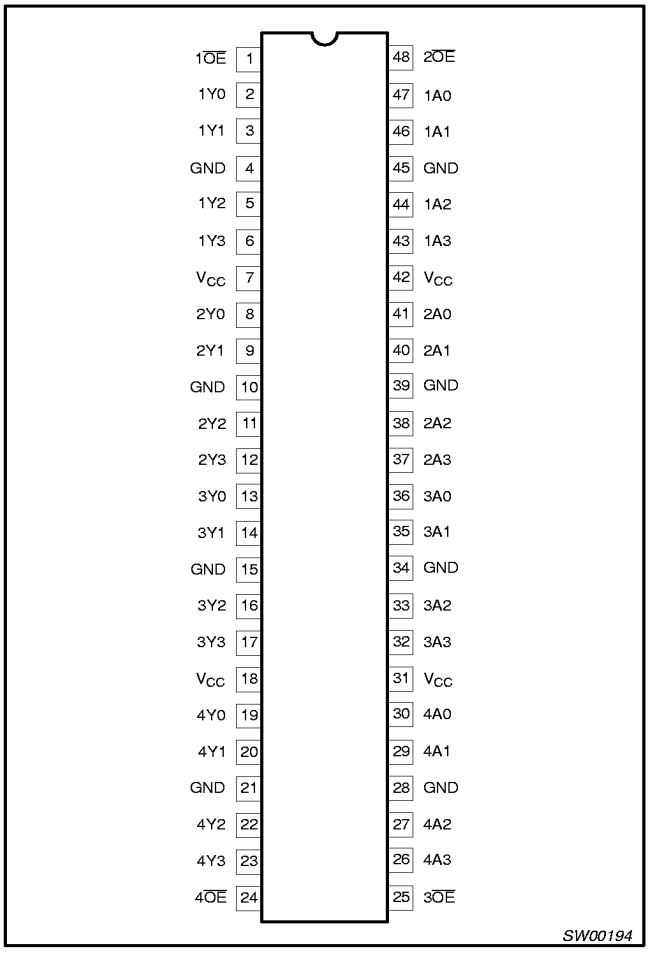
DESCRIPTION

The 74LVC(H)162244A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. These features allow the use of these devices in a mixed 3.3V/5V environment.

The 74LVC(H)162244A is a 16-bit non-inverting buffer/line driver with 3-State outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. The 3-State outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. The 74LVC(H)162244A is designed with 30Ω series termination resistors in both HIGH and LOW output stages to reduce line noise. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer.

The 74LVCH162244A bus hold data inputs eliminates the need for external pull up resistors to hold unused inputs.

PIN CONFIGURATION



ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74LVC162244A DL	VC162244A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVC162244A DGG	VC162244A DGG	SOT362-1
48-Pin Plastic SSOP Type III	–40°C to +85°C	74LVCH162244A DL	VCH162244A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVCH162244A DGG	VCH162244A DGG	SOT362-1

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay 1An to 1Yn; 2An to 2Yn	C_L = 50pF V_{CC} = 3.3V	2.9	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per buffer	V_I = GND to V_{CC}[1]	25	pF

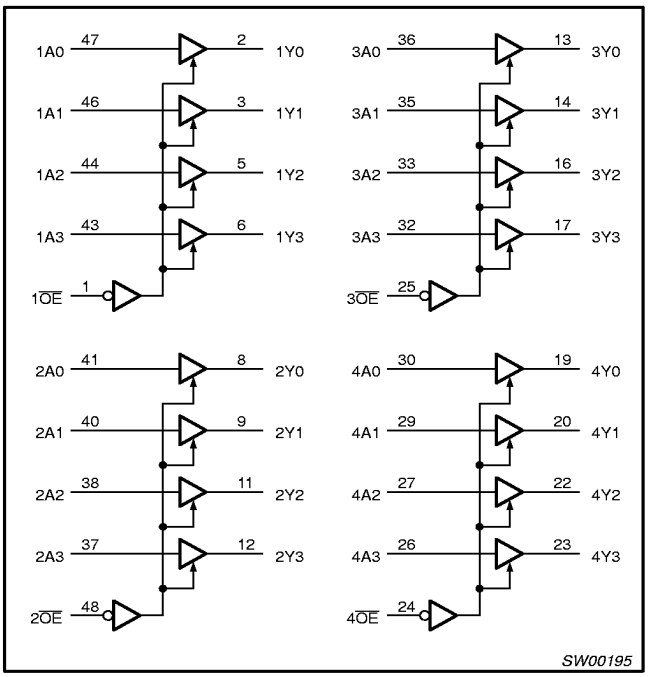
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in W):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	Output enable input (active LOW)
2, 3, 5, 6	1Y0 to 1Y3	Data outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
8, 9, 11, 12	2Y0 to 2Y3	Data outputs
13, 14, 16, 17	3Y0 to 3Y3	Data outputs
19, 20, 22, 23	4Y0 to 4Y3	Data outputs
24	$4\overline{OE}$	Output enable input (active LOW)
25	$3\overline{OE}$	Output enable input (active LOW)
30, 29, 27, 26	4A0 to 4A3	Data inputs
36, 35, 33, 32	3A0 to 3A3	Data inputs
41, 40, 38, 37	2A0 to 2A3	Data inputs
47, 46, 44, 43	1A0 to 1A3	Data inputs
48	$2\overline{OE}$	Output enable input (active LOW)

LOGIC SYMBOL

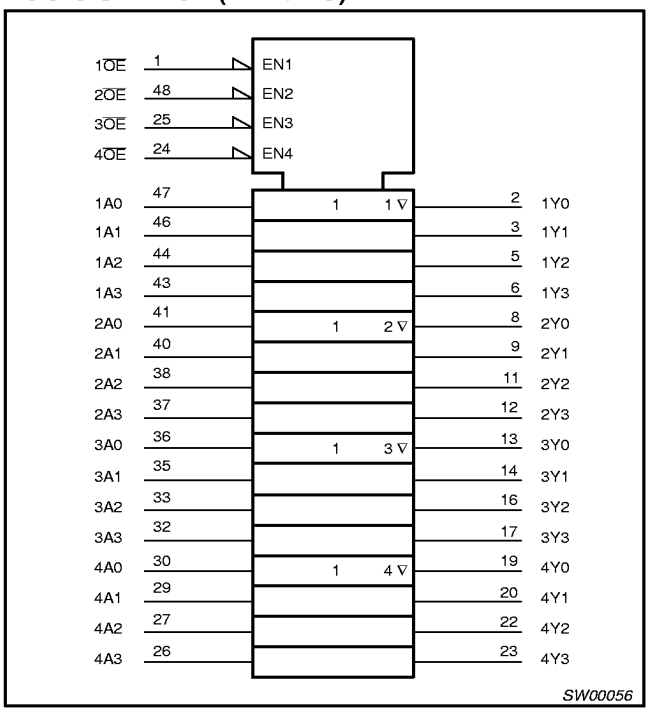


FUNCTION TABLE

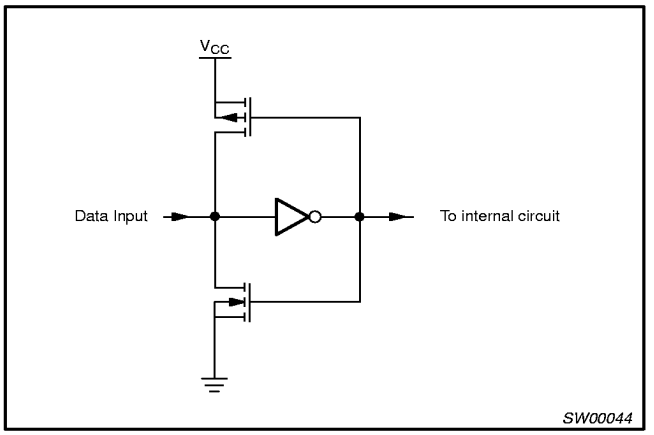
INPUTS		OUTPUT
$n\overline{OE}$	nAn	nYn
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

LOGIC SYMBOL (IEEE/IEC)



BUSHOLD CIRCUIT



ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134) Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		–0.5	+6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–	–50	mA
V_I	DC input voltage	Note 2	–0.5	+6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	–	50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	–0.5	V_{CC} + 0.5	V
V_O	DC output voltage; output 3-State	Note 2	–0.5	6.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	–	50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		–	100	mA
T_{stg}	Storage temperature range		–65	+150	°C
P_{tot}	Power dissipation per package – SSOP and TSSOP package	Above +60°C derate linearly 5.5mW/K		500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN.	MAX.	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC Input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
V_O	DC output voltage range; output 3-State		0	5.5	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics for individual device	–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –6mA	V_{CC}* 0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC}* 0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 12mA	V_{CC}* 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 6mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND[6]		0.1	5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; V_I = V_{IH} or V_{IL}; V_O = 5.5V or GND[6]		0.1	10	µA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V		0.1	10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	40	µA
ΔI_{CC}	Additional quiescent supply current per control pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V; I_O = 0		5	500	µA
ΔI_{CC}	Additional quiescent supply current per data input pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V; I_O = 0		150	750	µA
I_{BHL}	Bus hold LOW sustaining current	V_{CC} = 3.0V; V_I = 0.8V[2, 3, 4]	75			µA
I_{BHH}	Bus hold HIGH sustaining current	V_{CC} = 3.0V; V_I = 2.0V[2, 3, 4]	–75			µA
I_{BHLO}	Bus hold LOW overdrive current	V_{CC} = 3.6V[2, 3, 5]	450			µA
I_{BHHO}	Bus hold HIGH overdrive current	V_{CC} = 3.6V[2, 3, 5]	–450			µA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts (LVCH16-A) only.
3. For data inputs only, control inputs do not have a bus hold circuit.
4. The specified sustaining current at the data input holds the input below the specified V_I level.
5. The specified overdrive current at the data input forces the data input to the opposite logic input state.
6. For bus hold parts, the bus hold circuit is switched off when V_i exceeds V_{CC} allowing 5.5V on the input terminal.

AC CHARACTERISTICS

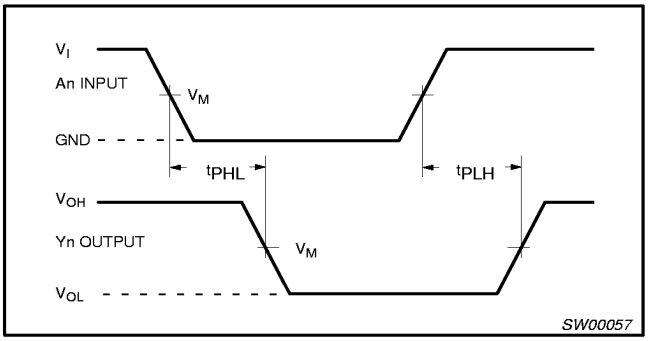
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		
			MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL} t_{PLH}	Propagation delay 1An to 1Yn; 2An to 2Yn	1	1.5	2.9	6.3	1.5	7.3	ns
t_{PZH} t_{PZL}	3-State output enable time $1\overline{OE}$ to 1Yn; $2\overline{OE}$ to 2Yn	2, 3	1.5	3.4	7.1	1.5	8.1	ns
t_{PHZ} t_{PLZ}	3-State output disable time $1\overline{OE}$ to 1Yn; $2\overline{OE}$ to 2Yn	2, 3	1.5	2.8	5.0	1.5	6.0	ns

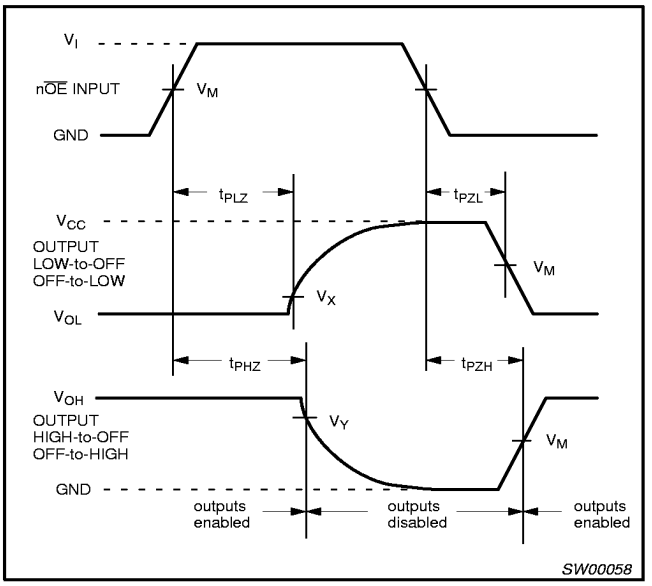
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at V_{CC} w 2.7V; V_M = 0.5 V_{CC} at V_{CC} t 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at V_{CC} w 2.7V; $V_X = V_{OL}$ + 0.1 V_{CC} at V_{CC} t 2.7V
$V_Y = V_{OH}$ –0.3V at V_{CC} w 2.7V; $V_Y = V_{OH}$ – 0.1 V_{CC} at V_{CC} t 2.7V

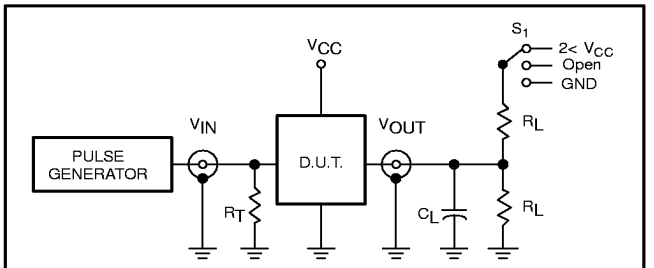


Waveform 1. Input (An) to output (Yn) propagation delay times



Waveform 2. 3-State enable and disable times

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2< V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_{IN}
t 2.7V	V_{CC}
2.7 – 3.6V	2.7V

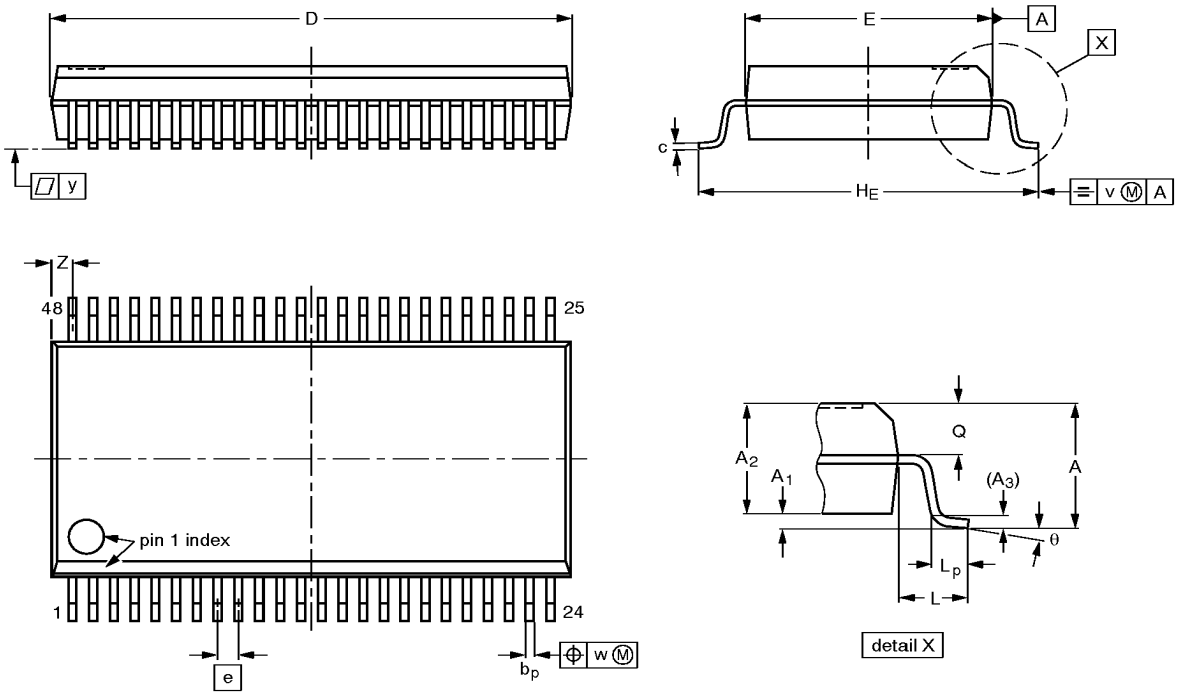
DEFINITIONS

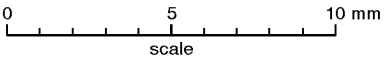
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00047

Waveform 3. Load circuitry for switching times

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**





DIMENSIONS (mm are the original dimensions)

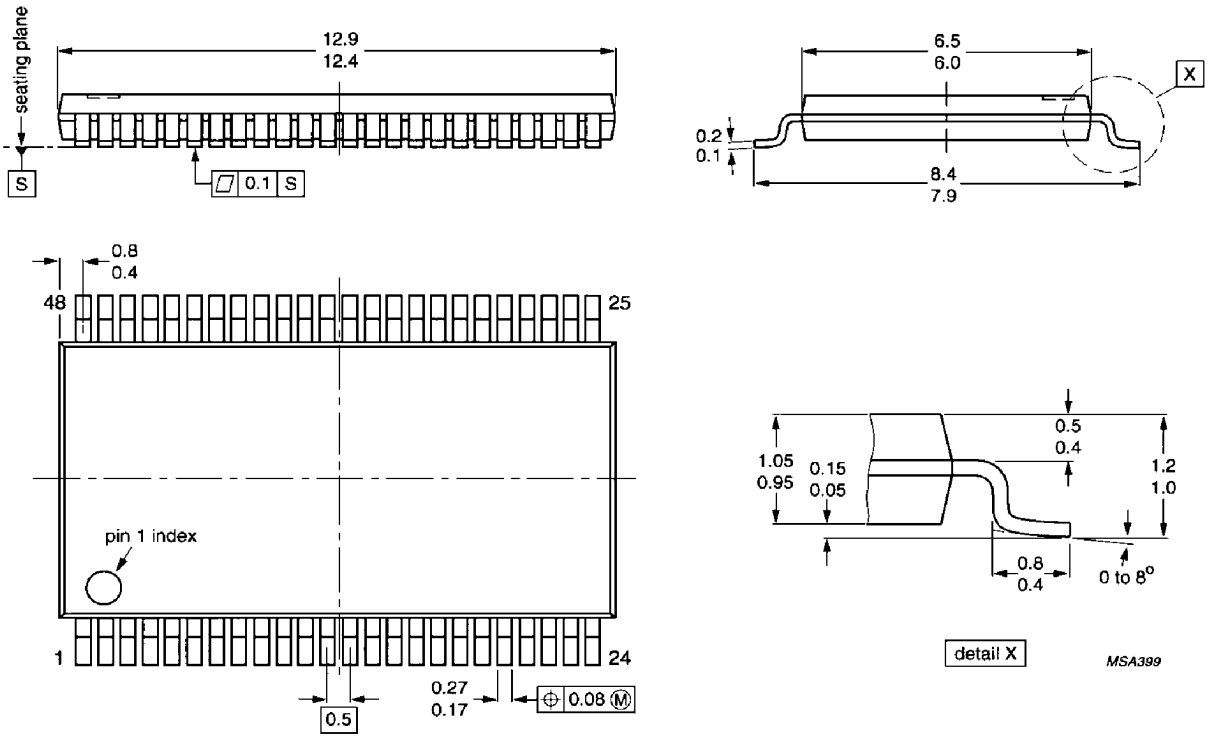
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				~~93-11-02~~ 95-02-04

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm **SOT362-1**



Dimensions in mm.