ANALOG DEVICES

12-Bit, 10 MSPS A/D Converter

ANALOG DEVICES INC

AD9005A

1.1 Scope.

This specification covers the requirements for a 12-bit, high speed analog-to-digital converter (ADC). The AD9005A is a complete 12-bit ADC which includes on-board track-and-hold amplifier, voltage reference, and timing circuits.

1.2 Part Number.

The complete part number is as follows:

Device	Part Number
−1	AD9005ATM/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
M	M-46	46-Pin Hermetic Metal DIP

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

Power Supply Voltages ($\pm V_S$)	±6 V
Positive Supply Voltage ($+V_{CC}$)	+18 V
Negative Supply Voltage ($-V_{EE}$)	−18 V
Power Dissipation (Typical)	260 mW
Analog Input Voltage (Pin 45)	±3.0 V dc
Digital Input Voltage	−0.5 V to $+V_S$
Digital Output Current	4 mA
Junction Temperature	+175°C
Operating Temperature Range (Case)	−55°C to +125°C
Storage Temperature Range (Case)	−65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

1.5 Thermal Characteristics.

Maximum junction temperature should not be allowed to exceed +175°C. Hybrid thermal model:
$T_{JUNCTION} = T_{AMBIENT} + P_{DISSIPATION} \times (\theta_{CA}) + (T_S - T_C)$ max
where $(T_S - T_C)$ max = 10°C. θ_{CA} = 14°C/W in still air; θ_{CA} = 6°C/W with 500 LFPM air flow.

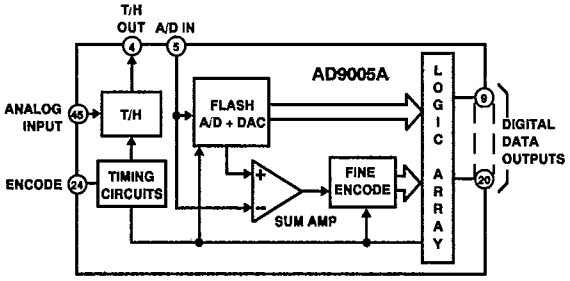
AD9005A—SPECIFICATIONS

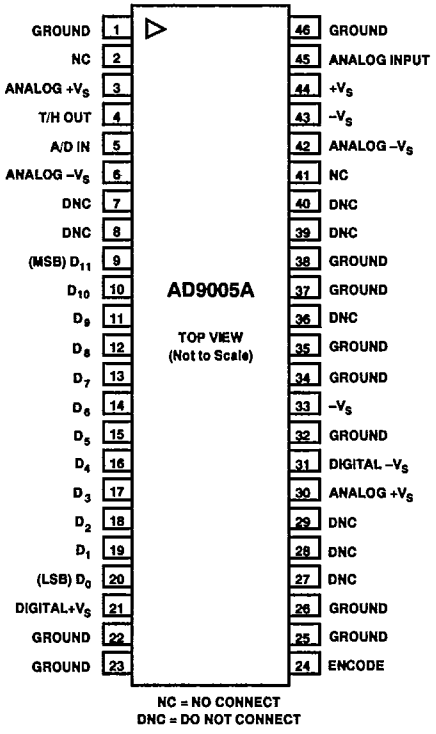
Table 1.

Test	Symbol	Device	Design Limits[1]	Sub Group 1	Sub Group 2, 3	Sub Group 4	Sub Group 5, 6	Test Condition[2]	Units
Differential Nonlinearity	DNL	−1				±0.75	−1.0 +1.5		LSB
Integral Nonlinearity[3]	INL	−1	±2.25						LSB
Gain Error		−1				±1.0	±2.0		% FS
Offset Error	V_{OS}	−1				±15	±40		mV
Input Resistance	R_I	−1		950	950				Ω min
				1050	1050				Ω max
Maximum Conversion Rate		−1				10.1	10.1		MSPS min
Aperture Uncertainty (Jitter)	t_j	−1	20					@ +25°C	ps rms
Transient Response	t_{TR}	−1	120					FS Step Input to ±1 LSB @ +25°C	ns
Overvoltage Recovery Time	t_{OR}	−1	250					200% Input to ±1 LSB @ +25°C	ns
Harmonic Distortion[4]	HD	−1					−63	f_{IN} = 4.3 MHz	dBc min
Signal-to-Noise Ratio[5]	SNR	−1					60	f_{IN} = 4.3 MHz	dB min
Encode Pulse Voltage (HIGH)	$V_{E(H)}$	−1	2.0						V min
Encode Pulse Voltage (LOW)	$V_{E(L)}$	−1	0.8						V max
Encode Pulse Current (HIGH)	$I_{E(H)}$	−1		150	150				μA max
Encode Pulse Current (LOW)	$I_{E(L)}$	−1		150	150				μA max
Encode Pulse Width (HIGH)	$t_{E(H)}$	−1	25					@ +25°C	ns min
High Level Output Voltage	V_{OH}	−1		2.4	2.4			2 mA source	V min
Low Level Output Voltage	V_{OL}	−1		0.4	0.4			4 mA sink	V max
Positive Analog Supply Current (+5.0 V)	$+I_{AS}$	−1		210	210				mA max
Negative Analog Supply Current (−5.2 V)	$-I_{AS}$	−1		250	250				mA max
Positive Digital Supply Current (−5.2 V)	$+I_{DS}$	−1		60	60				mA max
Negative Digital Supply Current (−5.2 V)	$-I_{DS}$	−1		100	100				mA max
Positive Supply Current (+15.0 V)	$+I_{CC}$	−1		25	25				mA max
Negative Supply Current (−15.0 V)	$-I_{EE}$	−1		55	55				mA max
Power Supply Rejection Ratio[6]	PSRR	−1				0.02			%/% max
Power Dissipation	P_{DISS}	−1		4.1					W max

NOTES
[1]Indicates specification which is guaranteed but not tested. Value shown is at T_A = full unless otherwise noted in Test Conditions.
[2]$+V_{CC}$ = +15 V; $-V_{EE}$ = −15 V; $+V_S$ = +5 V; $-V_S$ = −5.2 V, unless otherwise indicated.
[3]Parameter is tested at +25°C; guaranteed but not tested at temperature extremes.
[4]Input at 1 dB below full scale; worst case spurious in-band signal relative to input level.
[5]Input at 1 dB below full scale; rms signal to rms noise, including harmonics.
[6]Sensitivity of full-scale gain error with respect to power supply variation with supply min/max limits; PSRR is tested over given voltage range.

3.2.1 Functional Block Diagram and Terminal Assignments.





NC = NO CONNECT
DNC = DO NOT CONNECT

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).