CALMOS™

CA29C632A

WINDOW ADDRESSABLE MEMORY

- **32 simultaneous range comparisons every 80 nsec (up to 32 bits wide)**
- **Maximum processing throughput of 12.8 Gbits/s**
- **Handles up to 32 - bit input words**
- **Fully programmable windows and subfields**
- **On board sequential priority encoder:**
  - **– produces 5 - bit match address**
  - **– multiple match resolution capability**
  - **– expansion I/O – vertically cascadable**
- **64 - bit mode**
- **Separate synchronous 32 - bit buses for programming limit and parameter data**
- **Exceeds VHSIC Phase 1 performance criteria**
- **Low power CMOS**
- **TTL compatible**
- **120 lead PGA package**

The Newbridge Microsystems *CA29C632A Window Addressable Memory (WAM)* is a high speed associative processor capable of comparing up to 32-bit input words against 32 programmable sets of upper and lower limits in 80 nsec. Each window can be divided into a maximum of four fields for multidimensional window comparisons. Multiple CA29C632As can be arrayed in the vertical direction for an increased number of windows.

Powerful programmable control enables the WAM to accept or reject inputs falling within one or more windows, turn entire windows on and off, perform logic AND/OR/NOT comparisons on the data and change window field resolution from multiple 8-bit fields to a single 32-bit field. The control allows 16-bit subfields to be programmed in one cycle – this includes both limits and control.

Upon receiving an input word that falls within one of the 32 windows, a match exists. The match output will be output through the on–board *Sequential Priority Encoder* (SPE), an intelligent logic block. The SPE generates a 5-bit match address when a valid match occurs. The SPE has two flags to indicate that the match address is valid and that the current match address is the last valid one – for multiple match resolution. The SPE also has expansion I/O which allows easy cascading of CA29C632A devices.

Applications for the CA29C632A include:

- Signal processing
- Environmental filtering
- High speed associative processing
- Fuzzy associative memory
- List sorts
- Database searching and management
- High speed record searching for optical mass storage
- Pattern recognition

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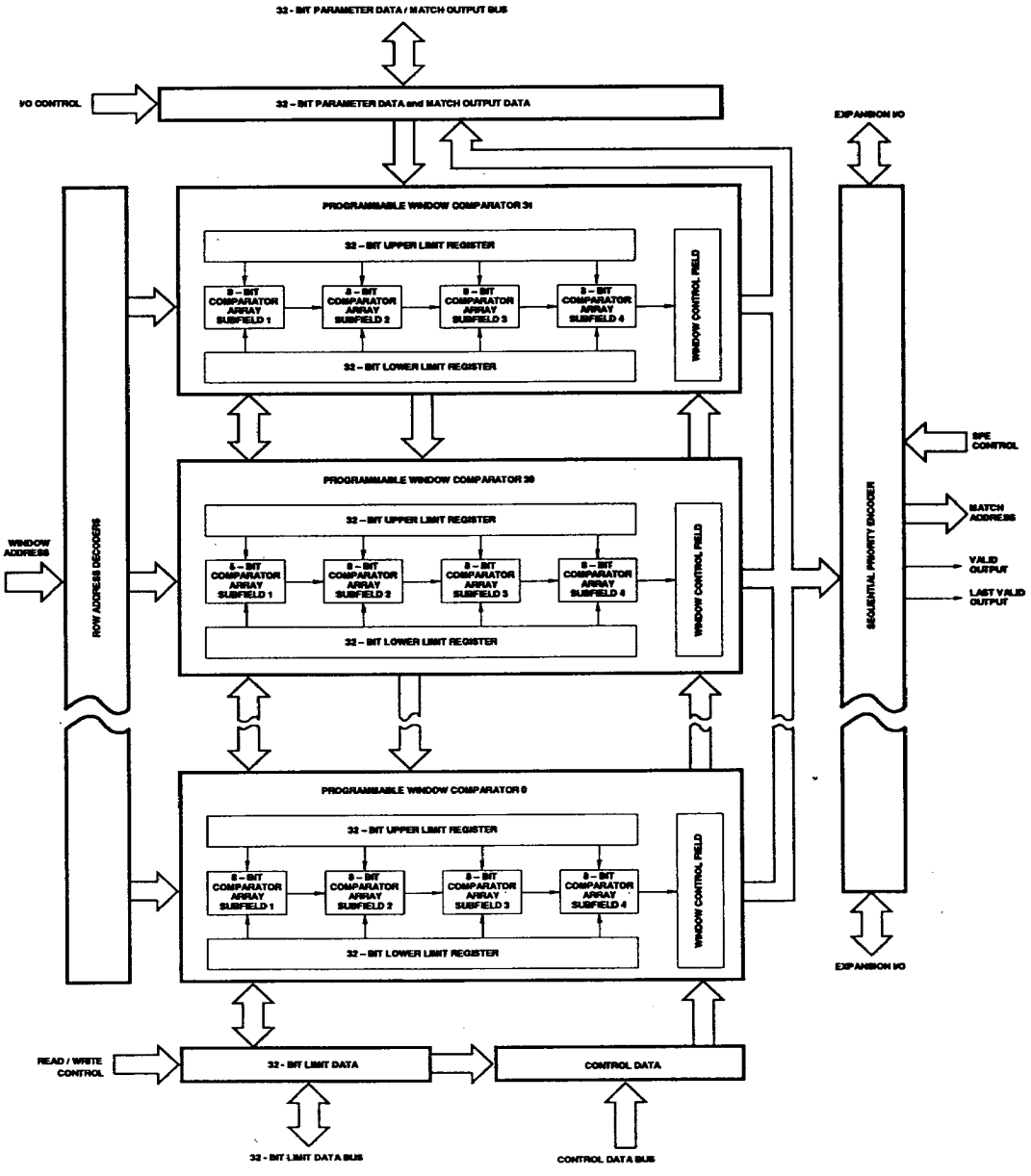

Figure 1 : CA29C632A WINDOW ADDRESSABLE MEMORY BLOCK DIAGRAM

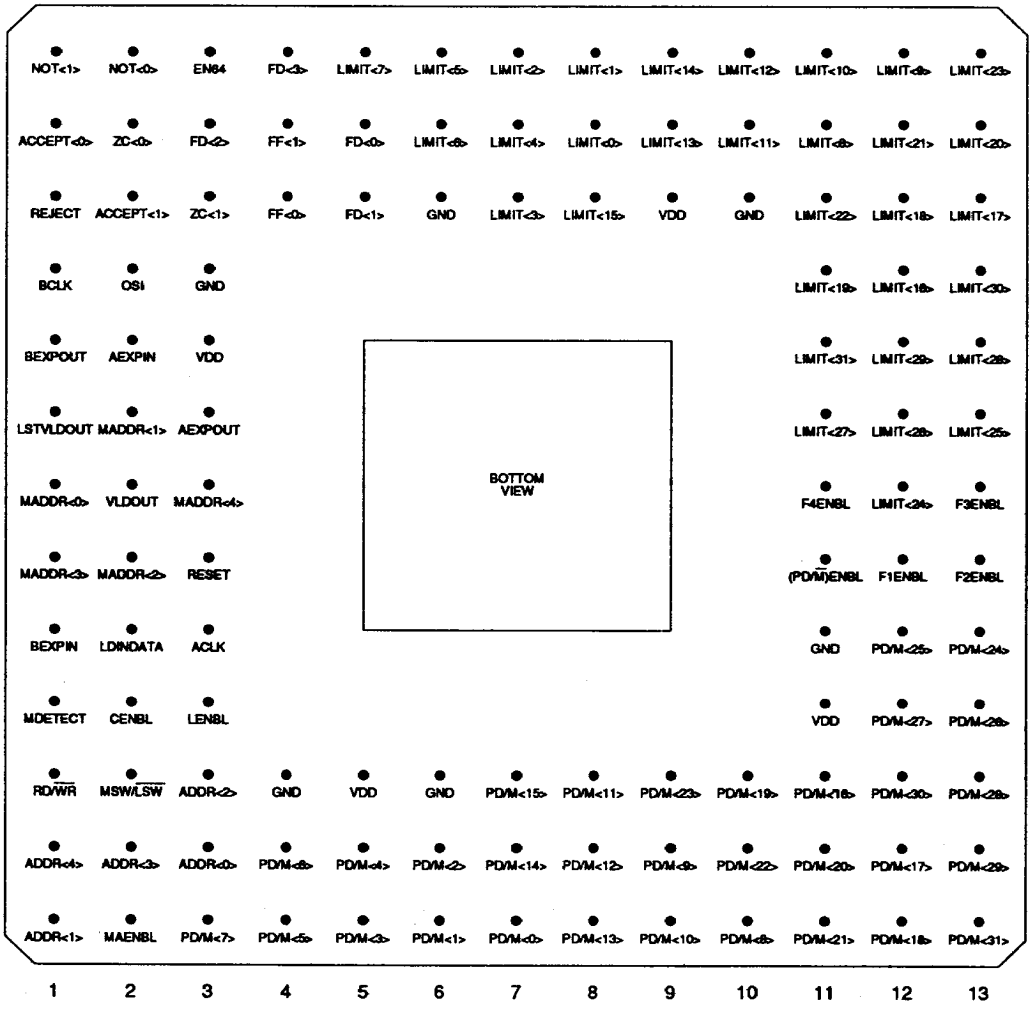

Figure 2 : 120 – PIN PGA PINOUT CONFIGURATION

Table 1 : PIN DESCRIPTIONS

Symbol	Type	Name and Function
Window Addressable Memory Control		
ACLK	I	**Clock A :** Input clock (12.5 MHz maximum). Loads input data into registers on rising edge if enable signals active. Clock is also used to read and write limit data if the appropriate enables are active.
$ADDR_{4-0}$	I	**Address Bus :** 5 address lines that are decoded to select one of 32 windows.
MSW/$\overline{LSW}$	I	**Most Significant Word / Least Significant Word :** One input address signal. Set high to access MSW and set low to access LSW.
RD/$\overline{WR}$	I	**Read / Write :** Input signal used for reading and writing limit data, and for writing control data bits only. Set high for read and set low for write.
Parameter Data		
PD/M_{31-0}	I/O	**Parameter Data / Match Bus :** Bidirectional bus, when acting as input corresponds to parameter data to be processed. When acting as output corresponds to match outputs from the 32 windows (active high).
(PD/$\overline{M}$)ENBL	I	**Parameter Data / $\overline{\text{Match}}$ Enable :** A high signal on this pin causes parameter data to be input to the device. A low on this signal causes match outputs to be output from the device.
F1ENBL	I	**Field 1 Enable :** Parameter data is latched and presented to the comparator array on the rising edge of ACLK if the appropriate Field Enable is high. A low signal on F1ENBL inhibits effect of ACLK for the first 8 bit field of parameter data (lower most byte of data). The previously latched parameter data value is used for successive comparisons when the Field Enable is low. This signal can be used in conjunction with Field Disables FD_{3-0}.
F2ENBL	I	**Field 2 Enable :** A low signal inhibits effect of ACLK for the second 8 bit field of parameter data. See F1ENBL for a complete description.
F3ENBL	I	**Field 3 Enable :** A low signal inhibits effect of ACLK for the third 8 bit field of parameter data. See F1ENBL for a complete description.
F4ENBL	I	**Field 4 Enable :** A low signal inhibits effect of ACLK for the fourth 8 bit field of parameter data (upper most byte of data). See F1ENBL for a complete description.
Limit Data Memory		
$LIMIT_{31-0}$	I/O	**Limit Data Bus :** Bidirectional bus, when acting as input corresponds to limit data to be written to the device. When acting as output corresponds to limit data read from the device. The most significant 16 bits corresponds to 16 bits of upper limit data and the least significant 16 bits corresponds to 16 bits of lower limit data.
LENBL	I	**Limit Enable :** The enable for reading and writing to the limit registers.
Control Data Memory		
CENBL	I	**Control Enable :** The enable for writing to the control register bits.
REJECT	I	**Reject Control Data Bit :** Set high to reject a window.
NOT_{1-0}	I	**Not Control Data Bits :** Set high to NOT an 8 bit field of data in a window. NOT_1 corresponds to the upper byte of a 16 bit word section and NOT_0 corresponds to the lower byte.
ZC_{1-0}	I	**Zero Crossover Control Data Bits :** Set high to perform Zero Crossover function on an 8 bit field of data in a window. ZC_1 corresponds to upper byte of a 16 bit word section and ZC_0 corresponds to lower byte.

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Table 1 : PIN DESCRIPTIONS CON'T

Symbol	Type	Name and Function
$ACCEPT_{1-0}$	I	**Accept Control Data Bits :** Set high to ACCEPT an 8 bit field of data in a window. $ACCEPT_1$ corresponds to the upper byte of a 16 bit word section and $ACCEPT_0$ corresponds to the lower byte.
Comparator Control		
FF_{1-0}	I	**Field Format :** 2 inputs signals decoded to determine how the 32 bit parameter data will be processed.
EN64	I	**64 Bit Enable :** Set high to perform a 64 bit compare. The 64 bit compare consists of the ANDed output of 2 adjacent windows over 2 ACLK cycles. There is still 32 match outputs from the array with every second output grounded.
FD_{3-0}	I	**Field Disables :** To permit any byte(s) in the input data to be ignored in generating a match output. The disabled field (FD_3 for upper most byte, FD_0 for lower most byte) is masked out for all 32 windows. All four lines will be functional only in the 4 x 8 bit input data field format. These signals can be used in conjunction with the Field Enables FxENBL.
MDETECT	O	**Match Detect :** A high output indicates that there is a minimum of one active match output.
Sequential Priority Encoder Control		
BCLK	I	**Clock B :** Input clock (12.5 MHz maximum). Loads the state of the match outputs into the sequential priority encoder on the rising edge.
LDINDATA	I	**Load Input Data :** On the rising edge of BCLK causes match output data to be stored in the sequential priority encoder.
OSI	I	**Output Sequence Inhibit :** A high causes the sequential priority encoder to remain in its current state. A low causes a sequence of match addresses for active match signals to be generated, one on each rising edge of BCLK.
RESET	I	**Synchronous Reset :** A high causes the sequential priority encoder to be reset on a rising edge of BCLK.
AEXPIN	I	**A Expansion In :** Allows additional CA29C632As to be cascaded in the vertical direction. Set high in a single chip system.
BEXPIN	I	**B Expansion In :** Allows additional CA29C632As to be cascaded in the vertical direction. Set high in a single chip system.
MAENBL	I	**Match Address Output Enable :** A high causes MADDR to operate with active pullup and pulldown. A low causes MADDR to operate in the high impedance mode.
Sequential Priority Encoder Output		
AEXPOUT	O	**A Expansion Out :** Allows additional CA29C632As to be cascaded in the vertical direction.
BEXPOUT	O	**B Expansion Out :** Allows additional CA29C632As to be cascaded in the vertical direction.
VLDOUT	O	**Valid Output :** A high signal indicates that the address is valid.
LSTVLDOUT	O	**Last Valid Output :** A high signal indicates that the current match address output is the last valid output.
$MADDR_{4-0}$	O	**Match Address Bus :** When the VLDOUT signal is high this bus gives the *complement* of the relative address of an active match output signal from the lowest value to the highest value.
V_{DD}	-	**Power :** 5V ±10% DC power supply. All power pins must be connected to this supply.
GND	-	**Ground :** 0 V DC. All ground pins must be connected to ground.

Table 2 : AC CHARACTERISTICS, CLOCK PARAMETERS (T_A = 0 to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Limits		Units
		Min	Max	
t_{PWH}	High pulse width	35		ns
t_{PWL}	Low pulse width	35		ns
t_{CLK}	Clock period	80		ns
t_R,t_F	Clock rise and fall time	0	10	ns

Table 3 : AC CHARACTERISTICS, PARM DATA / MATCH BUS TIMING (T_A = 0 to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Limits		Units
		Min	Max	
t_{PESCA}	Parameter data / Match enable ((PD/$\overline{M}$)ENBL) setup to Clock A (ACLK) ↑	5		ns
t_{PEHCA}	Parameter data / Match enable ((PD/$\overline{M}$)ENBL) hold from Clock A (ACLK) ↑	5		ns
t_{PSCA}	Parameter data (PD/M) setup to Clock A (ACLK) ↑	5		ns
t_{PHCA}	Parameter data (PD/M) hold from Clock A (ACLK) ↑	5		ns
t_{FESCA}	Field enable (FxENBL) setup to Clock A (ACLK) ↑	5		ns
t_{FEHCA}	Field enable (FxENBL) hold from Clock A (ACLK) ↑	5		ns
t_{FSCA}	Field format (FF) setup to Clock A (ACLK) ↑	5		ns
t_{FHCA}	Field format (FF) hold from Clock A (ACLK) ↑	5		ns
t_{DSCA}	Field disable (FD) setup to Clock A (ACLK) ↑	5		ns
t_{DHCA}	Field disable (FD) hold from Clock A (ACLK) ↑	5		ns
t_{PELBC}	Parameter data / Match enable ((PD/$\overline{M}$)ENBL) ↓ to PD/M bus changing		15	ns
t_{CAMV}	Clock A (ACLK) ↑ to valid match outputs on PD/M bus		55	ns
t_{CAMC}	Clock A (ACLK) ↑ to change in match detect (MDETECT)		60	ns

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Figure 3 : CLOCK PARAMETERS

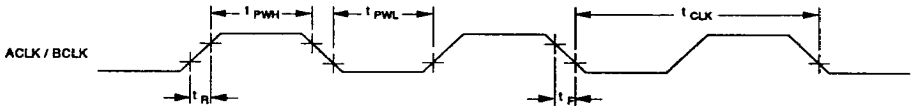
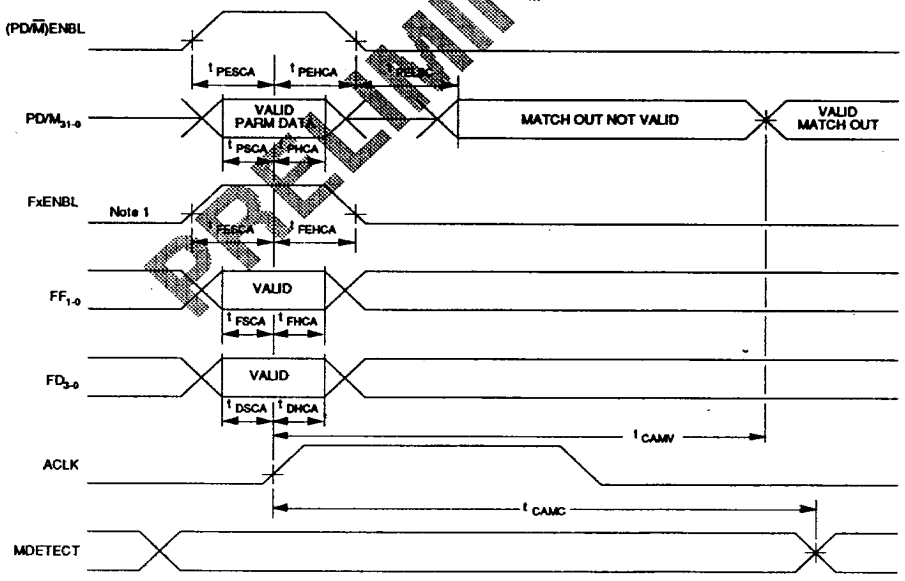


Figure 4 : PARAMETER DATA / MATCH BUS



Notes : 1. FxENBL implies F1ENBL, F2ENBL, F3ENBL, and/or F4ENBL

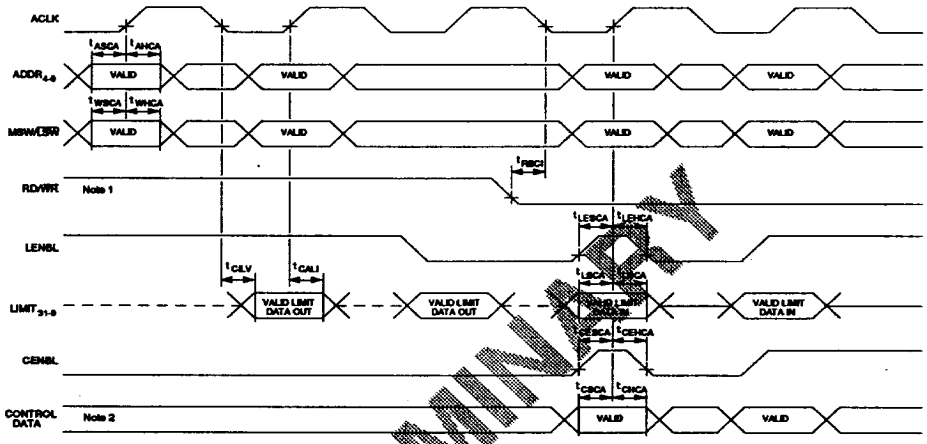
Table 4 : AC CHARACTERISTICS, LIMIT/CONTROL DATA : READ/WRITE TIMING
(T_A = 0 to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Limits		Units
		Min	Max	
t_{ASCA}	Address bus (ADDR) setup to Clock A (ACLK) ↑	5		ns
t_{AHCA}	Address bus (ADDR) hold from Clock A (ACLK) ↑	5		ns
t_{WSCA}	MSW/$\overline{LSW}$ setup to Clock A (ACLK) ↑	5		ns
t_{WHCA}	MSW/$\overline{LSW}$ hold from Clock A (ACLK) ↑	5		ns
t_{RSCI}	RD/$\overline{WR}$ setup to Clock A (ACLK) ↓	5		ns
t_{CESCA}	Control enable (CENBL) setup to Clock A (ACLK) ↑	5		ns
t_{CEHCA}	Control enable (CENBL) hold from Clock A (ACLK) ↑	5		ns
t_{CSCA}	Control data setup to Clock A (ACLK) ↑	5		ns
t_{CHCA}	Control data hold from Clock A (ACLK) ↑	5		ns
t_{LESCA}	Limit enable (LENBL) setup to Clock A (ACLK) ↑	5		ns
t_{LEHCA}	Limit enable (LENBL) hold from Clock A (ACLK) ↑	5		ns
t_{LSCA}	Limit bus setup to Clock A (ACLK) ↑ during a write operation	5		ns
t_{LHCA}	Limit bus hold from Clock A (ACLK) ↑ during a write operation	5		ns
t_{CILV}	Valid limit bus data from Clock A (ACLK) ↓ during a read operation		35	ns
t_{CALI}	Invalid limit bus data from Clock A (ACLK) ↑ during a read operation		10	ns

Table 5 : AC CHARACTERISTICS, 64 BIT COMPARE TIMING (T_A = 0 to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

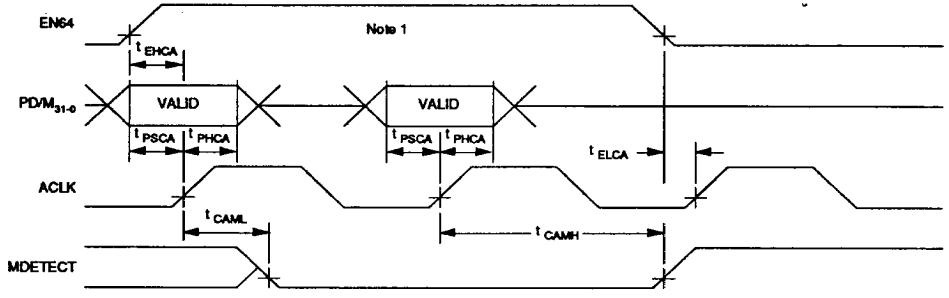
Symbol	Parameter	Limits		Units
		Min	Max	
t_{EHCA}	EN64 ↑ setup to Clock A (ACLK) ↑	5		ns
t_{ELCA}	EN64 ↓ setup to Clock A (ACLK) ↑	5		ns
t_{PSCA}	Parameter data (PD/M) setup to Clock A (ACLK) ↑	5		ns
t_{PHCA}	Parameter data (PD/M) hold from Clock A (ACLK) ↑	5		ns
t_{CAML}	Clock A (ACLK) ↑ to match detect (MDETECT) ↓		10	ns
t_{CAMH}	Clock A (ACLK) ↑ to match detect (MDETECT) ↑		60	ns

Figure 5 : LIMIT/CONTROL DATA (READ/WRITE)



Notes : 1. Transition only while limit enable is low.
2. Control data (NOT, ACCEPT, ZC, and REJECT) is write only.

Figure 6 : 64 BIT COMPARE



Notes : 1. EN64 must be high for a multiple of 2 ACLK cycles for proper 64 bit comparison operation.

Table 6 : AC CHARACTERISTICS, SEQUENTIAL PRIORITY ENCODER (SPE) TIMING
(T_A = 0 to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Limits		Units
		Min	Max	
t_{LSCB}	LDINDATA setup to Clock B (BCLK) ↑	5		ns
t_{LHCB}	LDINDATA hold from Clock B (BCLK) ↑	5		ns
t_{RSCB}	RESET setup to Clock B (BCLK) ↑	5		ns
t_{RHCB}	RESET hold from Clock B (BCLK) ↑	5		ns
t_{OSCB}	OSI setup to Clock B (BCLK) ↑	5		ns
t_{OHCB}	OSI hold from Clock B (BCLK) ↑	5		ns
t_{MLMZ}	MAENBL ↓ to MADDR bus tri-stating		15	ns
t_{MHMV}	MAENBL ↑ to MADDR bus valid		20	ns
t_{CBVL}	Clock B (BCLK) ↑ to VLDOUT ↓		30	ns
t_{CBVH}	Clock B (BCLK) ↑ to VLDOUT ↑		30	ns
t_{CBLL}	Clock B (BCLK) ↑ to LSTVLDOUT ↓		35	ns
t_{CBLH}	Clock B (BCLK) ↑ to LSTVLDOUT ↑		35	ns
t_{CBML}	Clock B (BCLK) ↑ to MADDR ↓ on reset		35	ns
t_{CBMC}	Clock B (BCLK) ↑ to MADDR bus changing		35	ns

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Table 7 : AC CHARACTERISTICS, SPE EXPANSION TIMING (T_A = 0 to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Limits		Units
		Min	Max	
t_{ALBL}	AEXPIN ↓ to BEXPOUT ↓		10	ns
t_{AHBH}	AEXPIN ↑ to BEXPOUT ↑		10	ns
t_{BLAL}	BEXPIN ↓ to AEXPOUT ↓		10	ns
t_{BHAH}	BEXPIN ↑ to AEXPOUT ↑		10	ns
t_{CBBL}	Clock B (BCLK) ↑ to BEXPOUT ↓		45	ns
t_{CBAL}	Clock B (BCLK) ↑ to AEXPOUT ↓		45	ns
t_{CBBH}	Clock B (BCLK) ↑ to BEXPOUT ↑		45	ns
t_{CBAH}	Clock B (BCLK) ↑ to AEXPOUT ↑		45	ns

Figure 7 : SEQUENTIAL PRIORITY ENCODER (SPE)

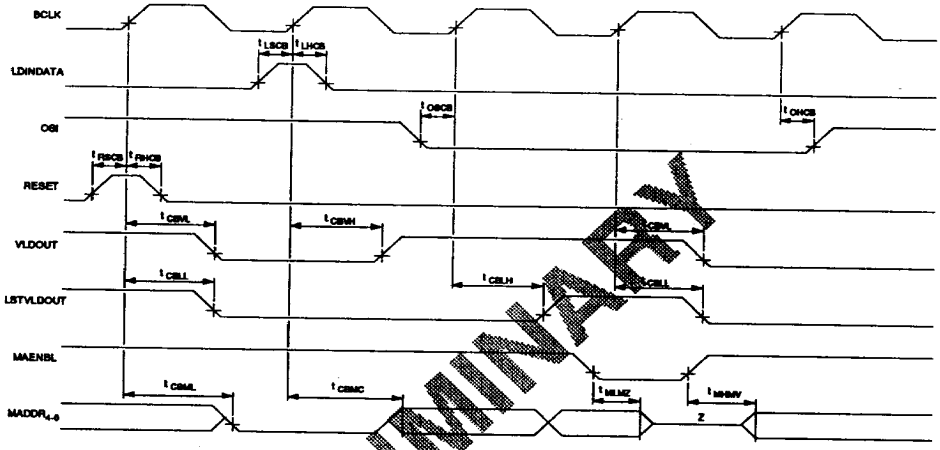
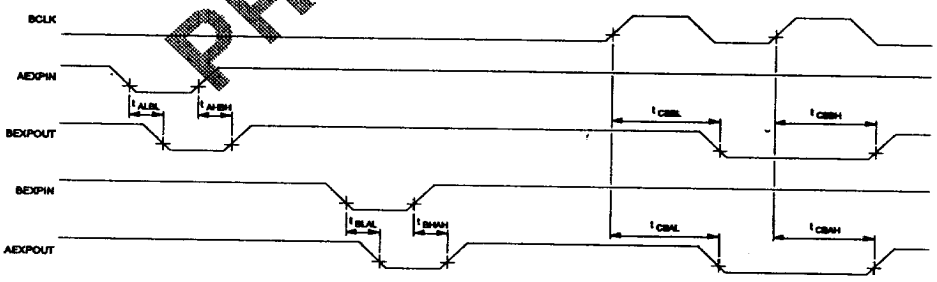
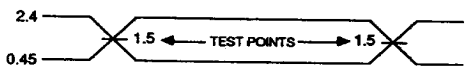


Figure 8 : SPE EXPANSION





AC Testing Inputs are driven at 2.4V for a Logic 1 and 0.45V for a Logic 0. Timing measurements are made at 1.5V for a logic 1 and 1.5V for a Logic 0.

Figure 9: AC TESTING I/O WAVEFORM

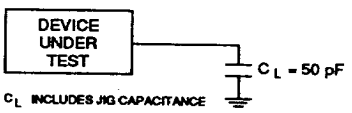


Figure 10: AC TESTING LOAD CIRCUIT

Table 8 : DC CHARACTERISTICS (T_A = 0 to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{LIH}	Input leakage current high	$V_{IN} = V_{DD}$		10	µA
I_{LIL}	Input leakage current low (inputs and bidirectionals)	V_{IN} = 0V		–100	µA
I_{LOH}	Output leakage current high	$V_{OUT} = V_{DD}$		10	µA
I_{LOL}	Output leakage current low	V_{OUT} = 0V	0	–10	µA
V_{IH}	Input voltage high		2.0	V_{DD}+0.3	V
V_{IL}	Input voltage low		–0.5	0.8	V
V_{OH}	Output voltage high	I_{OH} = –400 µA	2.4		V
V_{OL}	Output voltage low	I_{OL} = 2.5 mA		0.4	V
	Supply current operating	Clock freq. = 12.5 MHz		200	mA

Table 9 : CAPACITANCE (T_A = 25°C , V_{DD} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
C_{IN}	Input capacitance	Unmeasured pins		10	pF
C_{OUT}	I/O Capacitance	Returned to GND		20	pF

Table 10 : RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage		+4V to +6V
Operating Temperature Range	Commercial	0 to 70°C
	Industrial	–40 to +85°C

Table 11 : ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage (V_{DD})	–0.5V to +7.0V
Power Dissipation (PD_{MAX})	0.5 Watt
Operating Temperature (T_{OPT})	0 to 70°C
Storage Temperature (T_{STG})	–65 TO +150°C

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

FUNCTIONAL DESCRIPTION

The CA29C632A, as shown in Figure 1, is a Window Addressable Memory that consists of 32 windows of width 32 bits. Each window contains a programmable upper and lower limit. Parameter data of width 32 bits is processed by all 32 windows simultaneously to provide 32 window match results based on the parameter data being within the preset upper and lower limits. Provisions are provided to operate on the parameter data in smaller bit formats as well as to control the window based on several control bits. Detailed operation of a window is described in the section *Window Operation*. Parameter data may be processed every 80 ns for an effective clock frequency of 12.5 MHz. Match output results are then presented to the priority encoder which will prioritize any active match outputs, from highest to lowest, in a 5 bit encoded match output. Detailed operation of the priority encoder is described in the section *Sequential Priority Encoder (SPE)*. All bidirectional and input pins contain on chip resistors to pull any unconnected inputs to a valid state.

WINDOW OPERATION

The comparator array consists of 32 windows of width 32 bits. Each window is essentially identical in operation except for the 64 bit comparison function, which is described in the section *64 Bit Comparison Operation*. Within each window there is a 32 bit upper limit register, 32 bit lower limit register, four 8 bit comparators, 13 control data bit registers, and combinational logic to produce the final window match result (see Figure 1). The default mode of operation, *compare within limits*, is defined by the equation:

Match Output = (Parameter Data ≤ Upper Limit
AND
Parameter Data ≥ Lower Limit)

The match outputs from all 32 windows are ORed together to produce the MDETECT output. MDETECT when high indicates that there is a minimum of one active match output. Details relating to limit data are given in the section *Reading and Writing Limit Data*.

Table 12 : FIELD FORMAT OPTIONS

FF_1	FF_0	Parameter Data Processed As
1	1	One 32 bit word (32)
1	0	Two 16 bit words (1616)
0	1	One 16 bit word and two 8 bit words (1688)
0	0	Four 8 bit words (8888)

Field Format

A number of input signals define the operation of all 32 windows. Input signals FF_{1-0}, the field format signals, determine how the parameter data will be processed, according to Table 12. FF_{1-0} are latched on the rising edge of ACLK. Figure 11 illustrates the possible field formats.

Field Disable

Inputs FD_{3-0}, the field disable signals, when high allow any 8 bit section in the parameter data to be ignored (masked out) in the generation of the window match result. FD_3 corresponds to the upper most byte of parameter data, PD/M_{31-24}, and FD_0 corresponds to the lower most byte of parameter data, PD/M_{7-0}. The field disables are only active as shown in Table 13. FD_{3-0} are latched on the rising edge of ACLK.

Table 13 : FIELD DISABLE OPTIONS

	FD_3	FD_2	FD_1	FD_0
32 bit compare	1	X	X	X
1616 bit compare	1	X	1	X
1688 bit compare	1	X	1	1
8888 bit compare	1	1	1	1

Control Data

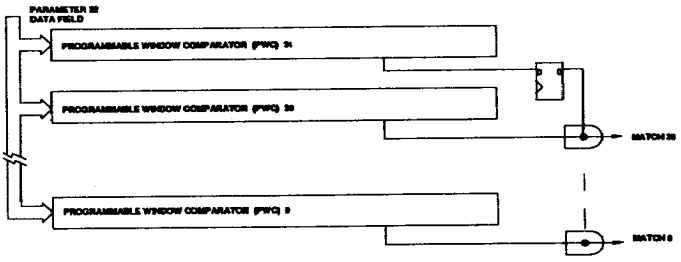
All 32 windows are individually programmable providing several modes of operation. Each 8 bit section of a window contains programmable control data bits (described below) for ZERO CROSSOVER (ZC), ACCEPT, and NOT. The REJECT control data bit is valid for the entire window. See section *Writing Control Data* for details on writing to each 8 bit section.

Zero Crossover Compare Within Limits : This mode allows a window to be defined which wraps around zero and full scale. The logic performed is defined by the equation :

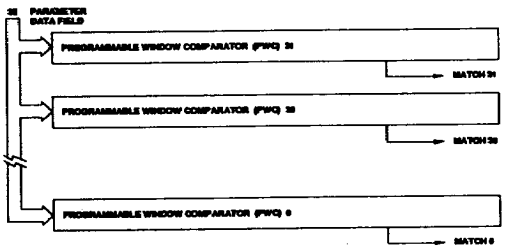
Match Output = (Parameter Data ≤ Upper Limit
OR
Parameter Data ≥ Lower Limit)

This function is enabled by setting the ZERO CROSSOVER bit in the control register to a logic 1 value.

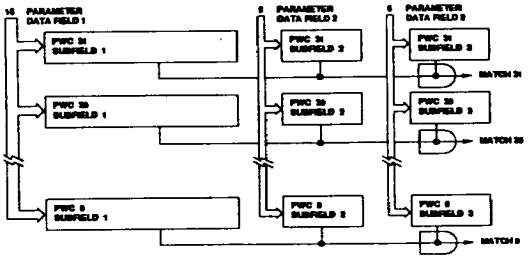
Not Compare : This function negates the programmable window comparator output expected from either of the preceding modes. It is enabled by programming the NOT bit in the control register to a logic 1 value.



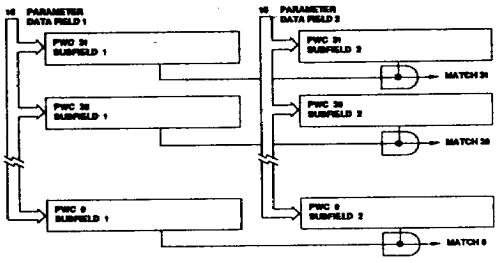
a) 64 - Bit Field Format



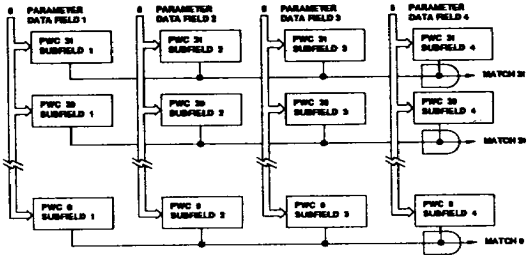
b) 32 - Bit Field Format



d) 16/8/8 - Bit Field Format



c) 16/16 - Bit Field Format



e) 8/8/8/8 - Bit Field Format

Note: Sequential priority encoders are not shown

Figure 11 : WINDOW COMPARATOR FIELD FORMATS

Accept : This function forces the output of the programmable window comparator to a logic 1 value. It is enabled by programming the ACCEPT bit in the control register to a logic 1 value.

Reject : This function forces the output of the programmable window comparator to a logic 0 value. It is enabled by programming the REJECT bit in the control register to a logic 1 value.

Special care should be taken in programming the control data bits. For instance, setting the ACCEPT and NOT bits for an 8 bit section of a window will reject that field of data, and will therefore reject that entire window. The order of precedence of the control bits is as follows (highest to lowest) : REJECT, NOT, ACCEPT, ZC.

Table 14 : 32 BIT COMPARE

	Field			
	4	3	2	1
Accept	1	X	X	X
Zero Crossover	1	X	X	X
Not	1	X	X	X

Table 15 : 1616 BIT COMPARE

	Field			
	4	3	2	1
Accept	1	X	1	X
Zero Crossover	1	X	1	X
Not	1	X	1	X

Table 16 : 1688 BIT COMPARE

	Field			
	4	3	2	1
Accept	1	X	1	1
Zero Crossover	1	X	1	1
Not	1	X	1	1

Table 17 : 8888 BIT COMPARE

	Field			
	4	3	2	1
Accept	1	1	1	1
Zero Crossover	1	1	1	1
Not	1	1	1	1

All of the 13 control data bits will only be active in the 8888 field format. The active bits for the field formats are illustrated in Tables 14 – 17.

64 BIT COMPARISON OPERATION

A 64 bit comparison operation may be performed through the setting of the EN64 input. When EN64 is set high, 64 bit comparison mode is enabled. A 64 bit comparison consists of the ANDing of two adjacent window match results over two clock cycles (see Figure 11a) 64 - Bit Field Format). EN64 must be high for a multiple of 2 ACLK cycles for proper operation in this mode. EN64 is latched on the rising edge of ACLK. A high latched value will set all 32 window match outputs low. The first piece of parameter data will be processed by an odd numbered window and the second and final piece of parameter data will be processed by an even numbered window. Only 16 match outputs will be valid, those being the even numbered match outputs: Match<30>, Match<28>, ..., Match<2>, and Match<0>. The odd numbered match outputs : Match<31>, Match<29>, ..., Match<3>, and Match<1> will always be low. The internal Match bus is passed to the Sequential Priority Encoder (SPE) in addition to being used to produce the MDETECT output. The process of performing a 64 bit compare is illustrated in Figure 6.

READING AND WRITING LIMIT DATA

The $LIMIT_{31-0}$ bus is a bidirectional bus used to read and write upper and lower limit data to the 32 windows. Limit data is written-to or read-from a 16 bit MSW/LSW section of a window. The organization of the data is: $LIMIT_{31-16}$ corresponds to 16 bits of upper limit data and $LIMIT_{15-0}$ corresponds to 16 bits of lower limit data. During a write, the upper limit data is written when ACLK is high and the lower limit data is written when ACLK is low. This has the advantage of reprogramming a complete 16 bit section of upper and lower limit data for a window in one clock cycle. Therefore to completely program the upper and lower limits for a window, two clock cycles are required.

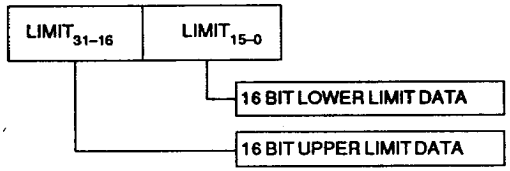


Figure 12 : LIMIT DATA BUS

Reading of limit data is performed in much the same manner. After a read has completed, $LIMIT_{31-16}$ will correspond to 16 bits of upper limit data and $LIMIT_{15-0}$ will correspond to 16 bits of lower limit data. Limit data will only be valid at the end of the read cycle.

Limit data is written on the rising edge of ACLK in the following manner: $LIMIT_{31-0}$, the limit data bus, must contain valid limit data; LENBL, the limit enable signal, must be high; $ADDR_{4-0}$ must reflect the window address to be programmed and MSW/$\overline{LSW}$ must be set to the 16 bit section of the window to be programmed. Reading is performed in exactly the same manner. RD/$\overline{WR}$ is latched on the falling edge of ACLK, it may only be changed when LENBL is low. The process of reading and writing limit data is illustrated in Figure 5.

WRITING CONTROL DATA

The control data bits $ACCEPT_{1-0}$, ZC_{1-0}, NOT_{1-0} and REJECT are write only, no provisions for reading are available, as in the case of limit data. Control data is written on the rising edge of ACLK in the following manner: CENBL, the control enable signal, must be high; RD/$\overline{WR}$ must be low for writing (latched on falling edge of ACLK); $ADDR_{4-0}$ must reflect the window address to be programmed; MSW/$\overline{LSW}$ must be set to the 16 bit section of the window to be programmed and the correct control data must be on $ACCEPT_{1-0}$, ZC_{1-0}, NOT_{1-0} and REJECT. Each 8 bit section's control data is derived from Figure 13.

The REJECT bit rejects the entire window so it may be programmed by either MSW or LSW, i.e. the state of MSW/$\overline{LSW}$ has no effect. Since only the control data for MSW or LSW may be programmed in a single ACLK cycle, two ACLK cycles are required to program the control data for a complete window. The process of writing control data is illustrated in Figure 5.

PARAMETER DATA / MATCH OUTPUT BUS

The 32 bit PD/M bidirectional bus is used to input parameter data to the CA29C632A. The input signal (PD/$\overline{M}$)ENBL controls the direction of this bus. When (PD/$\overline{M}$)ENBL is set high, the PD/M bus is set for input of parameter data. When (PD/$\overline{M}$)ENBL is set low, the internal MATCH bus, representing the 32 window match results, is enabled for output. Note that Limit Enable (LENBL) and Control Enable (CENBL) must be inactive in order to get a valid match output.

Parameter data is written to a 32 bit parameter data register. This data is presented to all 32 windows and may be configured in the following manner : four 8 bit bytes comprise the parameter data register, each 8 bit byte has a field enable pin associated with it, F1ENBL for the lower most byte proceeding to F4ENBL for the upper most byte. To load data into a particular 8 bit byte, (PD/$\overline{M}$)ENBL must be high and the field enable FxENBL must be high. Data will be loaded into the register on the rising edge of ACLK. If these conditions are not met, the register's contents remains unchanged. (PD/$\overline{M}$)ENBL and FxENBL are latched on the rising edge of ACLK. The parameter data/match output bus is illustrated in Figure 4.

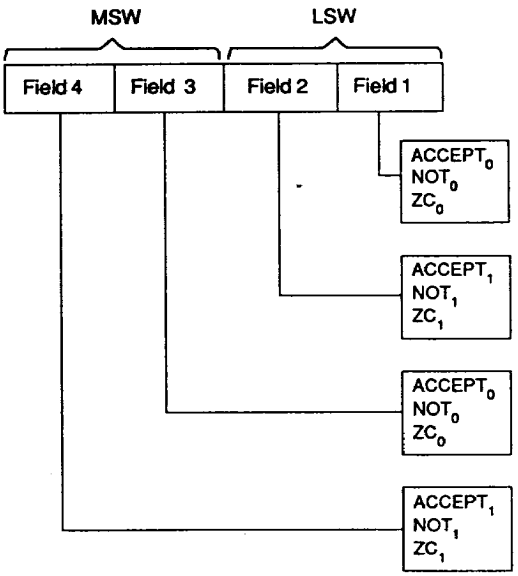


Figure 13 : CONTROL DATA PROGRAMMING

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SPECIAL OPERATING NOTE

Although programming limit/control data and processing parameter data are essentially separate tasks, they may still be performed during the same clock cycle. Since only one window may be programmed during a clock cycle, only 31 windows will contain valid match output results while the window being programmed will have its match output set low. This is to prevent an incorrect match output from being generated due to the simultaneous actions of processing parameter data and writing limit and/or control data.

SEQUENTIAL PRIORITY ENCODER (SPE)

The sequential priority encoder (SPE) will encode 5 bit addresses for active match outputs from the internal MATCH bus onto $MADDR_{4-0}$. The SPE is completely synchronous with all transitions occuring on the rising edge of BCLK. The SPE may be clocked at a maximum frequency of 12.5 MHz for a clock period of 80 ns, equal to the maximum clock frequency of ACLK. Figure 1 depicts how the SPE is incorporated into the CA29C632A. In situations where only one active match is expected, the SPE may be pipelined with the comparator array. In this case parameter data is processed and the match is encoded by the SPE in an 80 ns clock period.

Window match data on the internal MATCH bus is presented to the SPE each clock cycle that LDINDATA, the load in data signal, is high. Figure 7 illustrates the timing relationships of the SPE. A low on LDINDATA causes no new data to be processed by the SPE. The highest active window match result (ie: window 31 is lowest and window 0 is highest) is encoded and output on $MADDR_{4-0}$. Two additional output signals are provided. VLDOUT, the valid output signal, when high indicates that there is a valid match output from the SPE. LSTVLDOUT, the last valid output signal, when high indicates that the present encoded match output is the last valid match output from the SPE, since the SPE can store more than one active match. LSTVLDOUT provides advance notice of the last active match result thereby saving one additional clock cycle, which normally would be used to detect that the SPE was empty if the LSTVLDOUT signal was not provided. VLDOUT will remain high as long as there is valid match output data. The SPE will be reset and all storage elements cleared when RESET is set high. Reset will occur on the rising edge of BCLK.

Multiple match capability is provided for in the CA29C632A. More than one active match output is indicated by VLDOUT high and LSTVLDOUT low after the match outputs have been loaded into the SPE through LDINDATA being set high. The output sequence inhibit signal, OSI, is provided to cycle the remaining match outputs out of the SPE. OSI provides the capability to operate the SPE in systems that utilize wait state operations. It can be used as a handshaking signal to permit the generation of the next match address at the time when it can be used. OSI is set high to suppress lower prioritized outputs on MADDR, usually when data is loaded into the SPE via LDINDATA. OSI is then set low to cycle out on MADDR the next highest prioritized match output address. Figure 7 depicts this process. For each BCLK cycle that OSI is low the next highest prioritized match output address is presented on MADDR until all addresses have been cycled out. LSTVLDOUT will only be high on the last address while VLDOUT will be high the entire time. VLDOUT and LSTVLDOUT will then go low on the first clock cycle after the last address has been cycled out.

The priority of the SPE control signals (from highest to lowest) is as follows: RESET, LDINDATA and OSI. The highest active prioritized control signal will override any lower active control signals, hence there are no illegal combinations of SPE control signals.

The encoded match address bus, MADDR, is tristateable to enable cascading of multiple CA29C632As. A high on MAENBL, the match address output enable, will enable the MADDR bus while a low will tristate the bus. In a cascaded system, the MADDR bus will be connected to all CA29C632As. The VLDOUT signal will be used to connect to the MAENBL pin indicating that there is a valid match output and therefore the MADDR bus should be enabled for that CA29C632A alone. Multiple CA29C632As are connected via the expansion pins AEXPIN, AEXPOUT, BEXPIN, and BEXPOUT. In a single chip system AEXPIN and BEXPIN are connected high. In a cascaded multichip system, adjacent CA29C632As are connected as shown in Figure 14.

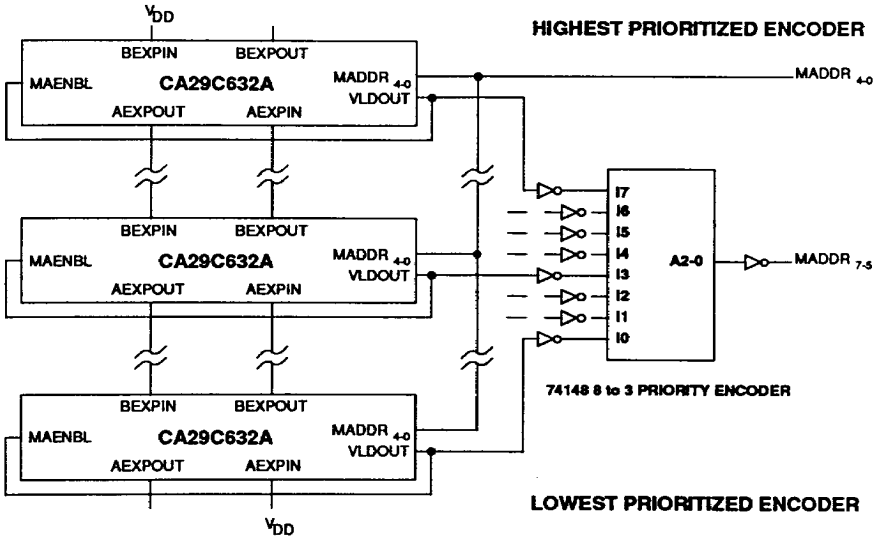

Figure 14 : CASCADING MULTIPLE CA29C632A DEVICES

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