256Kx16 PLASTIC MONOLITHIC SRAM

FEATURES

- 256Kx16 bit CMOS Static
- Random Access Memory
  - Access Times of 15, 17, 20, 25ns
  - Data Retention Function (LPA version)
  - TTL Compatible Inputs and Outputs
  - Fully Static, No Clocks
- Center Power/Ground Pins (Revolutionary)
- 44 lead JEDEC Approved Revolutionary Pinout
  - Plastic SOJ Package
- Single +5V (±10%) Supply Operation

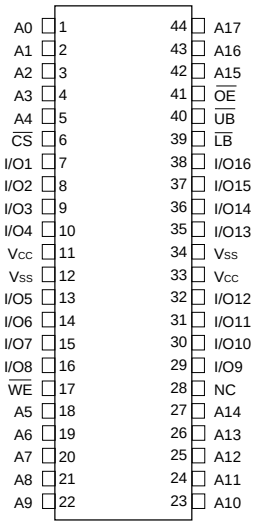
The EDI816256CA is a ruggedized plastic 256Kx16 SRAM that allows the user to capitalize on the cost advantage of using a plastic component while not sacrificing all of the reliability available in a full military device.

The EDI816256CA uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device allows upper and lower byte access by use of the data byte control pins ($\overline{LB}$, $\overline{UB}$).

Extended temperature testing is performed with the test patterns developed for use on WEDC's fully compliant 256Kx16 SRAMs. WEDC fully characterizes devices to determine the proper test patterns for testing at temperature extremes. This is critical because the operating characteristics of device change when it is operated beyond the commercial guarantee a device that operates reliably in the field at temperature extremes. Users of WEDC's ruggedized plastic benefit from WEDC's extensive experience in characterizing SRAMs for use in military systems.

WEDC ensures Low Power devices will retain data in Data Retention mode by characterizing the devices to determine the appropriate test conditions. This is crucial for systems operating at -40°C or below and using dense memories such as 256Kx16s.WEDC's ruggedized plastic SOJ is footprint compatible with WEDC's full military ceramic 44 pin SOJ.

PIN CONFIGURATION
TOP VIEW



PIN DESCRIPTION

A_{0-17}	Address Inputs
$\overline{LB}$	Lower-Byte Control (I/O_{1-8})
$\overline{UB}$	Upper-Byte Control (I/O_{9-16})
I/O_{1-16}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	+5.0V Power
V_{SS}	Ground
NC	No Connection

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	Data I/O		Power
						I/O_{1-8}	I/O_{9-16}	
H	X	X	X	X	Not Select	High Z	High Z	Standby
L	H	H	X	X	Output Disable	High Z	High Z	Active
L	X	X	H	H				
L	H	L	L	H	Read	Data Out	High Z	Active
			H	L		High Z	Data Out	
			L	L		Data Out	Data Out	
L	L	X	L	H	Write	Data In	High Z	Active
			H	L		High Z	Data In	
			L	L		Data In	Data In	

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature (Mil.)	T_A	-55	+125	°C
Operating Temperature (Ind.)	T_A	-40	+85	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to V_{SS}	V_G	-0.5	Vcc + 0.5	V
Supply Voltage	V_{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Operating Temperature (Mil.)	T_A	-55	+125	°C
Operating Temperature (Ind.)	T_A	-40	+85	°C

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C_{IN}	V_{IN} = 0V, f = 1.0MHz	6	pF
Output capicitance	C_{OUT}	V_{OUT} = 0V, f = 1.0MHz	8	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Sym	Conditions		Min	Max	Units
Operating Power Supply Current	I_{CC1}	$\overline{WE}$, $\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA, Min Cycle		—	300	mA
Standby (TTL) Power Supply Current	I_{CC2}	$\overline{CS}$ ≥ V_{IH}, V_{IN} ≤ V_{IL}, V_{IN} ≥ V_{IH}		—	60	mA
Full Standby Power Supply Current	I_{CC3}	$\overline{CS}$ ≥ V_{CC}-0.2V	CA	—	25	mA
		V_{IN} ≥ V_{CC}-0.2V or V_{IN} ≤ 0.2V	LPA	—	15	mA
Input Leakage Current	I_{LI}	V_{IN} = 0V to V_{CC}		-10	10	µA
Output Leakage Current	I_{LO}	$V_{I/O}$ = 0V to V_{CC}		-10	10	µA
Output High Voltage	V_{OH}	I_{OH} =-4mA		2.4	—	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA		—	0.4	V

AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-15		-17		-20		-25		Units
Read Cycle		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		17		20		25		ns
Address Access Time	t_{AA}		15		17		20		25	ns
Output Hold from Address Change	t_{OH}	0		0		0		0		ns
Chip Select Access Time	t_{ACS}		15		17		20		25	ns
Output Enable to Output Valid	t_{OE}		10		10		10		12	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	5		5		5		5		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		7		7		7		8	ns
Output Disable to Output in High Z	t_{OHZ}[1]		7		7		7		8	ns
$\overline{LB}$, $\overline{UB}$ Access Time	t_{BA}		10		10		10		12	ns
$\overline{LB}$, $\overline{UB}$ Enable to Low Z Output	t_{BLZ}[1]	0		0		0		0		ns
$\overline{LB}$, $\overline{UB}$ Disable to High Z Output	t_{BHZ}[1]		7		7		7		8	ns

1. This parameter is guaranteed by design but not tested.

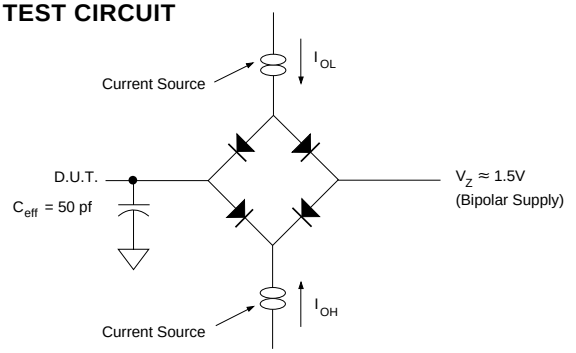
AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-15		-17		-20		-25		Units
Write Cycle		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		17		20		25		ns
Chip Select to End of Write	t_{CW}	12		15		15		17		ns
Address Valid to End of Write	t_{AW}	12		15		15		17		ns
Data Valid to End of Write	t_{DW}	10		10		10		12		ns
Write Pulse Width	t_{WP}	12		15		15		17		ns
Address Setup Time	t_{AS}	0		0		0		0		ns
Address Hold Time	t_{AH}	0		0		0		0		ns
Output Active from End of Write	t_{OW}[1]	0		0		0		0		ns
Write Enable to Output in High Z	t_{WHZ}[1]		8		8		8		8	ns
Data Hold Time	t_{DH}	0		0		0		0		ns
$\overline{LB}$, $\overline{UB}$ Valid to End of Write	t_{BW}	12		15		16		18		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT

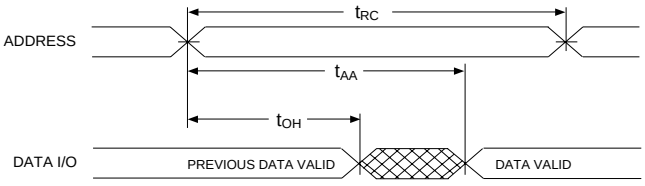


AC TEST CONDITIONS

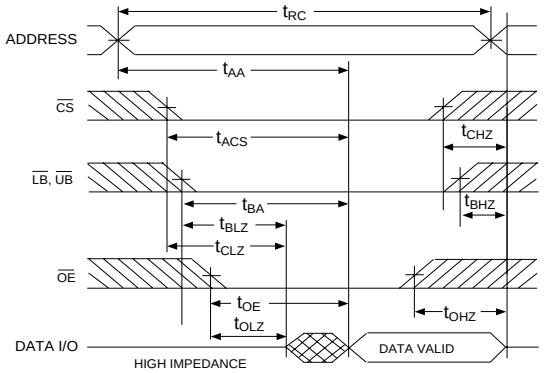
Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

TIMING WAVEFORM - READ CYCLE

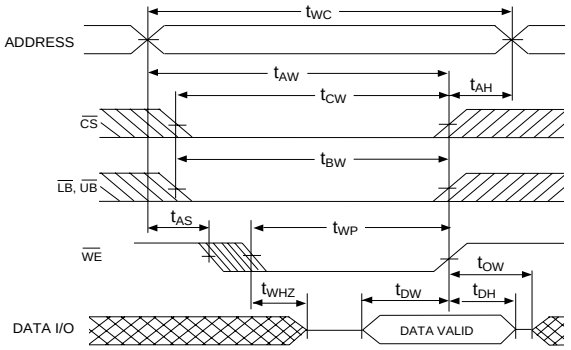


READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL}, $\overline{WE}$ = V_{IH})



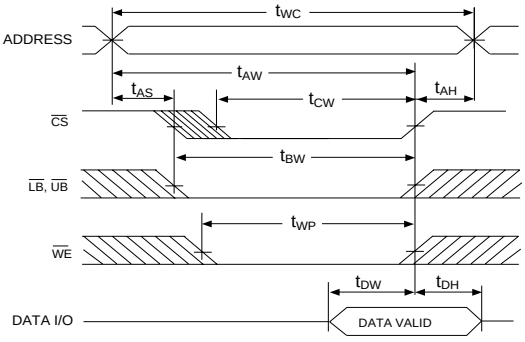
READ CYCLE 2 ($\overline{WE}$ = V_{IH})

WRITE CYCLE - $\overline{WE}$ CONTROLLED



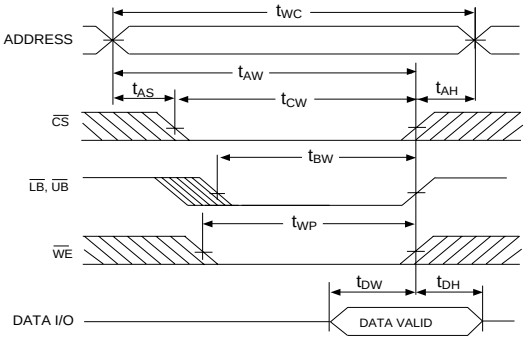
WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

WRITE CYCLE - $\overline{CS}$ CONTROLLED



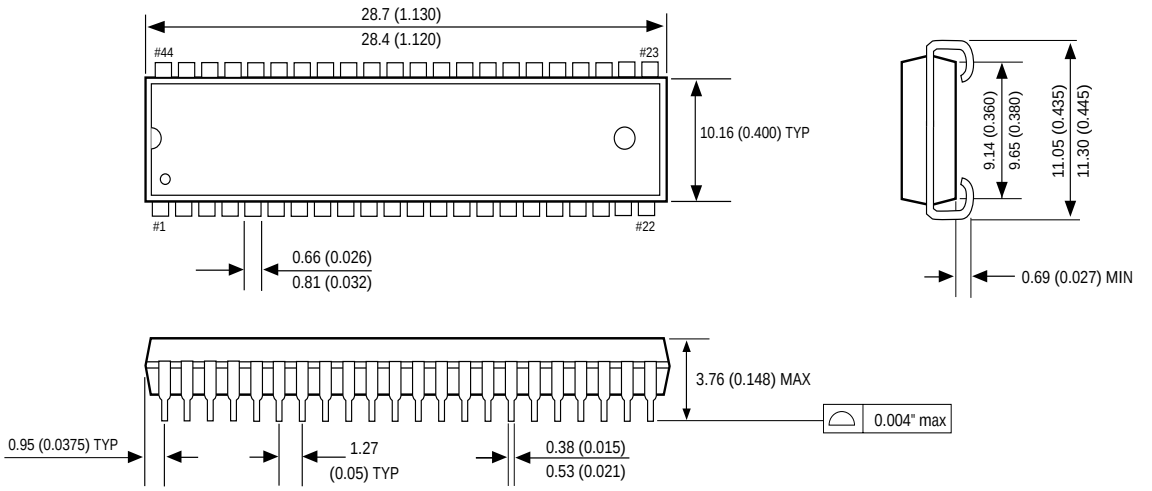
WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

WRITE CYCLE - $\overline{LB}$, $\overline{UB}$ CONTROLLED



WRITE CYCLE 3, $\overline{LB}$, $\overline{UB}$ CONTROLLED

44 LEAD, PLASTIC SOJ (400 mil)



DIMENSIONS IN MILLIMETERS AND (INCHES)

ORDERING INFORMATION

EDI 8 16 256 CA X X X

WHITE ELECTRONIC DESIGNS

SRAM

ORGANIZATION, 256Kx16

TECHNOLOGY:
CA = CMOS Standard Power
LPA = Low Power

ACCESS TIME (ns)

PACKAGE TYPE:
M44 = 44 lead Plastic SOJ

DEVICE GRADE:

B = MIL-STD-883 Compliant	
M = Military Screened	-55°C to +125°C
I = Industrial	-40°C to +85°C
C = Commercial	0°C to +70°C