HM628127HBI Series

131072-word × 8-bit High Speed CMOS Static RAM

HITACHI

ADE-203-785A (Z)
Rev. 1.0
May. 19, 1997

Description

The HM628127HBI is an asynchronous high speed static RAM organized as 128-k word × 8-bit. It realize high speed access time (20 ns) with employing 0.8 µm shrink CMOS process and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. The HM628127HBI is packaged in 400-mil 32-pin SOJ for high density surface mounting.

Features

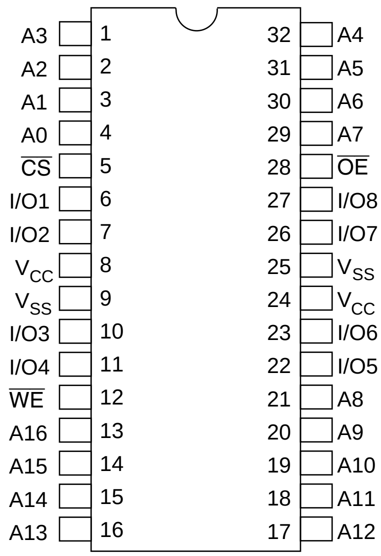
- Single 5 V supply
- Access time 20 ns (max)
- Completely static memory
  — No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible
  — All inputs and outputs
- 400-mil 32-pin SOJ package
- Center V_{CC} and V_{SS} type pinout
- Operating Temperature – 40 to + 85°C

Ordering Information

Type No.	Access time	Package
HM628127HBLJPI-20	20 ns	400-mil 32-pin plastic SOJ (CP-32DB)

Pin Arrangement

HM628127HBLJPI Series

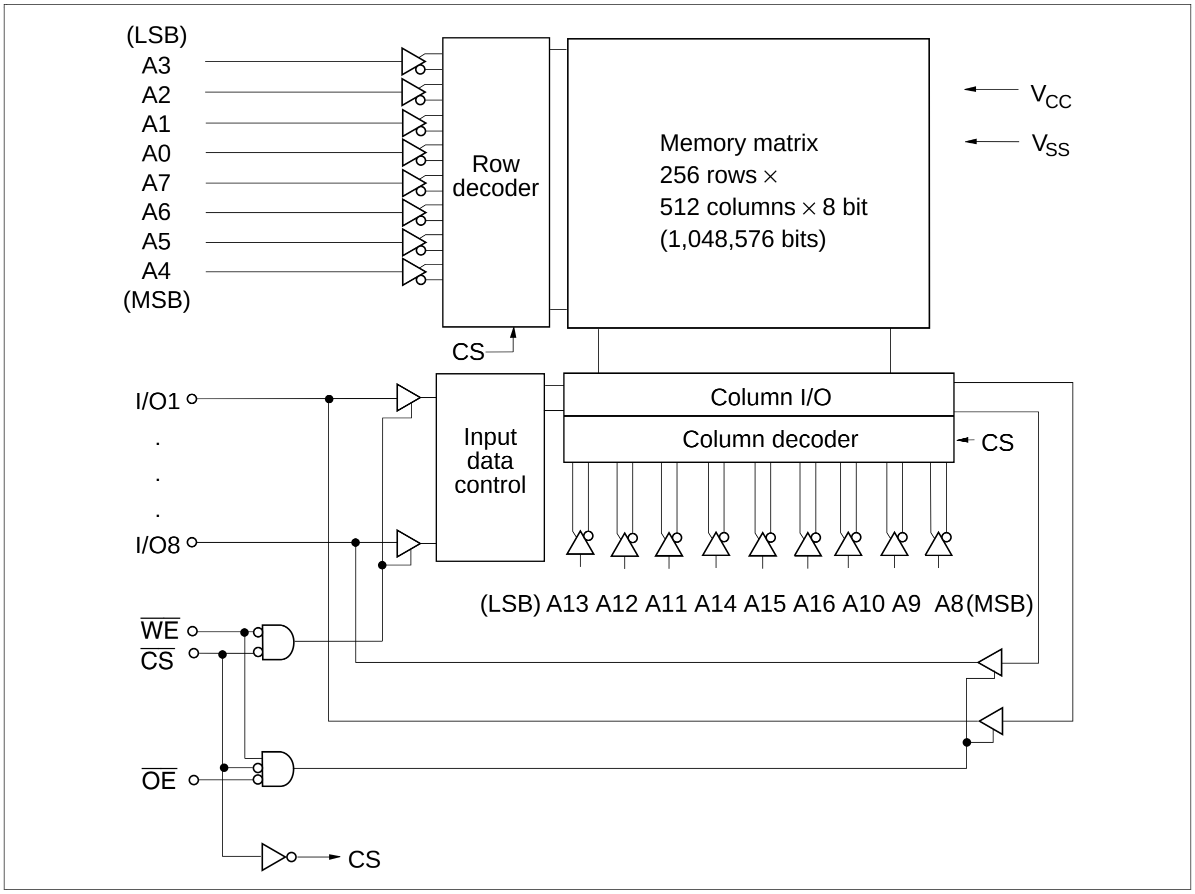


(Top view)

Pin Description

Pin Name	Function
A0 to A16	Address input
I/O1 to I/O8	Data input/output
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} current	I/O	Ref. cycle
H	×	×	Standby	I_{SB}, I_{SB1}	High-Z	—
L	H	H	Output disable	I_{CC}	High-Z	—
L	L	H	Read	I_{CC}	Dout	Read cycle (1) to (3)
L	H	L	Write	I_{CC}	Din	Write cycle (1)
L	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: ×: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +7.0	V
Voltage on any pin relative to V_{SS}	V_T	–0.5*[1] to V_{CC}+0.5	V
Power dissipation	P_T	1.0*[2]/1.5*[3]	W
Operating temperature	Topr	– 40 to + 85	°C
Storage temperature	Tstg	– 55 to + 125	°C
Storage temperature under bias	Tbias	– 40 to + 85	°C

Notes: 1. V_T min = –2.5 V for pulse width (under shoot) ≤ 10 ns
2. At still air condition
3. At air flow ≥ 1.0 m/s

Recommended DC Operating Conditions (Ta = – 40 to + 85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}*[2]	4.5	5.0	5.5	V
	V_{SS}*[3]	0	0	0	V
Input voltage	V_{IH}	2.4	—	V_{CC} + 0.5	V
	V_{IL}	–0.5*[1]	—	0.6	V

Notes: 1. V_{IL} min = –2.0 V for pulse width (under shoot) ≤ 10 ns
2. The supply voltage with all V_{CC} pins must be on the same level.
3. The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics (Ta = – 40 to + 85°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Min	Typ*[1]	Max	Unit	Test conditions
Input leakage current	$\lvert I_{LI} \rvert$	—	—	2	µA	Vin = V_{SS} to V_{CC}
Output leakage current	$\lvert I_{LO} \rvert$	—	—	2	µA	Vin = V_{SS} to V_{CC}
Operation power supply current	I_{CC}	—	100	150	mA	$\overline{CS}$ = V_{IL}, Iout = 0 mA Other inputs = V_{IH}/V_{IL}
Standby power supply current	I_{SB}	—	45	80	mA	$\overline{CS}$ = V_{IH}, Other inputs = V_{IH}/V_{IL}
	I_{SB1}	—	—	0.5	mA	$V_{CC} \geq \overline{CS} \geq V_{CC}$ - 0.2 V, (1) 0 V ≤ Vin ≤ 0.2 V or (2) V_{CC} ≥ Vin ≥ V_{CC} - 0.2 V
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
	V_{OH}	2.4	—	—	V	I_{OH} = –4 mA

Notes: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and not guaranteed.

Capacitance (Ta = 25°C, f = 1.0 MHz)

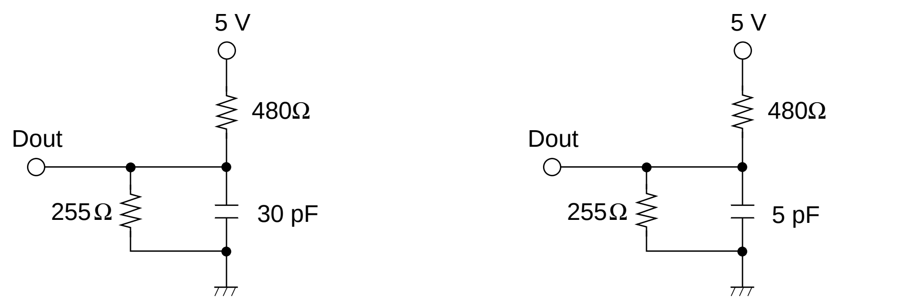
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance*[1]	Cin	—	—	6	pF	Vin = 0 V
Input/output capacitance*[1]	$C_{I/O}$	—	—	8	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = – 40 to + 85°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0 V to 3.5 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.5V
- Output load: See figures (Including scope and jig)



Output load (A)

Output load (B)
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{OW})

Read Cycle

Parameter	Symbol	HM628127HBI-20 Min	Max	Unit	Notes
Read cycle time	t_{RC}	20	—	ns	
Address access time	t_{AA}	—	20	ns	
Chip select access time	t_{ACS}	—	20	ns	
Output enable to output valid	t_{OE}	—	10	ns	
Output hold from address change	t_{OH}	5	—	ns	
Chip select to output in low-Z	t_{CLZ}	3	—	ns	1
Output enable to output in low-Z	t_{OLZ}	1	—	ns	1
Chip deselect to output in high-Z	t_{CHZ}	—	7	ns	1
Output disable to output in high-Z	t_{OHZ}	—	7	ns	1
Chip selection to power up time	t_{PU}	0	—	ns	
Chip selection to power down time	t_{PD}	—	20	ns	

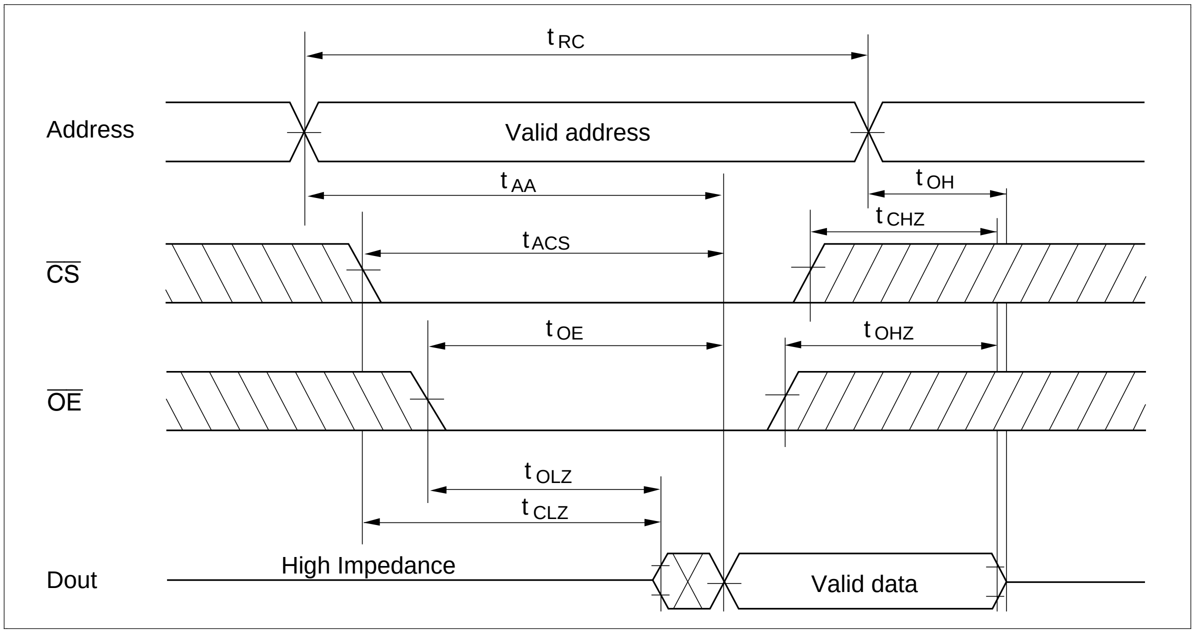
Write Cycle

Parameter	Symbol	HM628127HBI-20 Min	Max	Unit	Notes
Write cycle time	t_{WC}	20	—	ns	
Address valid to end of write	t_{AW}	15	—	ns	
Chip select to end of write	t_{CW}	12	—	ns	9
Write pulse width	t_{WP}	12	—	ns	8
Address setup time	t_{AS}	0	—	ns	6
Write recovery time	t_{WR}	2	—	ns	7
Data to write time overlap	t_{DW}	10	—	ns	
Data hold from write time	t_{DH}	1	—	ns	
Write disable to output in low-Z	t_{OW}	3	—	ns	1
Output disable to output in high-Z	t_{OHZ}	—	7	ns	1
Write enable to output in high-Z	t_{WHZ}	—	7	ns	1

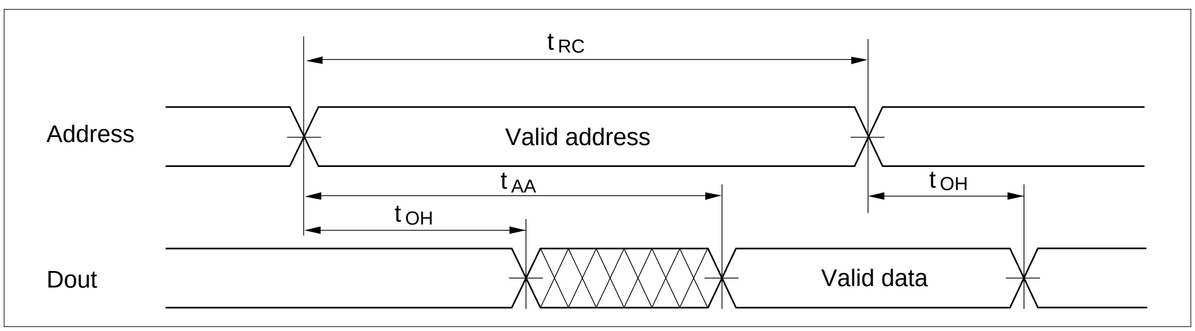
Note:
1. Transition is measured ±200 mV from steady voltage with Load (B). This parameter is sampled and not 100% tested.
2. Address should be valid prior to or coincident with $\overline{CS}$ transition low.
3. $\overline{WE}$ and/or $\overline{CS}$ must be high during address transition time.
4. if $\overline{CS}$ and $\overline{OE}$ are low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains a high impedance state.
6. t_{AS} is measured from the latest address transition to the later of $\overline{CS}$ or $\overline{WE}$ going low.
7. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the first address transition.
8. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
9. t_{CW} is measured from the later of $\overline{CS}$ going low to the end of write.

Timing Waveforms

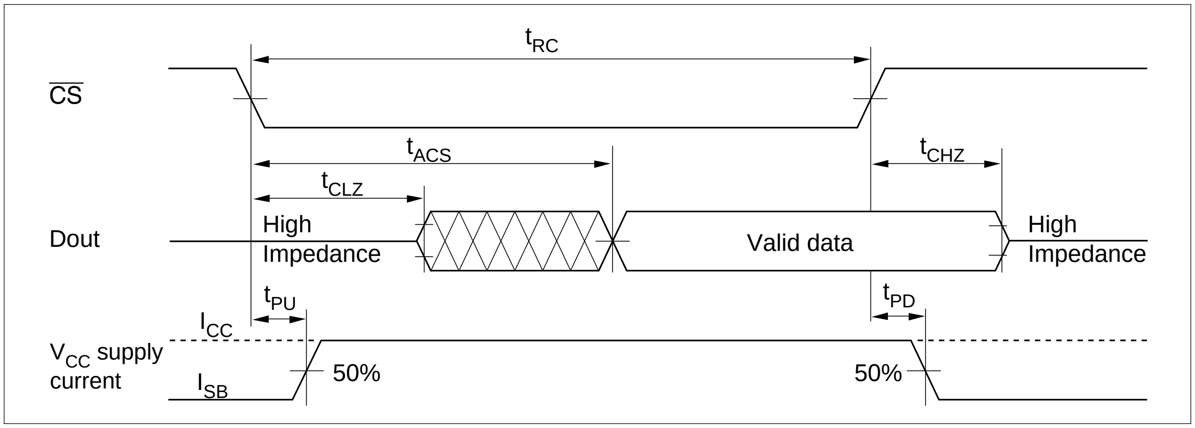
Read Timing Waveform (1) ($\overline{WE}$ = V_{IH})



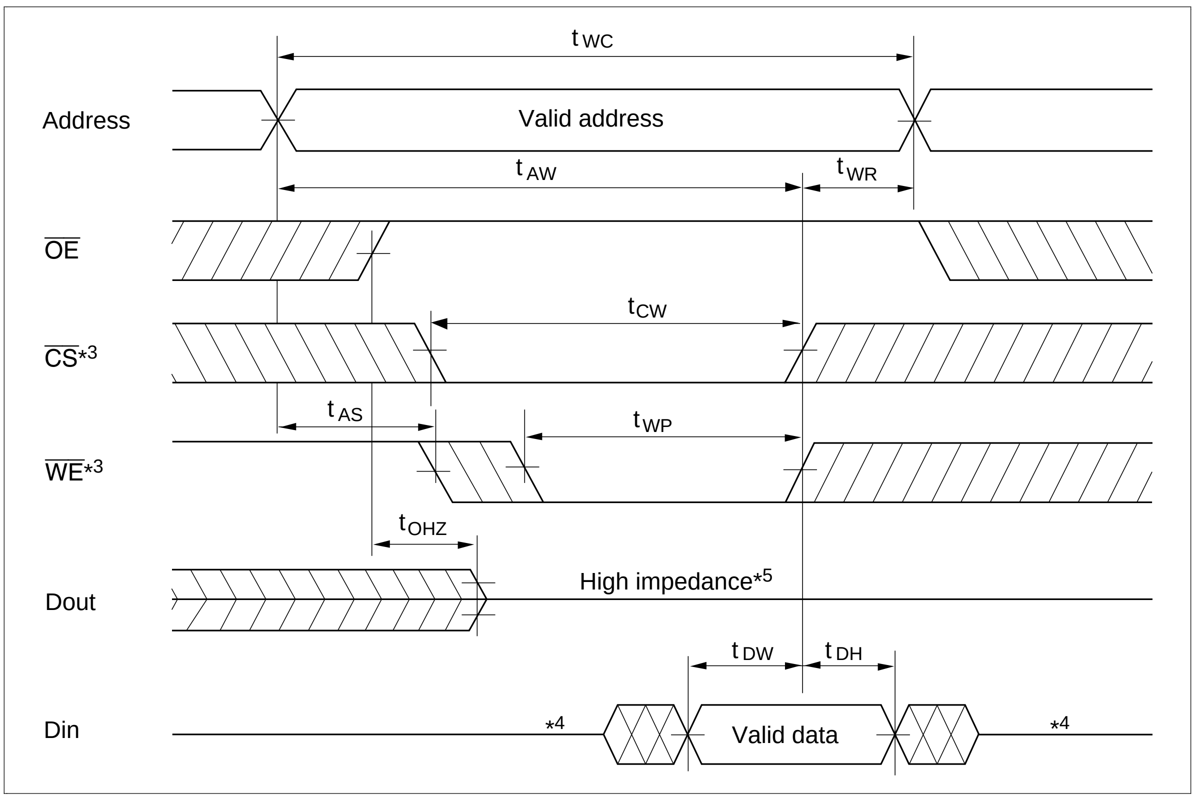
Read Timing Waveform (2) ($\overline{WE}$ = V_{IH}, $\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IL})



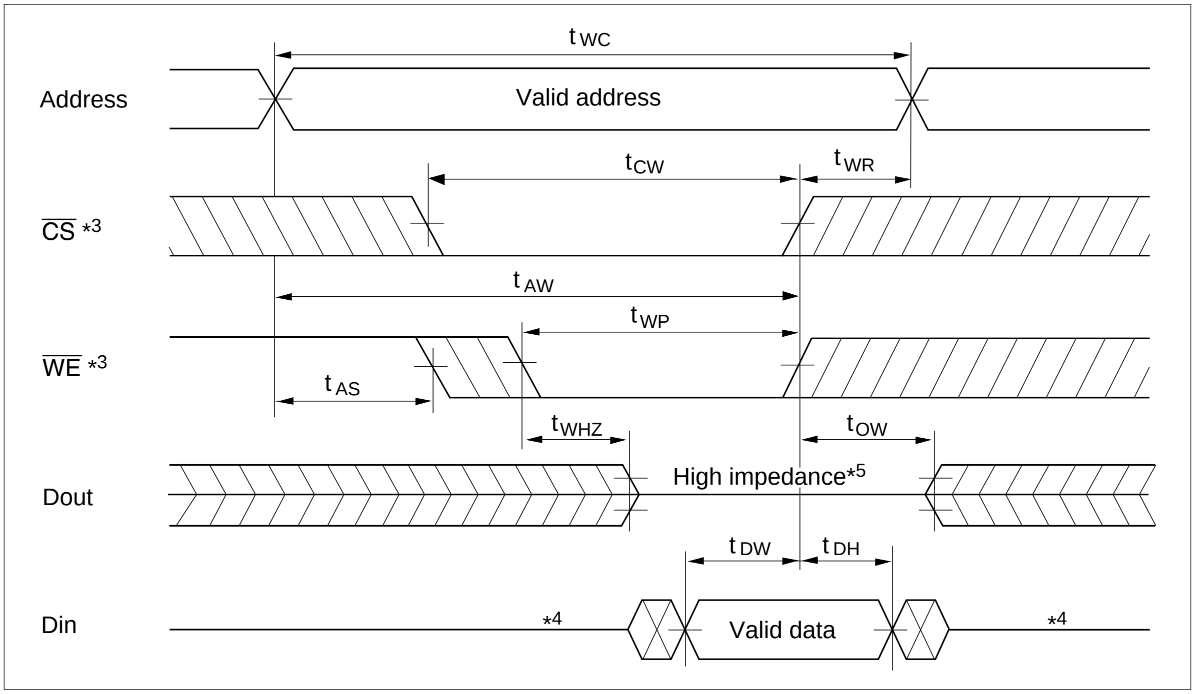
Read Timing Waveform (3) ($\overline{WE}$ = V_{IH}, $\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IL})*2



Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)

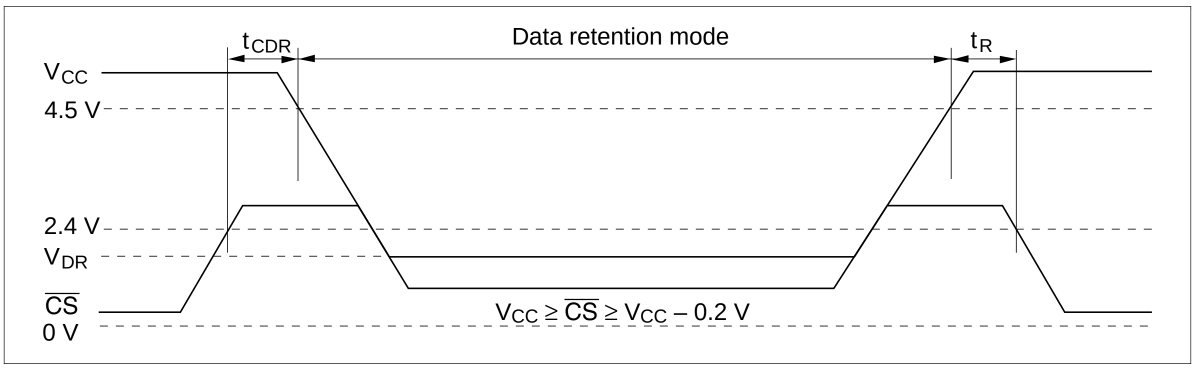


Low V_{CC} Data Retention Characteristics (Ta = – 40 to + 85°C)

Parameter	Symbol	Min	Typ*[1]	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2$ V (1) 0 V ≤ Vin ≤ 0.2 V or (2) $V_{CC} \geq$ Vin $\geq V_{CC} - 0.2$ V
Data retention current	I_{CCDR}	—	2	200	µA	V_{CC} = 3 V, $V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2$ V (1) 0 V ≤ Vin ≤ 0.2 V or (2) $V_{CC} \geq$ Vin $\geq V_{CC} - 0.2$ V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	50	—	—	ms	

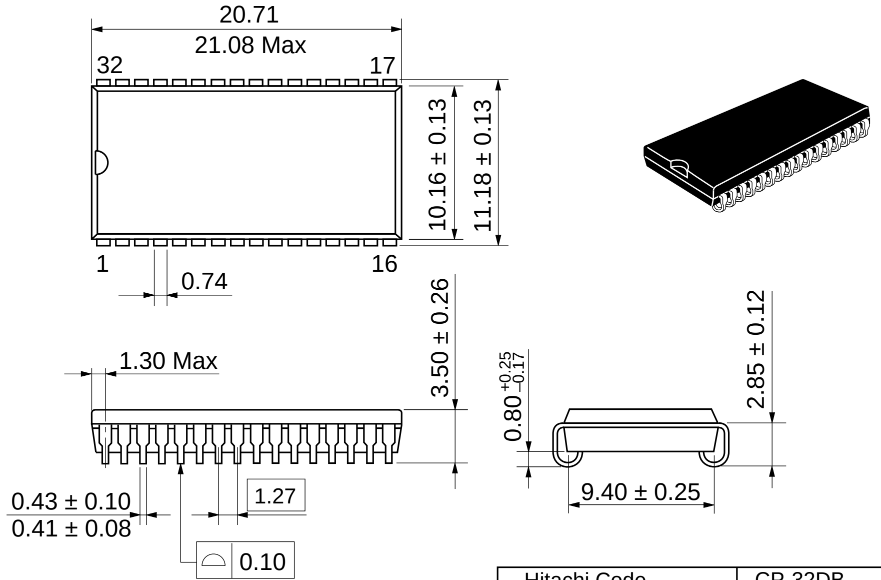
Note: 1. Typical values are at V_{CC} = 3.0 V, Ta = 25°C, and not guaranteed.

Low V_{CC} Data Retention Timing Waveform



Package Dimensions

HM628127HBLJPI Series (CP-32DB) Unit: mm



Hitachi Code	CP-32DB
JEDEC Code	MO-061-AB
EIAJ Code	SC-638
Weight	1.2 g

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Revision Record

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1.0	May. 19. 1997	Initial issue		