IXSE501

Incremental Shaft Encoder Peripheral Interface

FEATURES

- Direct (2-channel) quadrature inputs
- x4 quadrature detection for high resolution counting
- Low power LSI CMOS
- Easily interfaces to most microprocessors and microcomputers
- Non-intrusive counter latching
- 8-bit counter with automatic reset on read
- Highly noise immune differential line receiver Schmitt trigger inputs
- Optional version with RS-422 compatible inputs
- EXTERNAL EVENT detected and latched for positioning needs
- Quadrature pulse rate up to a frequency of CLOCK/2
- INDEX pulse decoding and sampling into a dedicated latch
- 20-pin slim DIP package (0.300 inch width)

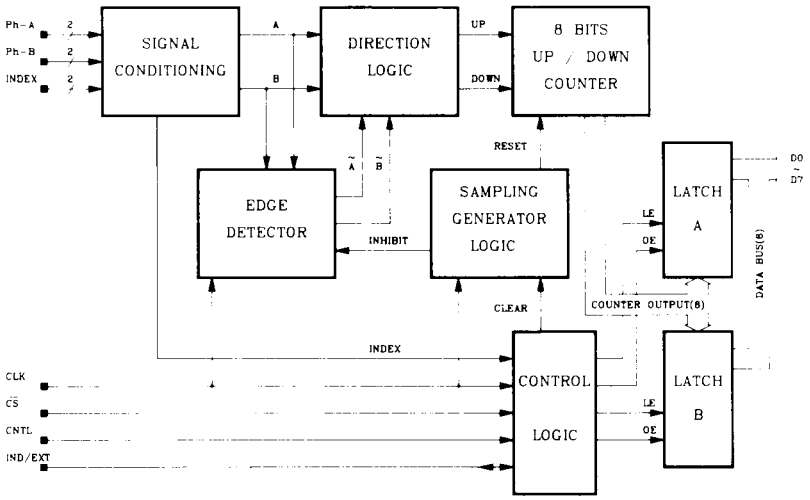
DESCRIPTION

The IXSE501 Shaft Encoder Peripheral Interface (SEPI) is a CMOS LSI device designed to interface a standard two-phase incremental encoder (either linear or rotary) with a microprocessor or microcomputer. The SEPI accepts two-phase incremental encoder signals directly, performs the quadrature detection, and counts the number of incremental encoder pulses in an internal 8-bit up/down counter. A separate hardware latch latches the exact count in the 8-bit up/down counter when either an INDEX pulse or an EXTERNAL EVENT pulse occurs, providing a means for very accurate absolute positioning.

The differential encoder inputs can be directly connected to two-phase incremental encoders with line driver type outputs. This line driver output to line receiver input combination provides very reliable signal conditioning and high noise immunity, especially in electrically noisy industrial environments. The hysteresis built into the encoder inputs aids both differential and single-ended signals. Because the IXSE501 encoder inputs are Schmitt triggered they can be directly connected to TTL, CMOS, and analog signals and still retain a high level of noise immunity.

Direction detection and up/down count accumulation result in a 2's complement number that is directly readable by the host microprocessor. The information provided by the IXSE501 aids in calculating the acceleration, velocity, and position of an incremental encoder; significantly reducing microprocessor overhead. Reduction of microprocessor overhead is particularly important in real-time MOTION CONTROL applications, such as servo motor velocity and position control systems.

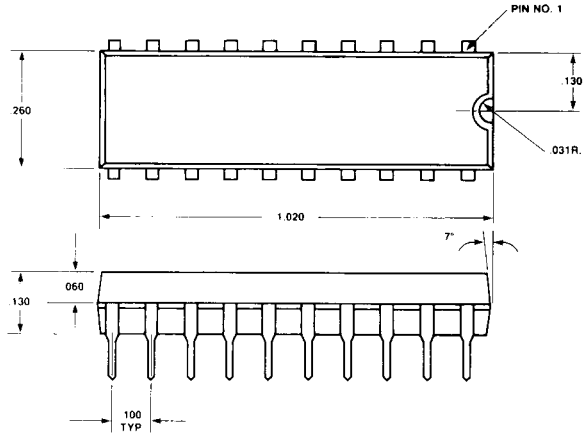
Figure 1. BLOCK DIAGRAM

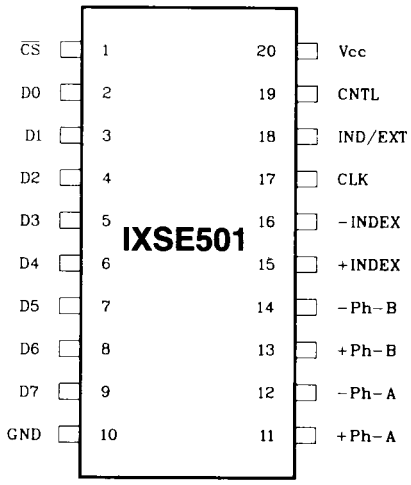


DEVICE FAMILY

	Features
IXSE501	Differential inputs with Schmitt trigger circuitry
IXSE501R	RS-422 compatible Differential inputs

PACKAGE OUTLINE AND PINOUTS





Physical Dimensions 20-Pin Plastic Dip

PART NUMBER DESCRIPTION

IXSE501 R P C

Optional Processing
Blank = Standard
B = Burn-In

Temperature Range
C = Commercial (0 to 70°C)
I = Industrial (−40 to +85°C)
M = Military (−55 to +125°C)

Package Type
P = 20-Pin Plastic Dip
D = 20-Pin Ceramic Dip
L = Leadless Chip Carrier

Optional Features
Blank = Standard
R = RS-422 Compatible Inputs

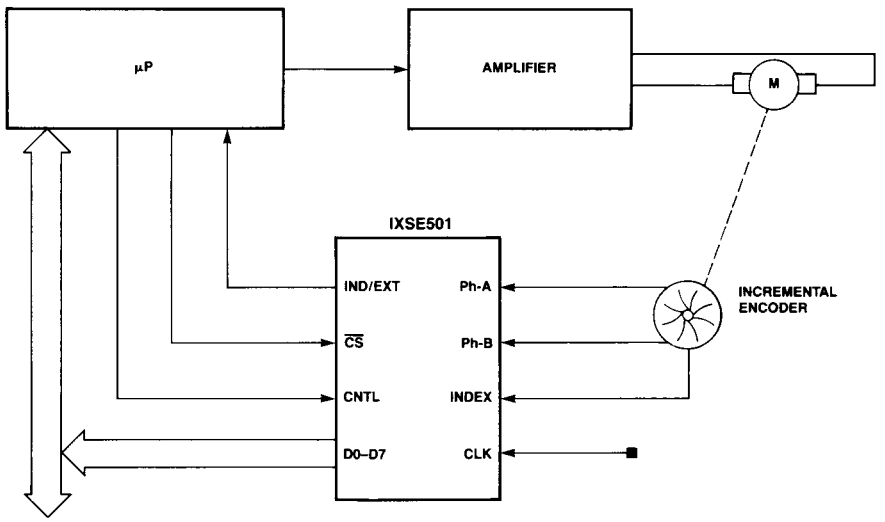
Device Type
8-Bit Counter Incremental SEPI

Note: Valid combinations are only those referenced in the IXYS price book or product selector guide. Consult the local IXYS sales office to confirm availability of specific combinations or new types.

PIN DESCRIPTIONS

SYMBOL	DESCRIPTION
V_{CC}	VOLTAGE SUPPLY—+5 Volts ±10%.
GND	CIRCUIT GROUND—0 Volts.
$\overline{CS}$	CHIP SELECT—a low on this input enables the data in the selected internal latch onto the external Data Bus, pins D0 through D7.
CNTL	CONTROL—(A-B select) a low on this input selects Latch A for reading. A high on this input selects Latch B for reading. For proper operation CNTL must be stable before $\overline{CS}$ goes low, for the duration of $\overline{CS}$ low, and after $\overline{CS}$ goes high. This input also determines how Latch B will be triggered. The Latch B Trigger has three states: triggered, armed for trigger on the IND/EXT input only, and armed for trigger by either the IND/EXT input or the INDEX input. Once Latch B has been triggered no additional trigger pulses will cause any latching to occur. Latch B must be read if it is to be triggered again. Reading Latch B (CNTL high and $\overline{CS}$ low) arms Latch B for trigger by the IND/EXT input only. If Latch B has not been triggered, a low-to-high transition on the CNTL input will arm Latch B for trigger on either the IND/EXT input or the INDEX input.
−Ph-A, +Ph-A, −Ph-B, +Ph-B	PHASE A and PHASE B—these differential line receiver inputs accept the quadrature signals from either a rotary or linear incremental encoder. They are compatible with standard RS-422 differential line drivers. These inputs can be used in a single-ended mode if the unused input is biased to approximately $V_{CC}/2$.
−INDEX, +INDEX	INDEX (sometimes called CHANNEL Z or MARKER PULSE)—these inputs have electrical characteristics identical to the Ph-A and Ph-B inputs. A low pulse on this input when Ph-A and Ph-B are also low will trigger Latch B, if Latch B is armed to trigger on the INDEX input.
CLK	CLOCK—external TTL clock.
D0 through D7	DATA BUS—these outputs provide access to the Latch A and Latch B data. The data is available as long as $\overline{CS}$ is low.
IND/EXT	INDEX/EXTERNAL EVENT—this pin is always active as both an input and an output. It should be sensed with a Schmitt trigger input and driven by an open-collector output. A high-to-low transition on this input when Latch B is armed causes the current count to be transferred to Latch B. The counter cannot be transferred again to Latch B until Latch B has been read. Reading Latch B arms it for trigger on the IND/EXT input. When the counter's contents are transferred to Latch B, this output generates a low pulse. If the INDEX input triggered Latch B, the pulse generated by this output will be as wide as the INDEX pulse. If an EXTERNAL EVENT triggered Latch B, the pulse generated by this output will be as wide as the EXTERNAL EVENT pulse.

Figure 2. BASIC SYSTEM CONFIGURATION



FUNCTIONAL DESCRIPTION

The IXSE501 is a Shaft Encoder Peripheral Interface (SEPI) designed with monolithic CMOS technology. A single +5 Volt supply and TTL level clock are required for operation. An internal 8-bit up/down counter continuously provides the number of quadrature edges (encoder counts) in a 2's complement binary format.

The SEPI has two separate 8-bit latches. Latch A contains the incremental encoder pulse count. Latch B stores the up/down count when an INDEX pulse occurs or an EXTERNAL EVENT pulse occurs. Both latches read the internal up/down counter which continuously counts the quadrature edges.

Outputs from either a rotary or linear incremental encoder are connected directly to the SEPI's differential line receiver inputs. The SEPI's incremental encoder inputs are designed to provide maximum noise immunity with minimum logic. No additional circuitry is required when connected to differential line drivers and only a few biasing resistors are required for single-ended operation.

The IND/EXT line can be used as both an input and an output. An open-drain configuration, IND/EXT is pulled up internally by a 25K resistor (approximately). This signal should be sensed with a hysteresis input and driven by an open-collector output. A low pulse on the IND/EXT line simultaneously latches data into Latch B and indicates that data has been transferred to Latch B.

The SEPI consists of primarily two sections, described below: the Signal Processing Logic and the Control and Output Buffer Logic.

Signal Processing Logic

The Signal Processing Logic is the center of the quadrature detection and up/down counting. It is the primary interface between the incremental encoder and the microprocessor. The Signal Processing Logic is represented by the Signal Conditioning, Direction Logic, Edge Detector, Sampling Generator Logic, and 8-bit up/down Counter blocks in Figure 1.

Control and Output Buffer Logic

The Control and Output Buffer Logic consists of the Control Logic, Latch A, and Latch B blocks in Figure 1. This logic is responsible for transferring data from the 8-bit up/down Counter to Latch A or Latch B and driving the contents of the latches onto the Data Bus. Data is transferred from the selected latch to the Data Bus when $\overline{CS}$ is low; CNTL determines which of the two latches is selected.

$\overline{CS}$ and CNTL also determine which input (INDEX or IND/EXT) will cause data to be transferred from the 8-bit up/down Counter to Latch B. Table 1 is a summary of the Latch B Trigger States. The Latch B Trigger can be in one of three states: armed for trigger by an IND/EXT pulse (the "FREE" state), armed for trigger by either an IND/EXT input or an INDEX pulse (the "SET" state), or triggered (the "LOCK" state). Thus, data can be written into Latch B in only two ways:

- a low pulse on the IND/EXT input when the Latch B Trigger is in either the "FREE" or "SET" state.
- or a low pulse on the INDEX input when the Latch B Trigger is in the "SET" state.

Once data has been transferred to Latch B, the Latch B Trigger goes to the "LOCK" state. In the "LOCK" state, the Latch B Trigger will ignore pulses on either the INDEX or IND/EXT input. Reading the contents of Latch B resets the Latch B Trigger to the "FREE" state. A low-to-high transition on the CNTL input when the Latch B Trigger is in the "FREE" state moves the Latch B Trigger to the "SET" state.

READING SEPI DATA

Reading Latch A:

1. Set CNTL low.
2. The falling edge of $\overline{CS}$ starts an internal cycle that transfers the up/down Counter data to Latch A and resets the Counter. The Counter starts counting from zero, uninterrupted and missing no encoder counts.

   Latch A data is available on the Data Bus as long as both $\overline{CS}$ and CNTL are low. The Access time is a function of $t_{CLK} + t_{CHDV}$ in asynchronous operation. The access time can be reduced if $\overline{CS}$ is synchronized with the clock.

Reading Latch B:

1. Set CNTL high.
2. When $\overline{CS}$ is low it will enable Latch B data onto the Data Bus. The contents of Latch B are not effected by reading Latch B. The Latch B Trigger is reset when the Latch B data is read.

Table 1. LATCH B TRIGGER STATES

CNTL	$\overline{CS}$	COUNTER	INDEX	EXTERNAL	OLD STATUS	LATCH A	LATCH B	NEW STATUS
H	L	Q_A	X	X	X	Q_{A-1}	ACTIVE	RESET(FREE)
X	H	Q_A	H	↓	FREE	Q_{A-1}	Q_A	LOCK
X	H	Q_A	↓	H	FREE	Q_{A-1}	Q_{A-1}	FREE
↑	H	Q_A	H	H	FREE	Q_{A-1}	Q_{A-1}	SET
X	H	Q_A	↓	H	SET	Q_{A-1}	Q_A	LOCK
X	H	Q_A	↓	H	LOCK	Q_{A-1}	Q_{A-1}	LOCK
X	H	Q_A	H	↓	LOCK	Q_{A-1}	Q_{A-1}	LOCK
L	L	Q_A	↓	H	SET	ACTIVE	Q_A	LOCK
L	H	Q_A	↓	H	SET	Q_{A-1}	Q_A	LOCK
L	L	Q_A	H	↓	FREE	ACTIVE	Q_A	LOCK
L	H	Q_A	H	↓	FREE	Q_{A-1}	Q_A	LOCK
L	↓	Q_A	H	H	X	Q_A	Q_{A-1}	X
L	↓	Q_A	↓	H	SET	Q_A	Q_A	LOCK
L	↓	Q_A	H	↓	FREE	Q_A	Q_A	LOCK

MAXIMUM RATINGS (Above Which Useful Life May Be Impaired)	
Supply Voltage	−0.3 to +7.0V
Common-Mode-Range [1]	−15.0 to +15.0V
Differential Input Voltage [1, 3]	−15.0 to +15.0V
Input Voltage [2]	−0.3 to +7.0V
Output Voltage	−0.3 to +7.0V
Maximum Power Dissipation	500mW
Storage Temperature Range	−55 to +125°C

OPERATING RANGE

		Commercial		
Parameters	**Description**	**Min**	**Max**	**Units**
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IC} [1]	Common-Mode-Range	−7.0	+7.0	V
V_{ID} [1, 3]	Differential Input Voltage	−7.0	+7.0	V
T_A	Operating Free Air Temperature	0	75	°C

DC CHARACTERISTICS (Over Operating Range)

Parameters	**Description**	**Applies to**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{TH}	Differential Threshold Voltage (Ph-A, Ph-B, Index)	IXSE501	$-7V \leq V_{IC} \leq +7V$	−0.4		0.4	V
		IXSE501R	$-7V \leq V_{IC} \leq +7V$	−0.2		0.2	V
R_I	Input Resistance	Ph-A, Ph-B, INDEX			4		KΩ
I_{IL}	Input Current Low	Ph-A, Ph-B, INDEX	$V_I = -7V$	−2.4			mA
I_{IH}	Input Current High	Ph-A, Ph-B, INDEX	$V_I = +7V$			2.4	mA
V_H	Input Hysteresis	Ph-A, Ph-B, INDEX	V_{CC} = 5V, V_{IC} = 0V		140		mV
V_{IH}	Input High Voltage	CLK, $\overline{CS}$, CNTL, IND/EXT		2.0		V_{CC} +0.3	V
V_{IL}	Input Low Voltage	CLK, $\overline{CS}$, CNTL, IND/EXT		−0.3		0.8	V
V_{OH}	Output High Voltage	D0 − D7	$I_{OH} = -2mA$	2.4			V
V_{OL}	Output Low Voltage	D0 − D7	$I_{OL} = 4mA$			0.4	V
I_{LI}	Input Leakage Current	CLK, $\overline{CS}$, CNTL	$0 \leq V_I \leq V_{CC}$	−10		10	μA
I_{LO}	Output Leakage Current	D0 − D7	$0 \leq V_O \leq V_{CC}$	−10		10	μA
V_{OL}	IND/EXT Low Output Voltage	IND/EXT	$I_{OL} = 4mA$			0.4	V
I_{PU}	IND/EXT Pull-Up Current	IND/EXT	$V_O = 0V$	200			μA
I_{CC}	Power Supply Current		f_{CLK} = 4 MHz; V_{IL} = 0, $V_{IH} = V_{CC}$			10	mA

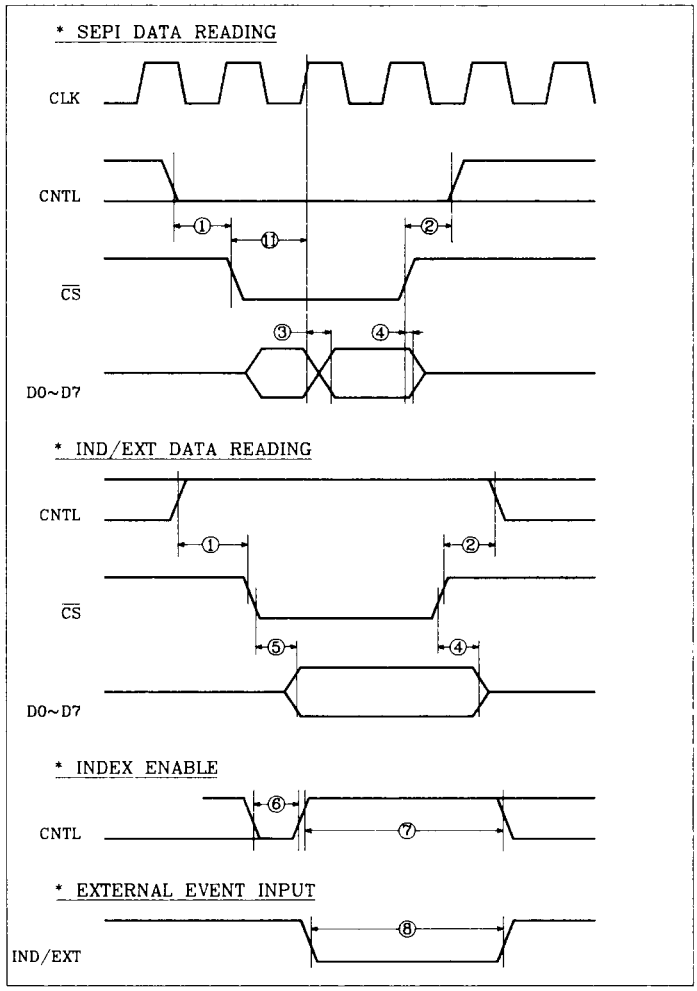
Notes: 1. These values apply to Ph-A, Ph-B, INDEX inputs.
2. These values apply to $\overline{CS}$, CNTL, IND/EXT, CLK inputs.
3. Differential voltages are measured at the noninverting input with respect to the inverting input.

AC CHARACTERISTICS (Over Operating Range Unless Otherwise Specified)

No	Parameter	Description	Min	Typ	Max	Unit
1	t_{CNVCSL}	CNTL to $\overline{CS}$ Low, Setup Time	10			ns
2	t_{CSHCNX}	CNTL after $\overline{CS}$ High, Hold Time	10			ns
3	t_{CHDV}	Latch A Data Valid after CLK High[1]		35	150	ns
4	t_{CSHDX}	Data Valid after $\overline{CS}$ High	0			ns
5	t_{CSLDV}	Latch B Data Valid after $\overline{CS}$ Low[1]		20	150	ns
6	t_{CNVCNH}	CNTL Low to INDEX Enable, Setup Time	100			ns
7	t_{CNHCNX}	CNTL High after INDEX Enable, Hold Time	100			ns
8	t_{ELEX}	EXT Low after EXTERNAL EVENT, Hold Time	100			ns
9	f_{CLK}	CLK (Clock) Frequency		4	12	MHz
10	f_A, f_B	Ph-A and Ph-B Frequency[2]		.5	1	MHz
11	t_{CSLCH}	$\overline{CS}$ Low to CLK High, Setup Time	10			ns

Notes: 1. Test condition is with a 100pf load.
2. Test condition is f_A, f_B less than or equal to $f_{CLK}/8$.

WAVEFORMS



CIRCUIT CONFIGURATIONS

The IXSE501 can be interfaced with nearly all available microprocessors. In some applications, the IXSE501 can be used with no added interface. Other applications may require WAIT STATE circuitry to overcome speed limitations.

INTERFACING TO THE INTEL 8051

As shown in Figure 3, the IXSE501 can be used with an 8051. D0–D7 is Port 0 and A8–A15 is Port 2. If A8–A15 are not used for addressing external memory, the system can be designed without the use of a 74HC138. In both cases, reading the IXSE501 is performed by using the move external RAM instruction (MOVX A, @ DPTR).

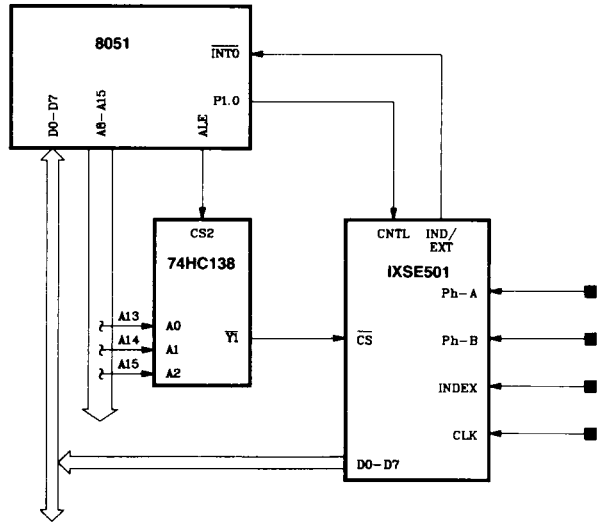


Figure 3. IXSE501 with 8051

INTERFACING TO THE MOTOROLA MC68000

An interface configuration with the 68000 microprocessor is shown in Figure 4. Unlike the 8051 interface shown, the SEPI's clock and the microprocessor's clock are synchronized in this circuit. The SEPI is accessed by reading and writing to any even address that has address bits A23 and A22 set to ones and A21 set to a zero.

The SEPI's CNTL input is cleared by writing a zero to the least significant bit at the SEPI's even address. The CNTL input is set by writing a one to the least significant bit at the SEPI's even address. To read the contents of a latch simply set the CNTL input to the appropriate state and read the byte at the SEPI's even address.

This circuit will work for a 68008 if $\overline{LDS}$ is replaced with $\overline{DS}$.

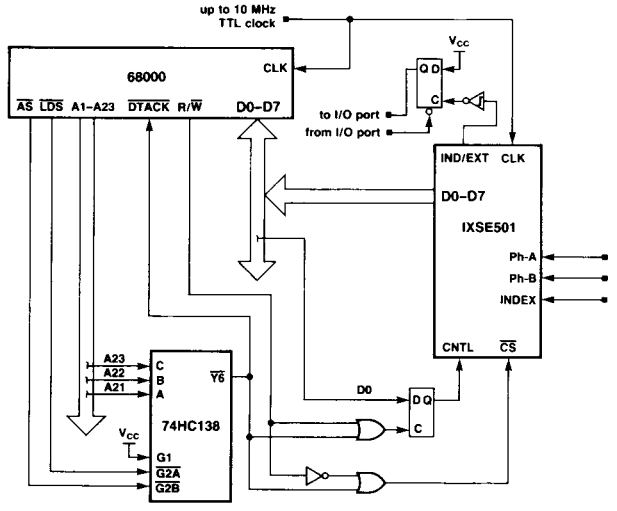


Figure 4. IXSE501 with MC68000

APPLICATION INFORMATION

INTRODUCTION

The IXSE501 is an *INCREMENTAL* peripheral interface between a shaft encoder and a microprocessor. As such it is designed to simplify this interface and reduce processor overhead. It is not an absolute position monitor. The register size needed for position monitoring varies widely from system to system, and can be easily implemented in the microprocessor by adding the 8-bit relative position information into a wider (16-, 24- or 32-bit) internal register.

One of the problems associated with a shaft encoder interface is ensuring count integrity; in other words, eliminating the possibility of missing input pulses, particularly during a read operation. An incremental interface, such as the IXSE501, with an automatic counter reset upon read and some additional internal logic, solves this problem and guarantees count integrity.

Operation with an 8-bit counter in the incremental mode, with automatic reset of counter on read, results in the lowest microprocessor overhead:

- Only one byte read operation required.
- No separate port or operation required for counter reset.
- By reading the SEPI at a constant rate (via a real time clock), every read directly represents velocity (# of pulses per update period), without the need for further manipulation.
- Absolute position is monitored in the microprocessor by a simple and fast add instruction of the 8-bit data into a wider (2, 3, or 4 byte) internal position register.
- Since data is presented in 2's complement format, the addition is a simple operation and by definition takes care of direction reversals.

Figure 5 demonstrates the velocity performance achievable with an 8-bit counter. This diagram reflects the need to read the counter before it overflows (127 pulses). It is clear from this diagram that only with very high resolution shaft encoders is the achievable motor speed somewhat limited. In most applications, using medium resolution shaft encoders, and typical update rates, motor speeds of several thousand rpm are achievable. For example: using a 500 line/rev shaft encoder, with a system update rate of 2 kHz, provides a resolution of 2000 counts per revolution and a maximum motor velocity of 7620 rpm.

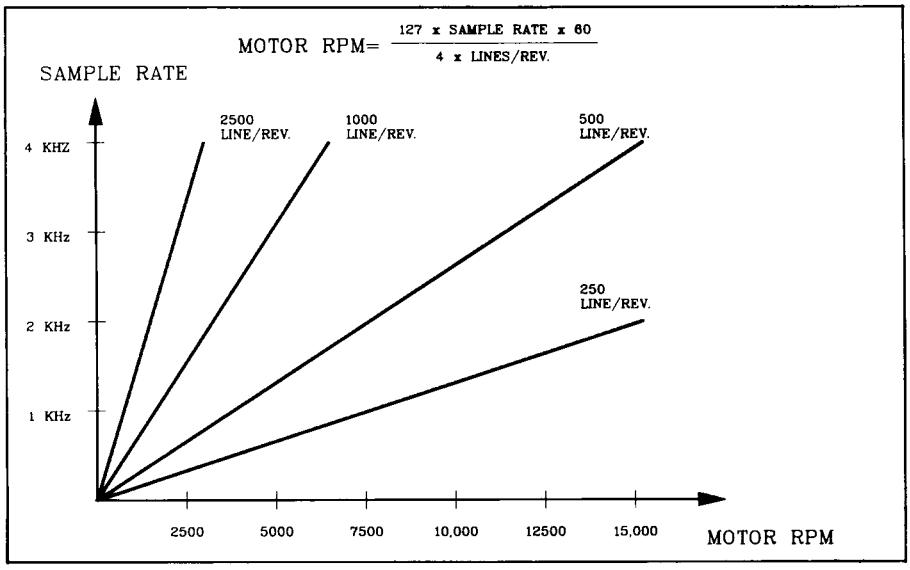


Figure 5. Maximum Motor rpm as a Function of Sample Rate

DIRECT INTERFACE WITH A SHAFT ENCODER

One of the unique features of the IXSE501 is its differential line receiver input structure. Most shaft encoder manufacturers provide several optional output configurations: Differential line drivers, TTL level, CMOS level, or open collector outputs. The IXSE501 is designed to directly interface with all these configurations.

For optimal noise immunity it is recommended that one use the differential line driver/receiver interface method (particularly if long cable lengths are required). See Figure 6. In the case of a single-ended interface one should use pull-up resistors (selected according to the shaft encoder used). Figure 7 shows the resistor values selected to interface with HP encoders. R1 and R2 provide a 2V reference to the (-) inputs, for optimal noise margin.

USE OF THE INDEX PULSE

In the incremental mode a direct interrupt on the INDEX pulse is not sufficient. There is no accurate method of determining the exact position of the INDEX pulse. The IXSE501 provides a dedicated latch (Latch B) to record the INDEX occurrence and handle interrupt generation.

For error detection a 16-bit dedicated register in the microprocessor should monitor pulses per revolution. Accumulate SEPI readings between 2 consecutive INDEX pulses and compare this number to the encoder resolution (4x line/rev).

CONSIDERATIONS FOR SELECTION OF CLOCK FREQUENCY

A. Available clock in the system.

B. In asynchronous operation a higher frequency clock provides faster access time to Latch A (max. access time = clock period + t_{CHDV}).

C. Noise immunity is a function of clock period; lower frequency clock provides better noise blockage.

D. Maximum encoder channel input frequency should be 1 MHz or less, and clock frequency should be at least 8 times the input frequency. (For 500 line/rev encoder and maximum velocity of 6000 rpm, max input frequency is 50 kHz and the clock should be a minimum of 400 kHz.)

E. To guarantee accurate position counting, with an encoder quadrature tolerance of ±45°, the clock frequency should be twice as much as calculated in D (16 times the input frequency).

F. It has been determined that a typical clock frequency of 4 MHz guarantees count integrity for most applications and provides an asynchronous max access time of 400 ns. 4 MHz is easily generated from most system clocks.

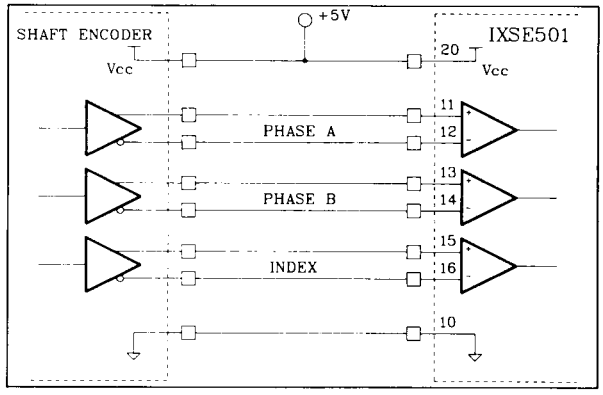


Figure 6. Differential Line Driver Shaft Encoder Interface

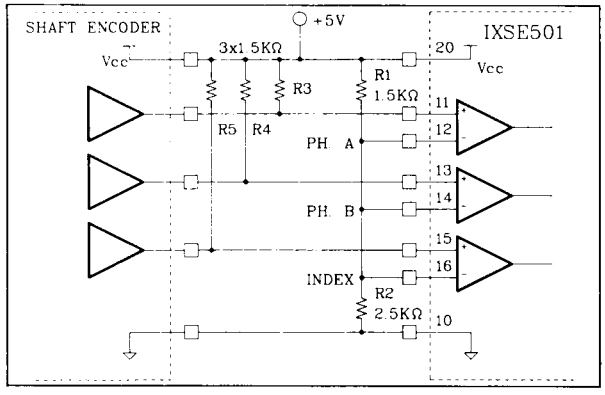


Figure 7. Single Ended Shaft Encoder Interface

IXYS DOMESTIC SALES REPRESENTATIVES

ALABAMA
The Novus Group, Inc.
Huntsville, AL
205-881-2207

ALASKA
Components West
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ARIZONA
Western High Tech Marketing
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513-433-6776

Dolfuss-Root & Co.
Strongsville, OH
216-238-0300

OKLAHOMA
Barry Sales, Inc.
Tulsa, OK
918-749-7775

OREGON
Components West, Inc.
Tigard, OR
503-684-1671

PENNSYLVANIA (EAST)
Knowles Associates
Feasterville, PA
215-322-7100

PENNSYLVANIA (WEST)
Dolfuss-Root & Co.
Bridgeville, PA
412-221-4420

RHODE ISLAND
Datcom, Inc.
Waltham, MA
617-891-4600

SOUTH CAROLINA
The Novus Group, Inc.
Raleigh, NC
919-872-3966

SOUTH DAKOTA
Robert W. Marshall Co., Inc.
Minneapolis, MN
612-929-0457

TENNESSEE (EAST)
The Novus Group, Inc.
Lilburn, GA
404-381-1015

TENNESSEE (WEST)
The Novus Group, Inc.
Huntsville, AL
205-881-2207

TEXAS
Barry Sales, Inc.
Austin, TX
512-837-3616

Barry Sales, Inc.
Houston, TX
713-784-5860

Barry Sales, Inc.
Richardson, TX
214-234-0255

UTAH
Moss Marketing
Salt Lake City, UT
801-363-5875

VERMONT
Datcom, Inc.
Waltham, MA
617-891-4600

VIRGINIA
Arbotek
Lynchburg, VA
804-385-6907

WASHINGTON
Components West, Inc.
Redmond, WA
206-885-5880

Components West, Inc.
Liberty Lake, WA
509-922-2412

W. VIRGINIA
Dolfuss-Root & Co.
Dayton, OH
513-433-6776

WISCONSIN
LTD Technologies
Milwaukee, WI
414-774-1000

Robert W. Marshall Co., Inc.
Minneapolis, MN
612-929-0457

WYOMING
Moss Marketing
Denver, CO
303-455-7205

*Contact IXYS Corporation
142 Charcot Avenue
San Jose, CA 95131
408-435-1900

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Berkshire
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JAPAN
SMI Systems Mktg.
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1 46 64 11 01

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E.L. Cap Electronics Ltd.
Hong Kong
0-6578883

ISRAEL
RDT Electronics Eng'g Ltd.
Tel Aviv
972 3 483211 9

ITALY
Cefra S.p.a.
Milan
2 23 60 154

Cefra S.p.a.
Roma
06 84 50 117

SWEDEN
Svensk Teleindustri
Spanga
08 761 7300

IXYS CORPORATION

142 Charcot Avenue • San Jose, California 95131

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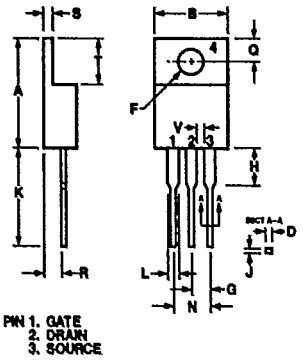
DETAILED PACKAGE OUTLINES

T-91-20

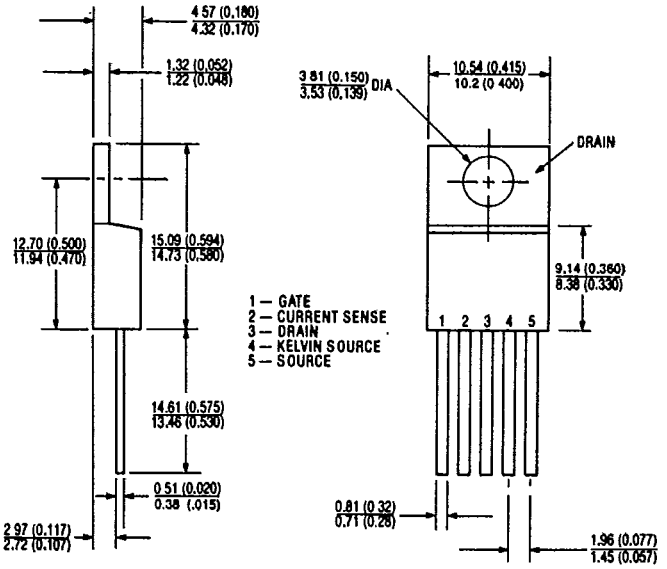
TO-220 AB



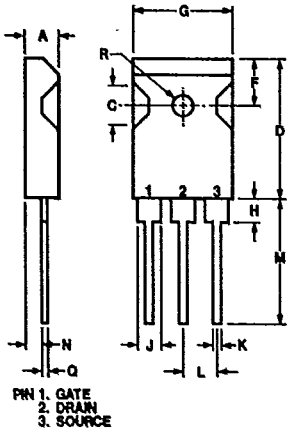
Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	14.23	16.51	.560	.650
B	9.66	10.66	.380	.420
C	3.56	4.82	.140	.190
D	0.64	0.89	.025	.035
F	3.54	4.08	.139	.161
G	2.29	2.79	.090	.110
H	–	6.35	–	250
J	0.51	.76	.020	030
K	12.70	14.73	.500	.580
L	1.15	1.77	045	.070
N	4.83	5.33	.190	.210
Q	2.54	3.42	.100	135
R	2.04	2.49	080	115
S	0.64	1.39	025	.055
T	5.85	6.85	2.30	2.70
V	1.15	–	.045	–

CONFORMS TO OUTLINE TO-220 (IR H-7)

Dimensions in Millimeters (Inches)

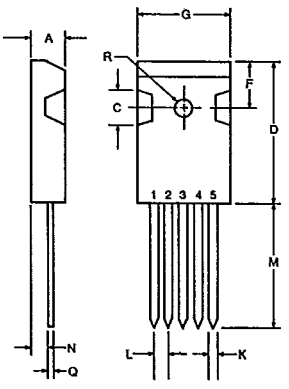


TO-247 (3 LEADED)



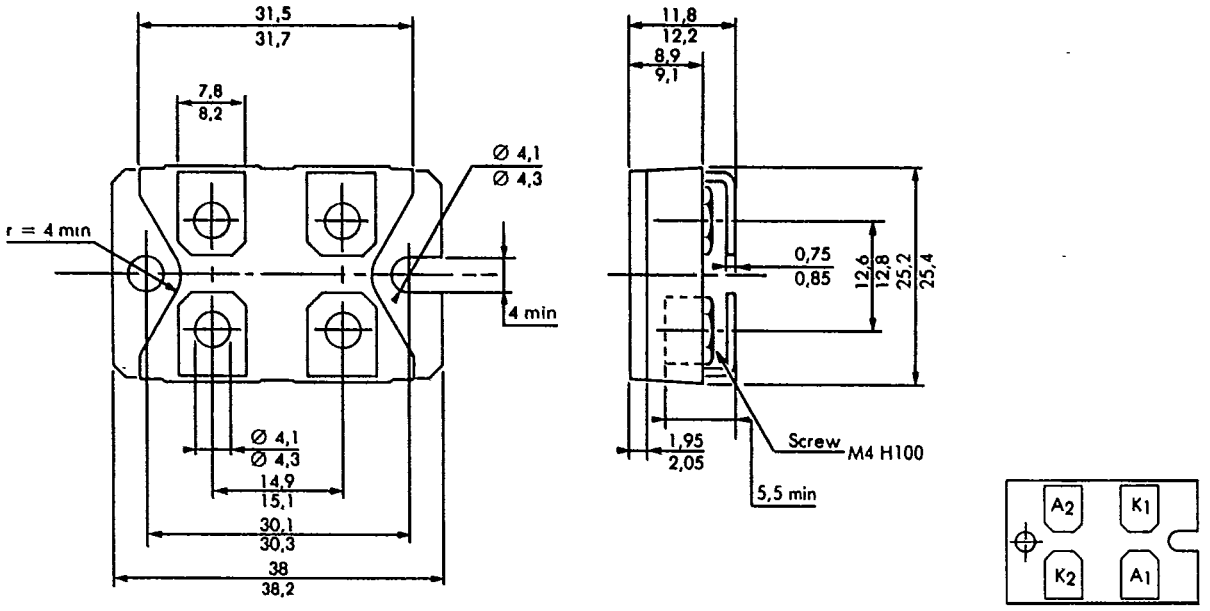
Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.7	5.3	.185	.209
C	4.5	6.0	.178	.236
D	19.7	21.4	.776	.843
F	5.3	6.1	.209	.240
G	15.3	15.9	.602	.625
H	3.7	4.3	.146	.169
J	1.95	2.4	.077	.094
J_1	2.97	3.4	.117	.134
K	1.0	1.4	.040	.055
L	5.4	5.5	.213	.217
M	19.9	20.2	.783	.795
N	2.2	2.6	.087	.102
Q	0.4	0.8	.016	.031
R	2.9	3.3	.114	.129

TO-247 (5 LEADED)

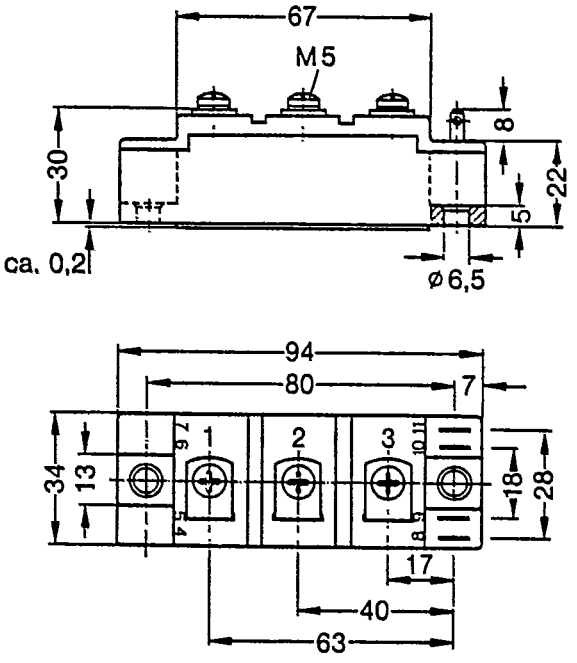


Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.7	5.3	.185	.209
C	4.5	6.0	.178	.236
D	19.7	21.4	.776	.843
F	5.3	6.1	.209	.240
G	15.3	15.9	.602	.625
K	1.1	1.3	.043	.051
L	2.51	2.56	.099	.101
M	19.9	20.2	.783	.795
N	2.2	2.6	.087	.102
Q	0.4	0.8	.016	.031
R	2.9	3.3	.114	.129

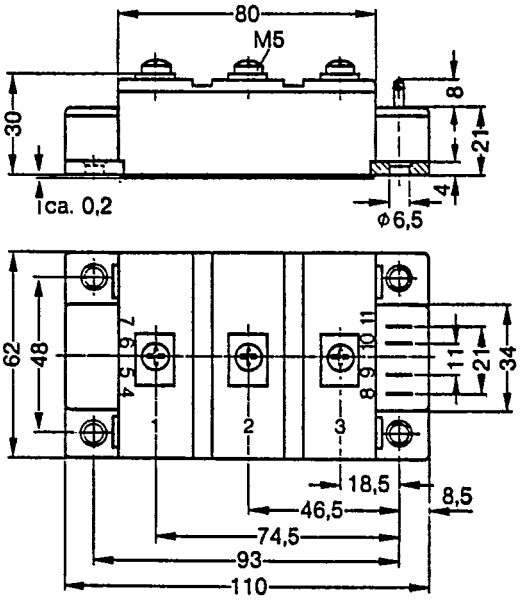
TO-238
Dimensions in Millimeters



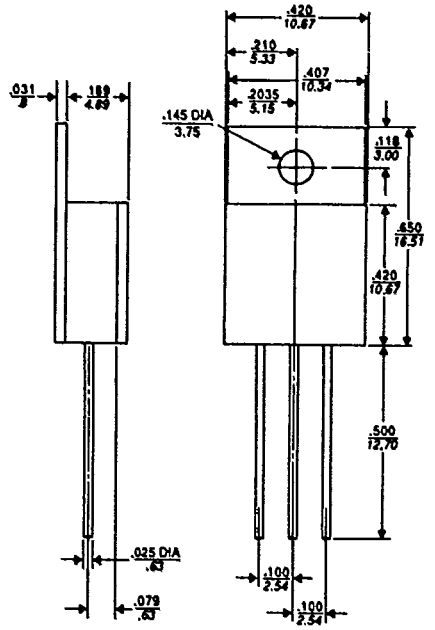
Y-4
Dimensions in Millimeters



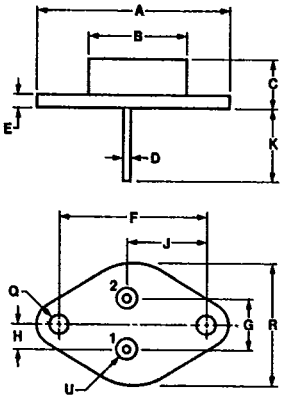
Y-3
Dimensions in Millimeters



TO-220 HERMETIC



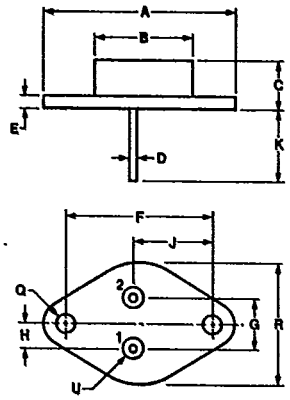
TO-204 AE



PIN 1. GATE
2. SOURCE
CASE–DRAIN

Dim.	Millimeter Min.	Millimeter Max.	Inches Min.	Inches Max.
A	–	39.37	–	1.55
B	–	19.71	–	.776
C	7.62	10.16	.300	.400
D	1.47	1.57	.058	.062
E	1.52	3.43	.060	.135
F	30.15	BSC	1.187	BSC
G	10.67	11.18	.420	.440
H	5.33	6.10	.210	.240
J	16.68	17.12	.657	.674
K	11.20	11.98	.441	.472
Q	3.86	4.11	.152	.162
R	24.84	25 27	.978	.995

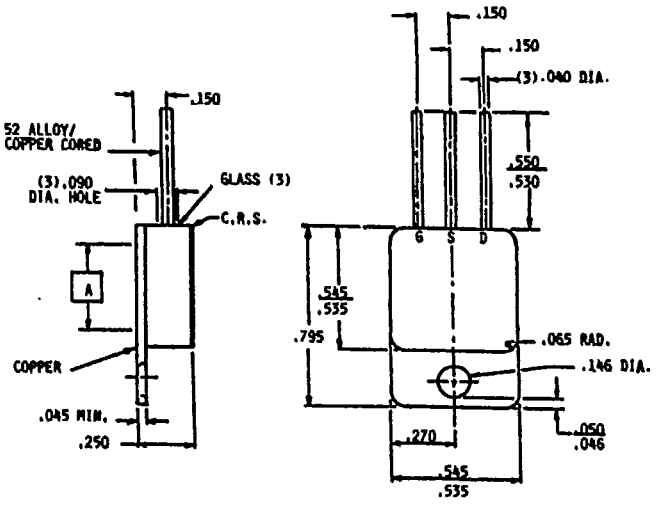
TO-204 AA



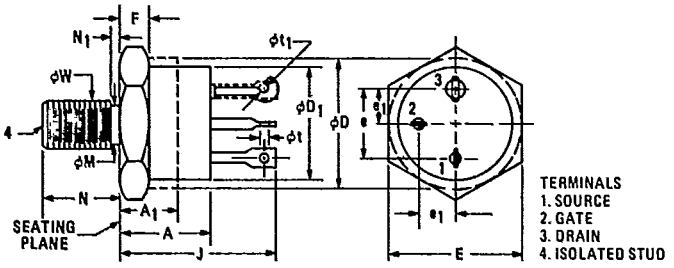
PIN 1. GATE
2. SOURCE
CASE–DRAIN

Dim.	Millimeter Min.	Millimeter Max.	Inches Min.	Inches Max.
A	–	39.37	–	.155
B	–	19.71	–	.776
C	6.35	8.89	.250	.350
D	.097	1.09.	.038	.043
E	–	3.43	–	.135
F	30.15	BSC	1.187	BSC
G	10.67	11.18	.420	.440
H	5.33	6.10	.210	.240
J	16.68	17.12	.657	.674
K	11.20	11.98	.441	.472
Q	3.86	4.11	.152	.162
R	24.84	25.47	.978	1.00

TO-254 HERMETIC



CONFORMS TO JEDEC OUTLINE TO-210AC (TO-61)
Dimensions in Millimeters (Inches)

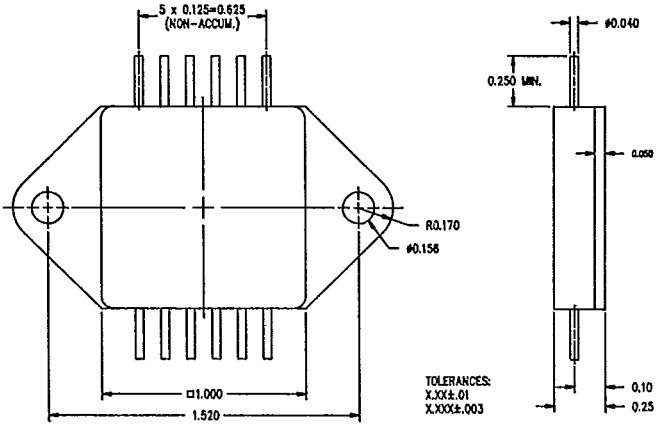


Symbol	Inches Min.	Inches Max.	Millimeters Min.	Millimeters Max.	Notes
A	0.325	0.460	8.26	11.68	
A_1		0.270		6.86	2
øD	0.610	0.687	15.49	17.45	2
$øD_1$	0.570	0.610	14.48	15.49	
E	0.667	0.687	16.94	17.45	
e	0.340	0.415	8.64	10.54	5
e_1	0.170	0.213	4.32	5.41	5
F	0.090	0.150	2.29	3.81	1

Symbol	Inches Min.	Inches Max.	Millimeters Min.	Millimeters Max.	Notes
J	0.640	0.875	16.26	22.23	
øM	0.220	0.249	5.59	6.32	
N	0.422	0.455	10.72	11.56	
N_1		0.090		2.29	
øt	0.055	0.072	1.19	1.83	
$øt_1$	0.046	0.077	1.17	1.96	4
øW	0.2225	0.2268	5.561	5.761	3

NOTES
1. DIMENSION DOES NOT INCLUDE SEALING FLANGES.
2. PACKAGE CONTOUR OPTIONAL WITHIN DIMENSIONS SPECIFIED.
3. PITCH DIAMETER – THREAD 1/4 28 UNF 2A (COATED).
   REFERENCE ISCREW THREAD STANDARDS FOR FEDERAL SERVICES - HANDBOOK H 28).
4. THIS TERMINAL CAN BE FLATTENED AND PIERCED OR HOOK TYPE.
5. POSITION OF LEADS IN RELATION TO THE HEXAGON IS NOT CONTROLLED.

QUADPAC



Z-Pac