

Features

- High speed access times
Com'l: 10, 12, 15, 17, 20 and 25 ns
Ind'l: 15, 17, 20, and 25 ns
- Low power operation
 - PDM41028SA
Active: 400 mW (typ.)
Standby: 150 mW (typ.)
 - PDM41028LA
Active: 350 mW (typ.)
Standby: 100 mW (typ.)
- Single +5V ($\pm 10\%$) power supply
- TTL compatible inputs and outputs
- Packages
 - Plastic DIP (400 mil) - P
 - Plastic SOJ (300 mil) - TSO
 - Plastic SOJ (400 mil) - SO
 - Plastic TSOP - T

Description

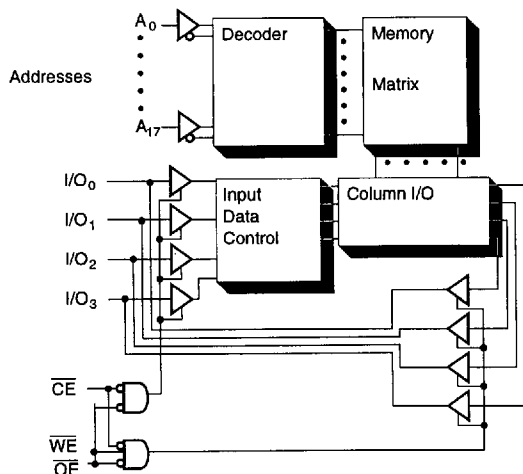
The PDM41028 is a high-performance CMOS static RAM organized as 262,144 x4 bits. This product is produced in Paradigm's proprietary CMOS technology which offers the designer the highest speed parts. Writing to this device is accomplished when the write enable (WE) and the chip enable (CE) inputs are both LOW. Reading is accomplished when WE remains HIGH and CE and OE are both LOW.

The PDM41028 operates from a single +5V power supply and all the inputs and outputs are fully TTL compatible. The PDM41028 comes in two versions, the standard power version PDM41028SA and a low power version the PDM41028LA. The two versions are functionally the same and only differ in their power consumption.

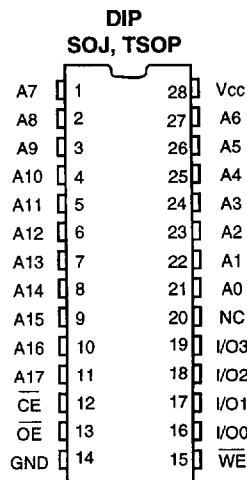
The PDM41028 is available in a 28-pin 400 mil Plastic DIP, 28-pin 300 mil SOJ, 28-pin TSOP, and a 28-pin 400 mil SOJ for surface mount applications.

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Functional Block Diagram



Pin Configuration



Truth Table⁽¹⁾

OE	WE	CE	I/O	MODE
X	X	H	Hi-Z	Standby
L	H	L	D _{OUT}	Read
X	L	L	D _{IN}	Write
H	H	L	Hi-Z	Output Disable

NOTE: 1. H = V_{IH} , L = V_{IL} , X = DON'T CARE

Absolute Maximum Ratings ⁽¹⁾

Symbol	Rating	Com'l.	Ind.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
Industrial	Ambient Temperature	-40	25	85	°C
Commercial	Ambient Temperature	0	25	70	°C

DC Electrical Characteristics ($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	Test Conditions		PDM41028SA		PDM41028LA		Unit
				Min.	Max.	Min.	Max.	
I_{LI}	Input Leakage Current	$V_{CC} = \text{MAX.}, V_{IN} = \text{GND to } V_{CC}$	Com'l/ Ind.	-5	5	-2	5	μA
I_{LO}	Output Leakage Current	$V_{CC} = \text{MAX.},$ $CE = V_{IH}, V_{OUT} = \text{GND to } V_{CC}$	Com'l/ Ind.	-5	5	-2	5	μA
V_{IH}	Input High Voltage			2.2	6.0	2.2	6.0	V
V_{IL}	Input Low Voltage			-0.5 ⁽¹⁾	0.8	-0.5 ⁽¹⁾	0.8	V
V_{OL}	Output Low Voltage	$I_{OL} = 8 \text{ mA}, V_{CC} = \text{Min.}$ $I_{OL} = 10 \text{ mA}, V_{CC} = \text{Min.}$		—	0.4 0.5	—	0.4 0.5	V V
V_{OH}	Output High Voltage	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min.}$		2.4	—	2.4	—	V

NOTE: 1. $V_{IL}(\text{min}) = -3.0V$ for pulse width less than 20 ns

Power Supply Characteristics

Symbol	Parameter	Power	-10	-12	-15		-17		-20		-25		Unit
			Com'l.	Com'l.	Com'l.	Ind.	Com'l.	Ind.	Com'l.	Ind.	Com'l.	Ind.	
I_{CC}	Operating Current $CE = V_{IL}$, and $CE2 = V_{IH}$	SA	250	230	185	195	165	175	155	165	145	155	mA
	$f = f_{\text{MAX}} = 1/f_{RC}$ $V_{CC} = \text{Max.}$ $I_{OUT} = 0 \text{ mA}$	LA	230	210	165	175	155	165	140	150	135	145	mA
I_{SB}	Standby Current $CE1 = V_{IH}$ or $CE2 = V_{IL}$	SA	80	70	55	55	50	50	45	45	40	40	mA
	$f = f_{\text{MAX}} = 1/f_{RC}$ $V_{CC} = \text{Max.}$	LA	75	65	50	50	45	45	40	40	35	35	mA
I_{SB1}	Full Standby Current $CE1 \geq V_{HC}$ or $CE2 \leq V_{LC}$	SA	20	20	10	15	10	15	10	15	10	15	mA
	$f = 0$ $V_{CC} = \text{Max.},$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	LA	10	10	5	10	5	10	5	10	5	10	mA

SHADED AREA = PRELIMINARY DATA

NOTES: All values are maximum guaranteed values.

$V_{LC} \leq 0.2V, V_{HC} \geq V_{CC} - 0.2V$

Capacitance⁽¹⁾ ($T_A = +25^\circ\text{C}, f = 1.0 \text{ MHz}$)

Symbol	Parameter	Max.	Unit
C_{IN}	Input Capacitance	8	pF
C_{OUT}	Output Capacitance	8	pF

NOTE:1. This parameter is determined by device characterization but is not production tested.

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AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input rise and fall times	5 ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

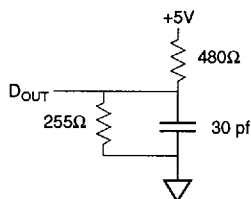


Figure 1. Output Load Equivalent

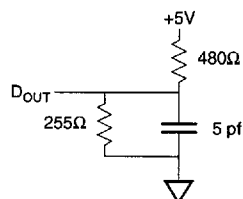


Figure 2. Output Load Equivalent
(for t_{LZCE} , t_{HZCE} , t_{LZWE} , t_{HZWE} , t_{LZOE} , t_{HZOE})

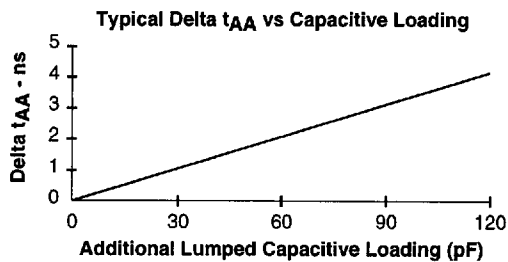
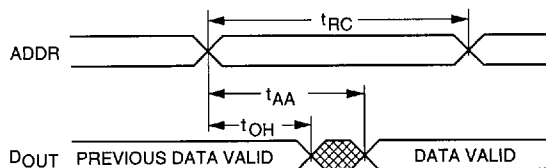
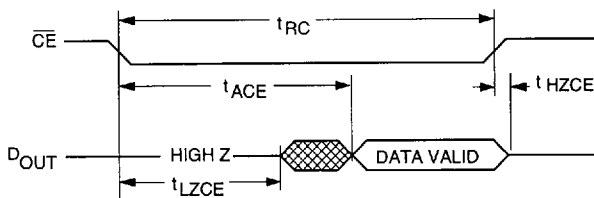


Figure 4.

Read Cycle No. 1^(4, 5)



Read Cycle No. 2^(2, 4, 6)



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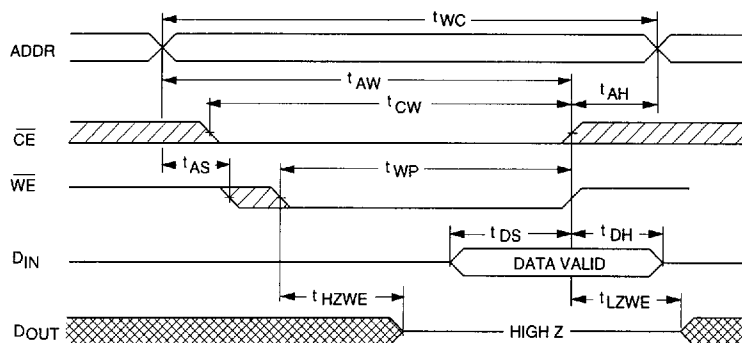
AC Electrical Characteristics (V_{CC} = 5V ± 10%, All Temperature Ranges)

Description		-10 ⁽⁷⁾		-12 ⁽⁷⁾		-15		-17		-20		-25		Units
READ Cycle	Sym	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ cycle time	t _{RC}	10		12		15		17		20		25		ns
Address access time	t _{AA}		10		12		15		17		20		25	ns
Chip enable access time	t _{ACE}		10		12		15		17		20		25	ns
Output hold from address change	t _{OH}	3		3		3		3		3		3		ns
Chip enable to output in low Z ^(1, 3)	t _{LZCE}	5		5		5		5		5		5		ns
Chip disable to output in high Z ^(1, 2, 3)	t _{HCZE}		6		6		7		7		8		10	ns
Chip enable to power up time ⁽³⁾	t _{PU}	0		0		0		0		0		0		ns
Chip disable to power down time ⁽³⁾	t _{PD}		10		12		15		17		20		25	ns
Output enable access time	t _{AOE}		6		6		6		6		6		8	ns
Output Enable to output in low Z ^(1, 3)	t _{LZOE}	0		0		0		0		0		0		ns
Output disable to output in high Z ^(1, 3)	t _{HZOE}		6		6		6		6		6		8	ns

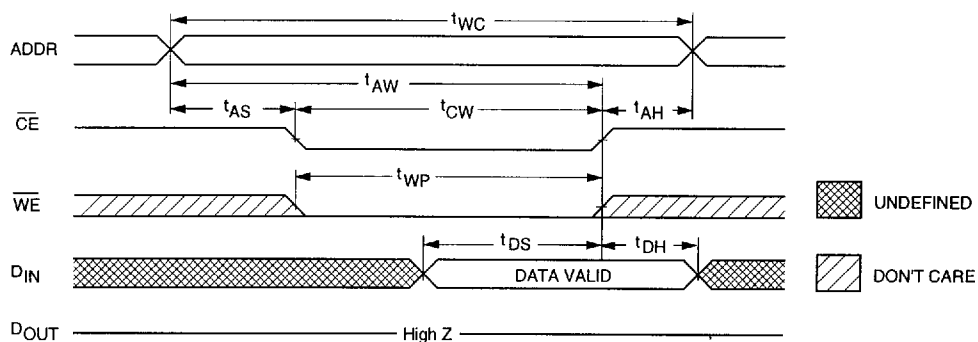
SHADED AREA = PRELIMINARY DATA

Notes referenced are after Data Retention Table.

Write Cycle No. 1 (Write Enable Controlled)



Write Cycle No. 2 (Chip Enable Controlled)

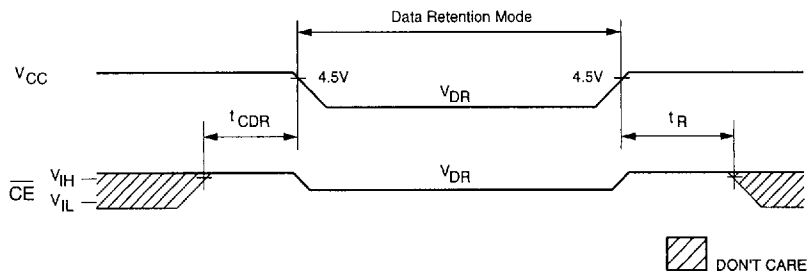


NOTE: Output Enable ($\overline{\text{OE}}$) is inactive (high)

AC Electrical Characteristics ($V_{CC} = 5V \pm 10\%$, All Temperature Ranges)

Description	Sym	-10 ⁽⁷⁾		-12 ⁽⁷⁾		-15		-17		-20		-25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE Cycle time	t_{WC}	10		12		15		17		20		25		ns
Chip enable access time	t_{CW}	10		10		11		12		13		15		ns
Address Valid to end of write	t_{AW}	10		10		11		12		13		15		ns
Address setup time	t_{AS}	0		0		0		0		0		0		ns
Address hold from end of write	t_{AH}	0		0		0		0		0		0		ns
Write pulse width	t_{WP1}	9		10		11		12		13		15		ns
Write pulse width	t_{WP2}	10		11		12		13		14		15		ns
Data setup time	t_{DS}	7		7		7		8		8		10		ns
Data hold time	t_{DH}	0		0		0		0		0		0		ns
Write disable to output in low $Z^{(1,3)}$	t_{LZ}	0		0		0		0		0		0		ns
Write enable to output in high ^(1,3)	t_{HZWE}		7		7		7		7		8		10	ns

SHADED AREA = PRELIMINARY DATA

Low V_{CC} Data Retention Waveform**Data Retention Electrical Characteristics (L Version Only)**

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{DR}	VCC for Retention Data			2	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	$V_{CC} = 2V$ $V_{CC} = 3V$	—	—	500 750	μA
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	ns
$t_R^{(3)}$	Operation Recovery Time			t_{RC}	—	—	ns

NOTES: (For 3 previous Electrical Characteristics tables)

1. The parameter is tested with $C_L = 5$ pF as shown in Fig. #2. Transition is measured ± 200 mV from steady state voltage.
2. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} .
3. This parameter is sampled.
4. WE is high for a READ cycle.
5. The device is continuously selected. All the Chip Enables are held in their active state.
6. The address is valid prior to or coincident with the latest occurring Chip Enable.
7. $V_{CC} = 5V \pm 5\%$.

Ordering Information

PDM	XXXXX	A	XX	A	A	Process / Temperature Range	
Device Type						Power	
						Speed	
						Package	
						Process / Temperature Range	
						Blank	Commercial (0° to +70°C)
						I	Industrial (-40°C to +85°C)
						P	28-pin 400 mil Plastic DIP
						D	28-pin 400 mil CerDIP
						TSO	28-pin 300 mil Plastic SOJ
						SO	28-pin 400 mil Plastic SOJ
						T	28-pin Plastic TSOP
						10	Commercial Only
						12	
						15	
						17	
						20	
						25	
						SA	Standard Power
						LA	Low Power
						41028	1 Meg (256K x 4) Static RAM

Chip	Package Type
PDM41028	28-pin Plastic DIP
	28-pin Cerdip
	28-pin Plastic SOJ
	28-pin Plastic TSOP