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SSI 32H6810/6810A
5V Servo & Motor Speed Drivers

Advance Information

January 1993

T-52-38

DESCRIPTION

The 32H6810/6810A combines the head positioning and spindle motor electronics with internal power FETs. It also provides voltage fault logic and over-temperature protection.

The positioner section serves as a transconductance amplifier by driving 4 internal FETs in an H-bridge configuration and performs motor current sensing. Class B operation is guaranteed by crossover protection circuitry, which ensures that only one FET in each leg of the H-bridge is active. It also offers over-temperature protection by disabling the output FETs. In addition, automatic head retraction may be initiated by a low voltage condition or upon external command.

(continued)

FEATURES

- **48-lead TQFP package**
- **NMOS output stage, no blocking diode required**
- **Internal 1.0A power devices**
- **Total spindle on resistance less than**
  2.5Ω: 32H6810
  1.7Ω: 32H6810A
- **No deadband, low distortion, class B servo driver output**
- **Thermal overload protection**

(continued)

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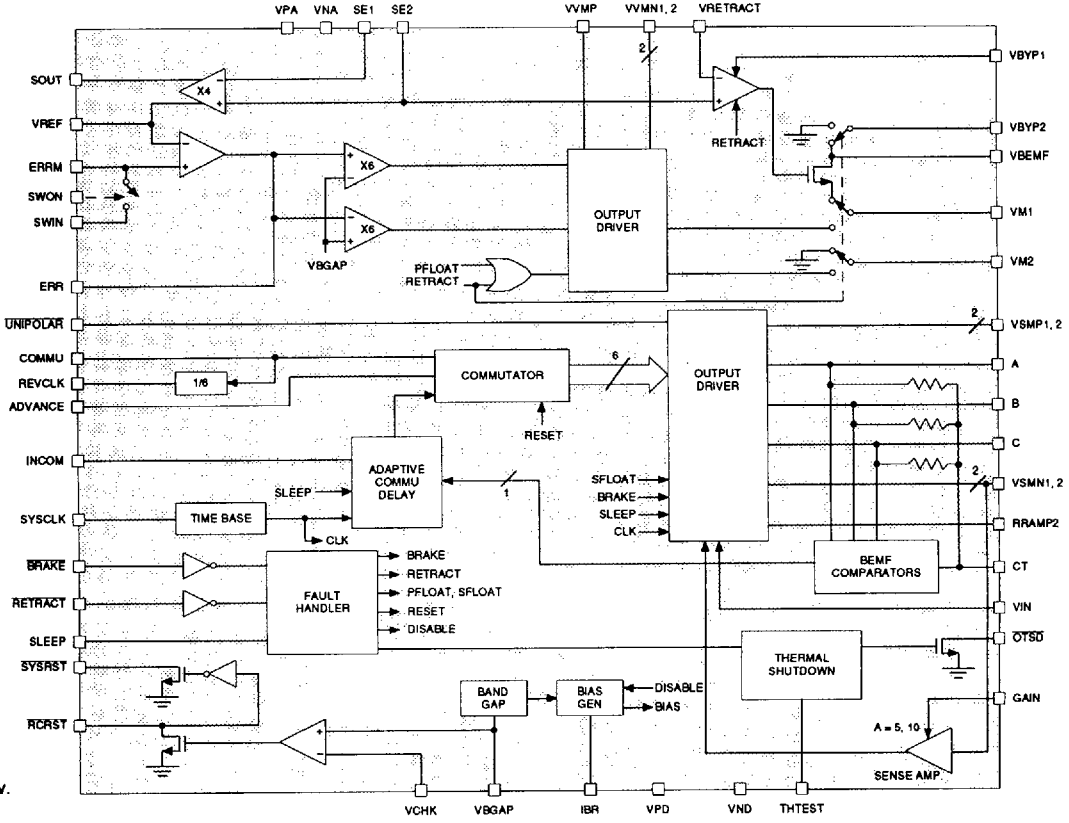
BLOCK DIAGRAM



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FEATURES (continued)

- **Built-in retract circuitry**
- **Multiple Brake/Coast/Retract modes**
- **Power fault detect & retract circuitry**
- **Optimum commutation without external components or Hall sensors**
- **Reduced DV/DT on commutation – no snubber networks required**
- **Both Unipolar and Bipolar operating modes**

DESCRIPTION (continued)

The (Spindle) Motor Commutator in conjunction with external components, provides the motor driving capability for starting, accelerating, and rotational speed regulation for brushless DC motors without the need for Hall sensors. Control is accomplished via five pins (plus 2 optional pins INCOM & $\overline{\text{UNIPOLAR}}$) and operation is monitored via three pins (plus optional pin REVCLK). The speed regulation control loop is completed with a microprocessor or signal processor external to the SSI 32H6810/6810A.

Motor speed control may be accomplished by measuring the period of the output signal COMMU. Motor armature position is determined by monitoring the coil voltage of the winding that is not presently being driven by the drivers. The back-emf from the coil in conjunction with the state of the output drivers, indicates armature position.

The back emf is compared to a reference (CT) and initiates commutation "events" when the appropriate comparison is made. (Commutation is the sequential switching of drive current to the motor windings.) Because the back-emf comparison event occurs prior to the time when optimum commutation should occur, it is preferred to delay commutation by a predetermined time after the comparison. The commutation delay is provided by circuitry which measures the interval between comparison events and delays commutation by a time equal to 3/7 of the prior measured interval. The circuit is adaptive and will provide the optimum delay for a wide range of motor speeds (-80% to +50% of nominal). Since the commutation of motor coils typically causes transients, the commutation delay circuit also provides a noise blanking function which prevents response to back-emf comparison events for a period of time equal to 4/7 of the interval (between events) after the comparison event. The commutation states are given in Table 1.

Input pin VIN is the non-inverting input of a linear transconductance amplifier which uses the lower driver transistor that is presently active per the commutation state as the power driver element. An external resistor Rsense is used to sense the current in the drive transistor source VSMN (and hence the motor coil current). The voltage across the sense resistor is amplified by a gain stage (Av = 5) and fed to the inverting input of the transconductance output stage.

The output pins A, B, and C are intended to drive motor coils directly. The output drivers operate to reduce switching noise transients by limiting dv/dt during commutation. Each output consists of two n-channel MOSFET drivers, one for pull-up to VSMP and one for pull-down to VSMN. The pull-up looks like a switch (1.5 Ω maximum) with voltage rise and fall times of about 25 microseconds. The pull-down transistor is part of the transconductance amplifier which converts VIN into motor current (Imotor = VIN/(Rsense • 5)). When the pull-down output is commutating to the "off" state, dv/dt is controlled such that dv/dt is approximately 1.5E10/Rramp volts per second.

Motor starting is accomplished by a companion microprocessor utilizing ADVANCE, SLEEP, $\overline{\text{BRAKE}}$ and COMMU. The microprocessor can control SLEEP and $\overline{\text{BRAKE}}$ to initialize the commutation counter and then increment the counter with ADVANCE. Reset with SLEEP = low and $\overline{\text{BRAKE}}$ = low then enable with $\overline{\text{BRAKE}}$ = high (power-up condition and preparation to begin a starting sequence), the commutation state will be state 0 per Table 1, but lower driver output B remains inactive to prevent current flow through the motor (out of A which is "high"). On the first ADVANCE set high, commutation state 1 is selected and the drivers are per Table 1. ADVANCE at logic high excludes internal commutations. COMMU provides feedback to the microprocessor on motor activity.

Seven operating conditions are selected via $\overline{\text{BRAKE}}$, SLEEP and $\overline{\text{RETRACT}}$ (when VPA is present) as indicated by Table 2. If VPA is not present (VCHK < VBGAP), power for the braking circuitry during retract and spin-down is provided by the charge stored on an external capacitor on pin VBYP1, power for the retract circuitry is provided by the back emf voltage and the retract circuitry itself is driven by charge stored on the capacitor between VBYP1 and VBYP2.

STATE	COMMU	Pull-Downs A	B	C	Pull-Ups A	B	C
0, (Reset state)	0	off	on (1)	off	on	off	off
1	1	off	off	on	on	off	off
2	0	off	off	on	off	on	off
3	1	on	off	off	off	on	off
4	0	on	off	off	off	off	on
5	1	off	on	off	off	off	on
(1) B is off in reset state, see text.							

TABLE 1: Commutation States

VCHK>VBGAP	SLEEP	$\overline{\text{BRAKE}}$	$\overline{\text{RETRACT}}$	CONDITION	ANALOG	POSITIONER	A, B, C
0	X	1	X	Power Fault	On	Retract	Float
0	X	0	X	Power Fault	On	Retract	Low Z to GND
1	1	1	1	Sleep	Off	Float	Float
1	1	0	1	Sleep/Brake	Off	Float	Low Z to GND
1	1	0	0	Sleep/Retract	Off	Retract	Low Z to GND
1	1	1	0	Sleep/Retract	Off	Retract	Float
1	0	0	X	Brake/Retract	On	Retract	Low Z to GND
1	0	1	0	Retract (Spindle Run)	On	Retract	Active
1	0	1	1	Run	On	Active	Active
X	X	X	X	Thermal Shutdown	On	Float	Float

TABLE 2: Operating Mode Control

NOTES:
1. $\overline{\text{BRAKE}}$ internally linked to force retract.
2. Voltage fault circuit is never turned off.
3. Counter is reset when sleep input is high.

The circuit also provides an over temperature detection function. If the die temperature exceeds 135°C (approximately), $\overline{\text{OTSD}}$ is asserted low and all output drivers are turned off. The drivers will become operative after the temperature is reduced and ADVANCE is asserted high.

PIN DESCRIPTION

POWER SUPPLIES

NAME	TYPE	DESCRIPTION
VPA	I	Supply: Analog positive power supply.
VNA	I	Ground: Analog ground.
VPD	I	Supply: Digital positive power supply.
VND	I	Ground: Digital ground. VND is circuitry ground and also the low side input to the current SENSE amplifier and thus care should be taken to see that VND and the low side of the external Rsense resistor are at the same potential.
VVMP	I	Supply: Positve supply for voice coil motor.
VVMN1, VVMN2	I	Supply: Negative supply for voice coil motor.

POSITIONER

SWON	I	Turns on the switch between ERRM and SWIN.
SWIN	I	Analog switch, the other side of the switch is connected to ERRM.
SOUT	O	The current sense amplifier output. SOUT is referenced to VREF.
ERR	O	The error amplifier output. ERR is used to provide compensation to the transconductance loop. ERR is referenced to VBGAP.
ERRM	I	The error amplifier negative input.
VREF	I	The reference voltage for the error amplifier and the current sense amplifier.
VRETRACT	I	The retract voltage. If left open, the retract voltage will be the default setting. This value can be over-ridden by biasing VRETRACT externally.
VM1	O	Connection for voice coil motor and sense resistor.
VM2	O	Connection for the other side of voice coil motor.
SE1, SE2	I	Sense voltage on the sense resistor.

MOTOR SPEED CONTROL

SYSCLK	I	System clock (input) pin. SYSCLK is 2.00 MHz nominal and is used to generate internal timing signals assuming a nominal 3600 RPM, 8-pole motor environment.
COMMU	O	Commutation count pin. COMMU is the LSB of the commutation counter.
REVCLK	O	REVCLK is COMMU divided by six.
$\overline{\text{UNIPOLAR}}$	I	Unipolar mode (inverse) select pin. This pin will turn all upper drivers off when low. Pulled high internally to provide the default bipolar mode.

MOTOR SPEED CONTROL (continued)

NAME	TYPE	DESCRIPTION
ADVANCE	I	Advance pin. ADVANCE is controlled by microprocessor during start mode to increment the commutation counter. The rising edge of ADVANCE will increment the counter. ADVANCE held high will inhibit internal incrementing of the counter, ADVANCE held low permits the normal operation of commutation from back-emf events.
INCOM	I	Commutation delay control pin. Adaptive commutation delay may be adjusted from its nominal value of one half the commutation interval by inserting or withdrawing current ot this pin. This should only be done via an external control loop which can compensate for the range of internal circuit parameter variations.
VIN	I	Control Voltage input pin. The internal driver transistors and internal predriver circuits form a transconductance amplifier which will set motor current in relation to VIN. In conjunction with Rsense at VSMN input and the gain of the Sense amplifier, transconductance (Gm) will be Gm = Im/VIN = 1/ (Rsense • 5).
A, B, C	O	Motor Drive Outputs. These pins provide drive to the motor coils.
CT	I	Back EMF input from motor coil center tap. Input connected to the center tap for sensing generated back emf voltages. It is also derived internally from A, B, C through a resistor network (y-connection). The circuit uses the back-emf voltages to determine rotor position and effect commutation.
RRAMP	I	Lower driver turn-off dv/dt setting resistor. External resistor from VPD to this pin sets the dv/dt slope of the motor coil voltage when the lower drivers are commutating to the off state. The dv/dt is given approximately by the relationship dv/dt (volts/second) = 1.5 • 10E10/Rramp. Typical value: RRAMP = 200K.
GAIN	I	Sense amplifier gain control pin. In normal operation, this pin is tied to high to set sense amplifier gain = 5. In low motor current operation, amplifier gain = 10 can be set by tying this input to low.
VSMP	I	Supply: Positive supply for spindle motor.
VSMN1, VSMN2	I	Supply: Negative for spindle motor. Current monitoring sense amplifier (high side) input pin and motor current returns to ground. **All pins must be connected with low resistance circuit board traces.** The lower driver transistor current (hence motor current) comes out of these pins to Rsense resistor to monitor motor current. During normal (at speed) operation, the circuit will control the voltage across this resistor (multiplied by the gain of 5 in the sense amplifier) to match VIN.
		VVMP, VVMN, VSMP and VSMN conductors must be sized in accordance with anticipated motor current. The analog and digital supplies should be bypassed separately. VPA and VPD should be shorted externally, VNA and VND should be shorted externally.

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PIN DESCRIPTION

MISCELLANEOUS

NAME	TYPE	DESCRIPTION
VBYP1	I	The bypassed power supply. An external voltage for BRAKE and RETRACT circuitry. An external capacitor is attached to this pin and an internal circuit will charge this pin to VCC. The charge on this capacitor is used by the brake and retract function when VCC is removed (power-off). The capacitor must hold sufficient charge during the period when VCC is lost while retract is taking place (20 to 50 ms) so it will have enough voltage to drive the outputs during braking. Very little current is used during power-off braking so that C can be chosen from the retract conditions: C ≥ Tretract • Ivbyp (float mode) / .5 volt or approximately: C ≥ 500E-6 • Tretract This pin is normally a diode drop below VPA, rising by VBEMF during retract.
VBYP2	I	The other side of the bypass capacitor connection. This pin is normally at VNA, rising to VBEMF during retract.
VBEMF	I	Rectified spindle back emf voltage. This voltage drives the internal retract FET.
SLEEP	I	Sleep pin. When asserted high, internal counters and registers are cleared. Refer to Table 2. Also forces an internal voltage fault which causes a head retract. Disables all output drivers, powers down all other circuitry except the over-temperature and voltage fault circuitry.
$\overline{\text{RETRACT}}$	I	Retract (inverse) pin. When asserted low, forces a retract. Refer to Table 2.
$\overline{\text{BRAKE}}$	I	Brake (inverse) pin. $\overline{\text{BRAKE}}$ is used to provide a delay between the initiation of fault-induced head retract and motor braking. A capacitor to ground and a resistor to $\overline{\text{SYSRST}}$ are selected such that 1.2 • R • C is equal to the maximum time required for retract. Refer to Table 2.
$\overline{\text{OTSD}}$	O	Over-Temperature Sense Detect. Excessive die temperature will bring this open drain output low. Spindle motor and positioner drivers are disabled whenever $\overline{\text{OTSD}}$ is asserted.
VCHK	I	Comparator input for power supply monitoring.
VBGAP	O	An internal voltage reference for use with the power supply monitor comparator.
IBR	O	A resistor is tied from this pin to ground to establish the bias current for internal circuitry.
$\overline{\text{RCRST}}$	I/O	This pin serves the dual purpose of providing power on reset and stretching short VFAULT pulses to a width suitable for the host microcontroller. An external RC network sets the minimum width of any $\overline{\text{SYSRST}}$ pulse.
$\overline{\text{SYSRST}}$	O	When low, this open drain output indicates that an internal voltage fault has occured or that $\overline{\text{RCRST}}$ has been pulled low.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	VPA, VPD, VVMP, VSMP (1, 2)	-0.3 -0.3	7.0 7.0	V V
Output Current	Imax (in or out of A, B, C, VM1, VM2)	-1.0	1.0	Amp
Analog I/O	VIN, RRAMP,	-0.3	VPD + 0.3	V
Voltage on pins	CT, A, B, C, VBEMF, VBYP1, VBYP2	-0.3	12.0	V
	VM1, VM2, SE1, SE2	-0.3	7.0	V
	All other pins	-0.3	VPD + 0.3	V
Storage Temperature	Tstg	-65	150	°C
Lead Temperature (10 sec duration)	Tlead	0	300	°C

OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	VPA, VPD VVMP, VSMP	4.5 4.5	5.5 5.5	V V
Supply Current	I (VPA + VPD)		20	mA
	I (VPA + VPD + VVMP + VSMP) Sleep mode		20	mA
	IVVMP		0.4	A
	IVSMP		0.5	A
VBEMF		1.0	10.0	V
VREF		0.5	VPA-2	V
VIN		0	2.5	V
Vin, VSMN1, VSMN2 *	Normal operation	0.0	0.50	V
RF		10		kΩ
RC		10		kΩ
RBIAS		112	114	kΩ
Ambient Temperature	Ta	0	70	°C
Capacitive Load Digital I/O	Cl	0	100	pF

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OPERATING CONDITIONS (continued)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Analog Outputs	CI	0	50	pF
Resistive Load Analog Outputs	RI	10		kΩ
Power Dissipation	Pd		500	mW

* Transconductance gain from VIN to motor current (steady-state) will be given by: G = Imotor/VIN = 1/(Rsense • 5)

PARAMETRIC REQUIREMENTS

Digital Input/Output

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Fclk, SYSCLK		1.5		2.5	MHz
Twh, Twl, SYSCLK width high or low		40			ns
Input Leakage ($\overline{\text{UNIPOLAR}}$)		-50		10	µA
Input Leakage (all other pins)				10	µA
Vil ($\overline{\text{BRAKE}}$)				1.2	V
Vih ($\overline{\text{BRAKE}}$)		2.0			V
Vil (all other digital inputs)				0.8	V
Vih (all other digital inputs)		2.0			V
Output Sink current	Vo = 0.4V	1.6			mA
$\overline{\text{RCRST}}$, $\overline{\text{OTSD}}$					
$\overline{\text{SYSRST}}$	Vo = 0.4V	4.0			mA

Digital Output COMMU, REVCLK

Voh	Iout = -100 µA	2.4			V
Vol	Iout = 2.0 mA			0.4	V

VIN

Input Current	0 ≤ Vin < 2.5V	-1		+1	µA

Outputs A, B, C

Total voltage drop	32H6810	Imotor = 200 mA, V_{PD} = 4.5V			0.5	V
across power FETs	32H6810A	Imotor = 500 mA, V_{PD} = 4.5V			0.85V	V

CT, And A, B, C, When Not Driving

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Rin	-0.3V ≤ Vin < 7V	5K	9K		Ω
Cin @ CT				20	pF
Cin @ A, B, C				200	pF

VBYP1

IVBYP1 (run)	VDD = 4.5V			100	µA
IVBYP1 (retract)	VDD = 0.5V, VBYP1 = 3V			20	µA
IVBYP1 (brake)	VDD ≤ 0.5V, VBYP1 = 3V			10	µA

BEMF

IBEMF	VBEMF = 4V			300	µA
IBEMF (retract)	I (VM1) = I (VM2) = 0, I (VBYP2) = 0			20	µA

SOUT

Gain		3.9		4.1	V/V
Input Offset	SOUT = VREF	-3		3	mV
Output Swing	R_L = 10 kΩ to VREF	0.15		VP-1	V

ERR

ERRM Input Offset	ERR = ERRM	-15		15	mV
ERR Output Swing		1.55		VP -1.25	V

POSITIONER

(VM1 - VM2) / (ERR - VBGAP)		11		13	V
Crossover Time	Imotor = 10 mA, PP @ 1 KHz, RL= 16Ω, RSENSE = 0.5Ω		10	25	µs
Output Distortion	Imotor = 100 mA, PP @ 100 Hz RL= 16Ω, RSENSE = 0.5Ω			2	%THD

VBGAP

Bandgap Voltage	Iout < ±0.2 mA	2.13		2.37	V

VCHK

Offset		-15		15	mV

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OUTPUT VM1, VM2

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Total voltage drop across power FETs	I = 400 mA			1.0	V

SWIN

On Resistance				250	Ω

RETRACT

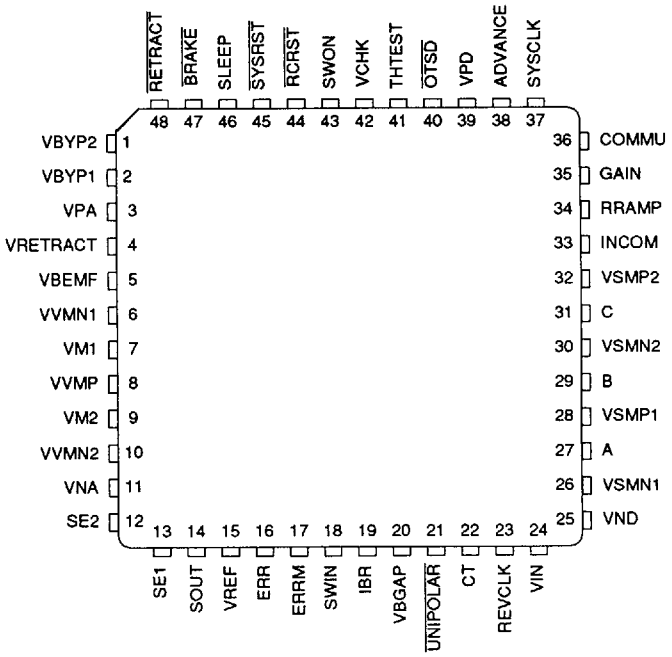
VRETRACT Offset	VRETRACT = 0.1V VBEMF ≥ 1V RL = 16Ω	-100		0	mV
Short Circuit Current	VRETRACT = 0.5V VBEMF = 1V VBYP1 = 4.5V VM1 = VM2	60			mA
	VRETRACT = 0.5V VBEMF = 1.5V VBYP1 = 4.5V VM1 = VM2	100			mA

$\overline{\text{OTSD}}$ (Thermal Shutdown)

Die temperature		125		145	°C

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



48-Lead TQFP

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Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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