12-Bit Parity Generator Checker

ELECTRICALLY TESTED PER:
5962-8756201

The 10H560 is a 12-bit parity generator-checker. The output goes high when an odd number of inputs are high providing the odd parity function. Unconnected inputs are pulled to a logic low allowing parity detection and generation for less than 12 bits.

The 10H560 is a functional pin duplication of the standard 10K family part with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 2.5 ns Typical
- 480 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

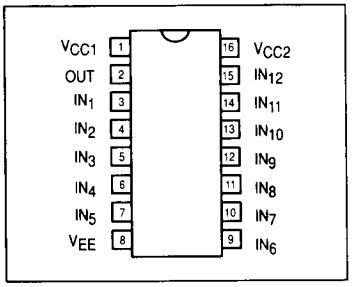
1) JAN: N/A
2) SMD: 5962-8756201
3) 883: 10H560/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

PIN ASSIGNMENTS

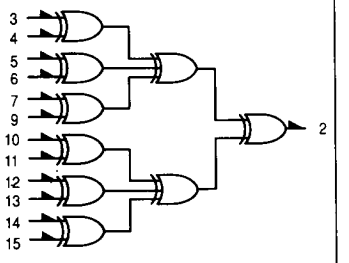
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Out	2	6	3	51 Ω to V_{TT}
IN_1	3	7	4	GND
IN_2	4	8	5	OPEN
IN_3	5	9	7	OPEN
IN_4	6	10	8	OPEN
IN_5	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
IN_6	9	13	12	OPEN
IN_7	10	14	13	GND
IN_8	11	15	14	OPEN
IN_9	12	16	15	OPEN
IN_{10}	13	1	17	OPEN
IN_{11}	14	2	18	OPEN
IN_{12}	15	3	19	GND
V_{CC2}	16	4	20	GND

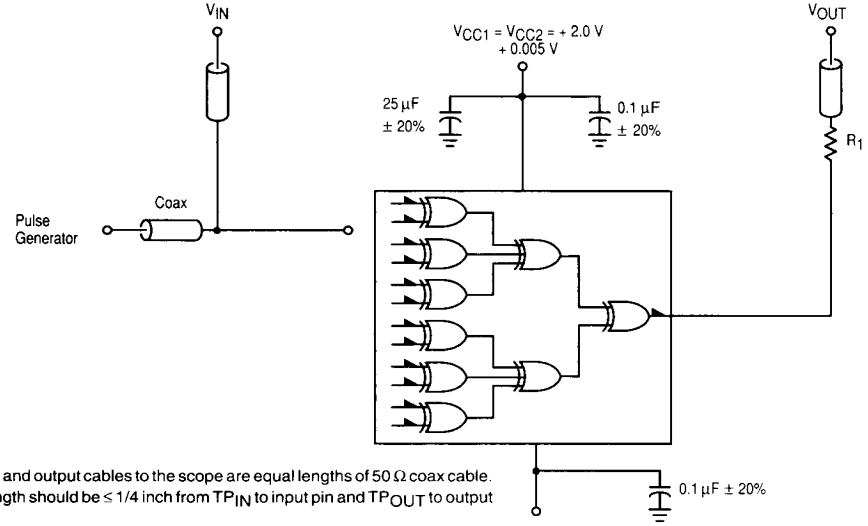


BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

Truth Table	
Input	**Output**
Sum of High Level Inputs	Pin 2
Even	Low
Odd	High

POSITIVE LOGIC DIAGRAM





NOTES

1. All input and output cables to the scope are equal lengths of 50 Ω coax cable. Wire length should be ≤ 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin.
2. R_1 = 50 Ω.
3. $t_r = t_f$ = 1.0 ns ± 0.1 ns (20% - 80%).
4. $P_W \geq 20$ ns.
5. P_{RR} = 1.0 MHz.

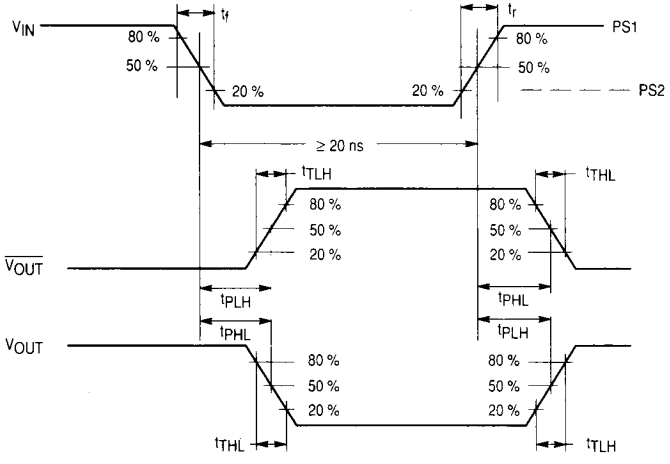


Figure 1. Switching Test Circuit and Waveforms

10H560
QUIESCENT LIMIT TABLE *

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.10	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE2}	V_{EE1}	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	3 - 7 9 - 15	3 - 7				8	1, 16	2
V_{OL}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V	3 - 7 9 - 15	3 - 7 9 - 15				8	1, 16	2
V_{OH1}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	3 - 7 9 - 11 13	4 - 7 9 -15	3, 5, 7 10, 12 14	12	8	8	1, 16	2
V_{OL1}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V	3 - 7 9 - 14	4 - 7 9 -15	4, 6, 9 11, 13 15	3	8	8	1, 16	2
I_{EE}	Power Supply Current	-78		-88		-88		mA						8	1, 16	8
I_{IH}	Input Current High		245		390		390	µA	4, 5, 9 10, 13, 14					8	1, 16	4, 5, 9, 10, 13, 14
I_{IH1}	Input Current High		285		455		455	µA	3, 6, 7 11, 12 15					8	1, 16	3, 6, 7, 11, 12, 15
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		3 - 7 9 - 15				8	1, 16	3 - 7, 9 - 15

10H560
QUIESCENT LIMIT TABLE *

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Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.10	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		P_{S2}	V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P.U.T.
t_{TLH}	Rise Time	0.55	1.8	0.75	1.9	0.55	1.8	ns	4 - 7, 9 - 15	4 - 7, 9 - 15	2	1, 16	8	4 - 7, 9 - 15	2
t_{THL}	Fall Time	0.55	1.8	0.75	1.9	0.55	1.8	ns	4 - 7, 9 - 15	4 - 7, 9 - 15	2	1, 16	8	4 - 7, 9 - 15	2
t_{PLH1}	Propagation Delay (3, 5, 7, 10, 12, 14)	1.2	2.9	1.35	3.2	1.15	2.8	ns	4 - 7, 9 - 15	4 - 7, 9 - 15	2	1, 16	8	4 - 7, 9 - 15	2
t_{PHL1}	Propagation Delay (3, 5, 7, 10, 12, 14)	1.45	3.0	1.7	3.4	1.4	2.8	ns	4 - 7, 9 - 15	4 - 7, 9 - 15	2	1, 16	8	4 - 7, 9 - 15	2
t_{PHL2}	Propagation Delay (3, 5, 7, 10, 12, 14)	1.3	2.9	1.55	3.2	1.25	2.9	ns	4 - 7, 9 - 15	4 - 7, 9 - 15	2	1, 16	8	4 - 7, 9 - 15	2
t_{PLH2}	Propagation Delay (3, 5, 7, 10, 12, 14)	1.4	3.2	1.55	3.6	1.35	2.8	ns	4 - 7, 9 - 15	4 - 7, 9 - 15	2	1, 16	8	4 - 7, 9 - 15	2
t_{PLH1}	Propagation Delay (4, 6, 9, 11, 13, 15)	1.1	2.9	1.25	3.2	1.05	2.7	ns	4 - 7, 9 - 15	4 - 7, 9 - 15	2	1, 16	8	4 - 7, 9 - 15	2
t_{PHL1}	Propagation Delay (4, 6, 9, 11, 13, 15)	1.15	2.7	1.35	3.2	1.1	2.6	ns	4 - 7, 9 - 15	4 - 7, 9 - 15	2	1, 16	8	4 - 7, 9 - 15	2
t_{PHL2}	Propagation Delay (4, 6, 9, 11, 13, 15)	1.2	2.8	1.45	3.0	1.15	2.6	ns	4 - 7, 9 - 15	4 - 7, 9 - 15	2	1, 16	8	4 - 7, 9 - 15	2
t_{PLH2}	Propagation Delay (4, 6, 9, 11, 13, 15)	1.1	3.0	1.25	3.3	1.1	2.8	ns	4 - 7, 9 - 15	4 - 7, 9 - 15	2	1 ,16	8	4 - 7, 9 - 15	2