REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
SHEET																								
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REV STATUS OF SHEETS	REV																							
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18					

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Todd D Creek

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APPROVED BY: Michael A. Frye

DRAWING APPROVAL DATE: 7 APRIL 1988

REVISION LEVEL:

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, CMOS, TIMING CONTROL UNIT, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-88599

SHEET 1 OF 18

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E836

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-88599	01	J	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Frequency
01	32C201	Timing control unit	10 MHz

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
J	D-3 (24-lead, 1.290" x .610" x .225"), dual-in-line package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to 7.0 V dc
Input voltage range	-0.5 V dc to 5.5 V dc
Output voltage range	-0.5 V dc to 5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation	1.0 W
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	+150°C
Thermal resistance, junction-to-case (θ_{JC})	(See MIL-M-38510, appendix C)

1.4 Recommended operating conditions.

Case operating temperature range	-55°C to +125°C
Operating supply voltage range	4.75 V dc to 5.25 V dc
Minimum high level input voltage	2.0 V dc
Maximum low level input voltage	0.8 V dc
Minimum high level input voltage (X_{IN} only)	3.8 V dc
Maximum low level input voltage (X_{IN} only)	1.0 V dc
Frequency of operation	10 MHz

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Functional block diagram. The functional block diagram shall be as specified on figure 2.

3.2.3 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol 1/	Conditions 2/ $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 5\%$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Input high voltage	V_{IH}	All inputs except $\overline{RSTI}$ and X_{IN}	1,2,3	2.4		V
Input low voltage	V_{IL}	All inputs except $\overline{RSTI}$ and X_{IN}	1,2,3		.8	V
$\overline{RSTI}$ rising threshold voltage	V_{T+}		1,2,3	2.0	3.5	V
$\overline{RSTI}$ hysteresis voltage	V_{HYS}		1,2,3	.8	1.9	V
X_{IN} input high voltage	V_{XH}		1,2,3	4.275		V
X_{IN} input low voltage	V_{XL}		1,2,3		.525	V
Input low current	I_{IL}	$V_{IN} = 0.0\ V$	1,2,3	-20		µA
Input high current	I_{IH}	$V_{IN} = V_{CC}$	1,2,3		+20	µA
Output low voltage	V_{OL}	I = 2 mA except PHI1, PHI2, X_{OUT}	1,2,3		.525	V
Output low voltage PHI1, PHI2	V_{OL}	I = 1 mA	1,2,3		.525	V
Output high voltage All outputs except OUT	V_{OH}	I = -1 mA	1,2,3	3.8		V

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol 1/	Conditions 2/ $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 5\%$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Three-state leakage current high	I_{ZH}	Force 5.25 V on outputs, 1 MHz	1,2,3		+20	µA
Three-state leakage current low	I_{ZL}	Force 0.4 V on outputs, 1 MHz	1,2,3	-20		µA
Supply current	I_{CC}	All outputs high F_{in} = 10 MHz	1,2,3		200	mA
Output capacitance	C_O	3/	4		50	pF
Input capacitance	C_I	3/	4		40	pF
Clock capacitance	C_{CLK}	3/	4		40	pF
Clock period	t_{CP} 7	PHI1 rising edge, to next PHI1 rising edge	9,10,11	100		ns
Clock high time	t_{CLh} 8	90 percent PHI1 rising edge, to 90 percent PHI1 rising edge	9,10,11	35	47	ns
Clock low time	t_{CLl} 9	10 percent PHI1 falling edge, to 10 percent PHI1 rising edge	9,10,11	43	60	ns
Clock pulse width	t_{CLW1} 10	At 2.0 V on PHI1 (both edges)	9,10,11	40	52	ns
Clock pulse width	t_{CLW2} 11	At 2.0 V on PHI2 (both edges)	9,10,11	40	52	ns
X_{IN} high time (external input)	t_{Xh} 1	2.5 V X_{IN} rising edge to 2.5 V X_{IN} falling edge	9,10,11	16		ns
X_{IN} low time (external input)	t_{Xl} 2	2.5 V X_{IN} falling edge to 2.5 V X_{IN} rising edge	9,10,11	16		ns
X_{IN} to FCLK rising edge delay	t_{XFr} 3	2.5 V X_{IN} rising edge to FCLK rising edge	9,10,11	3	29	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol 1/	Conditions 2/ $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 5\%$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
X_{IN} to FCLK falling edge delay	t_{XFr} 4	2.5 V X_{IN} falling edge to FCLK falling edge	9,10,11	6	29	ns
X_{IN} to CTTL rising edge delay	t_{XCR} 5	2.5 V X_{IN} rising edge to CTTL rising edge	9,10,11	3	34	ns
X_{IN} to PHI1 rising edge delay	t_{XPr} 6	2.5 V X_{IN} rising edge to PHI1 rising edge	9,10,11	3	32	ns
CTTL pulse width	t_{CTW}	At 50 percent V_{CC} on CTTL (both edges)	9,10,11	43	51	ns
Setup time	t_{RSIs} 18	Before PHI1 rising edge	9,10,11	20		ns
$\overline{RSTO}$ rising edge delay	t_{RSTr} 19	After PHI1 rising edge	9,10,11		21	ns
$\overline{ADS}$ setup time	t_{ADs} 20	Before PHI1 rising edge	9,10,11	30		ns
$\overline{ADS}$ pulse width	t_{ADw} 21	$\overline{ADS}$ leading edge to $\overline{ADS}$ trailing edge	9,10,11	25		ns
$\overline{DDIN}$ setup time	t_{DDs} 22	Before PHI1 rising edge	9,10,11	15		ns
$\overline{TSO}$ leading edge delay	t_{Tf} 12	After PHI1 rising edge	9,10,11		12	ns
$\overline{TSO}$ trailing edge delay	t_{Tr} 13	After PHI1 rising edge	9,10,11		18	ns
$\overline{RD}/\overline{WR}$ leading edge delay (fast cycle)	$t_{RWF(f)}$ 14	After PHI1 rising edge	9,10,11		35	ns
$\overline{RD}/\overline{WR}$ leading edge delay (peripheral cycle)	$t_{RWF(s)}$ 23	After PHI1 rising edge	9,10,11		25	ns
$\overline{DBE}$ leading edge delay (write cycle)	$t_{DBf(w)}$ 15	After PHI1 rising edge	9,10,11		28	ns
$\overline{DBE}$ leading edge delay (read cycle)	$t_{DBf(r)}$ 16	After PHI2 rising edge	9,10,11		21	ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol 1/	Conditions 2/ $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 5\%$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
$\overline{DBE}$ trailing edge delay	t_{DBr} 17	After PHI2 rising edge	9,10,11		23	ns
$\overline{RD}/\overline{WR}$ trailing edge delay	t_{RWr} 36	After PHI1 rising edge	9,10,11		25	ns
$\overline{CWAIT}$ setup time (cycle hold)	$t_{CWs(H)}$ 25	Before PHI1 rising edge	9,10,11	30		ns
$\overline{CWAIT}$ hold time (cycle hold)	$t_{CWh(H)}$ 26	After PHI1 rising edge	9,10,11	0		ns
$\overline{CWAIT}$ setup time (wait states)	$t_{CWs(W)}$ 24	Before PHI2 rising edge	9,10,11	10		ns
$\overline{CWAIT}$ hold time (wait states)	$t_{CWh(W)}$ 27	After PHI2 rising edge	9,10,11	20		ns
$\overline{WAITn}$ setup time	t_{Ws} 28	Before PHI2 rising edge	9,10,11	7		ns
$\overline{WAITn}$ hold time	t_{Wh} 29	After PHI2 rising edge	9,10,11	20		ns
$\overline{PER}$ setup time	t_{Ps} 30	Before PHI1 rising edge	9,10,11	5		ns
$\overline{PER}$ hold time	t_{Ph} 31	After PHI1 rising edge	9,10,11	30		ns
RDY delay	t_{Rd} 32	After PHI2 rising edge	9,10,11		25	ns
SYNC setup time	t_{Sys} 33	Before FCLK rising edge	9,10,11	6		ns
SYNC hold time	t_{Syh} 34	After FCLK rising edge	9,10,11	0		ns
CTTL/SYNC inversion delay	t_{Cs} 35	CTTL (master) to $\overline{RWEN}$/SYNC (slave)	9,10,11		10	ns

1/ Numbers included in this column are timing diagram reference numbers (see figure 3).
2/ AC loading and test circuits shall be as specified on figure 3. All the timing specifications refer to 15 percent or 85 percent of V_{CC} on the rising or falling edges of the clock phases PHI1 and PHI2, and all output signals; to 30 percent or 70 percent of V_{CC} on all the CMOS input signals, and to 0.8 V or 2.0 V on all the TTL input signals, unless specifically stated otherwise.
3/ The capacitance measurements shall be made between the indicated terminal and ground at a frequency of 1 MHz at T_C of +25°C. The dc bias of the measuring instrument shall be less than ±0.1 V. The ac signal amplitude shall be less than 50 mV rms.

Device type 01

Case J

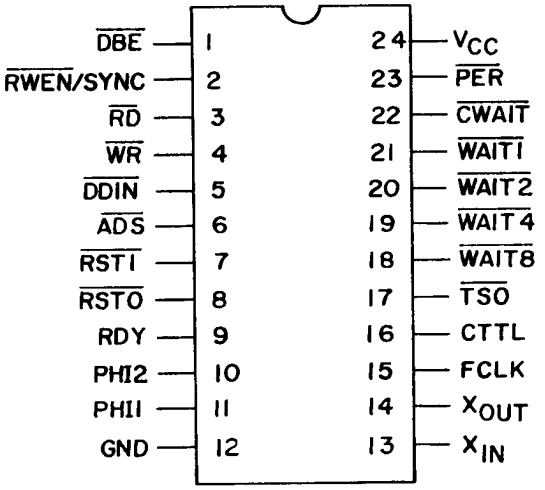

FIGURE 1. Terminal connections.

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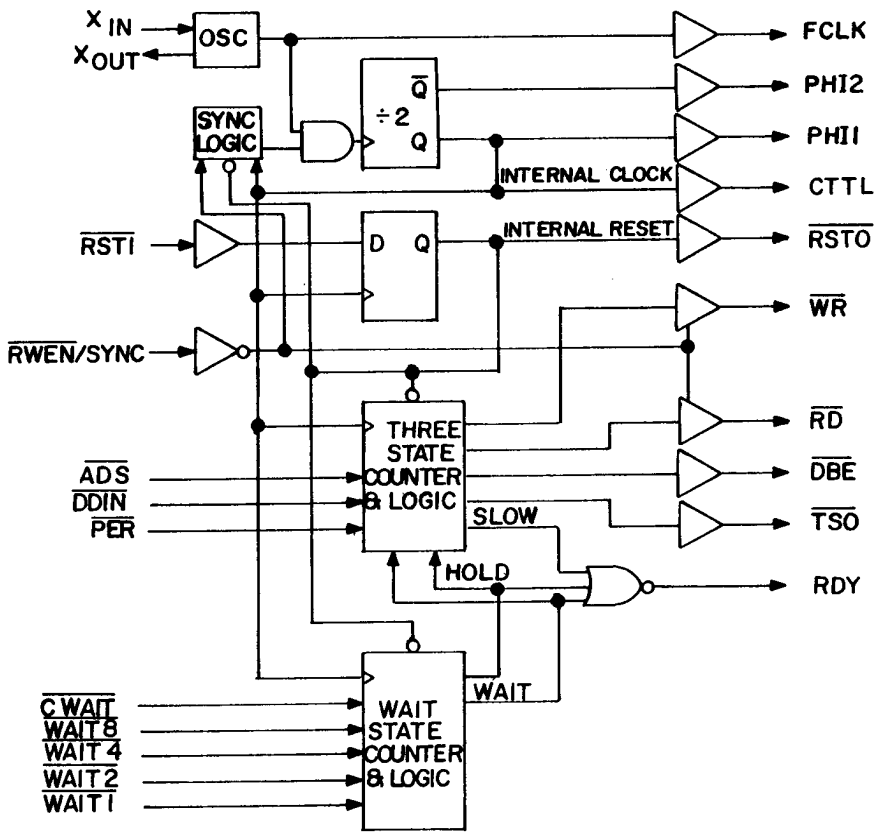
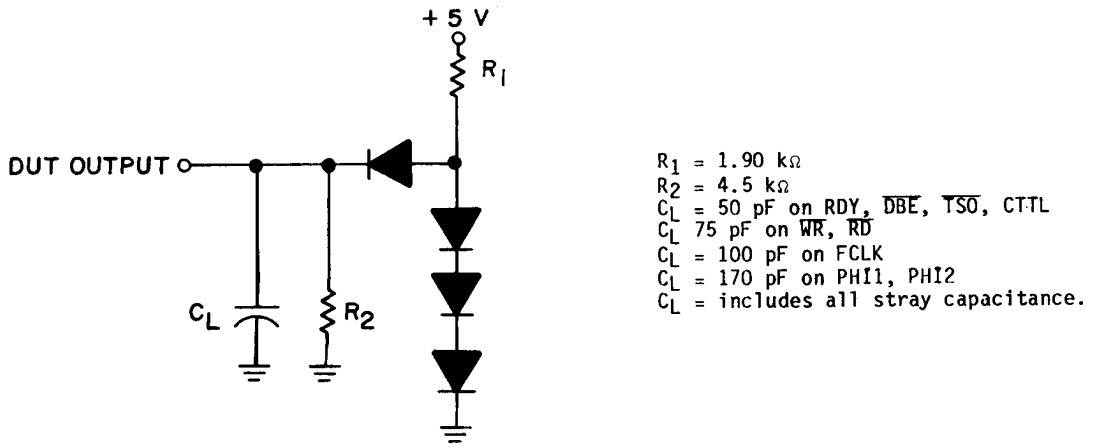
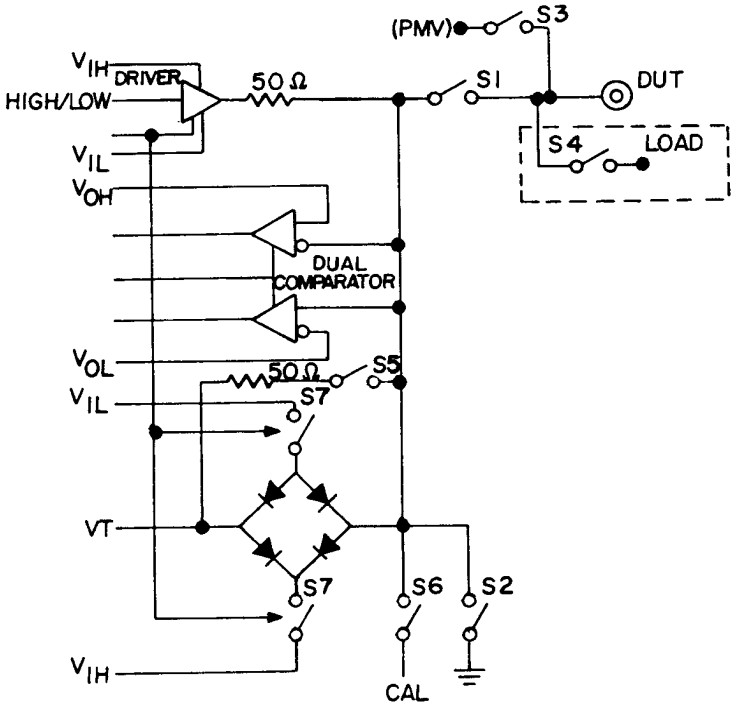


FIGURE 2. Functional block diagram.



R_1 = 1.90 kΩ
R_2 = 4.5 kΩ
C_L = 50 pF on RDY, $\overline{DBE}$, $\overline{TSO}$, CTTL
C_L 75 pF on $\overline{WR}$, $\overline{RD}$
C_L = 100 pF on FCLK
C_L = 170 pF on PHI1, PHI2
C_L = includes all stray capacitance.

OUTPUT LOAD CIRCUIT FOR AC, FUNCTIONAL, AND THREE-STATE TESTS



PROGRAMMABLE LOAD CIRCUIT FOR AC, FUNCTIONAL, AND THREE-STATE TESTS

FIGURE 3. Switching test circuits and waveforms.

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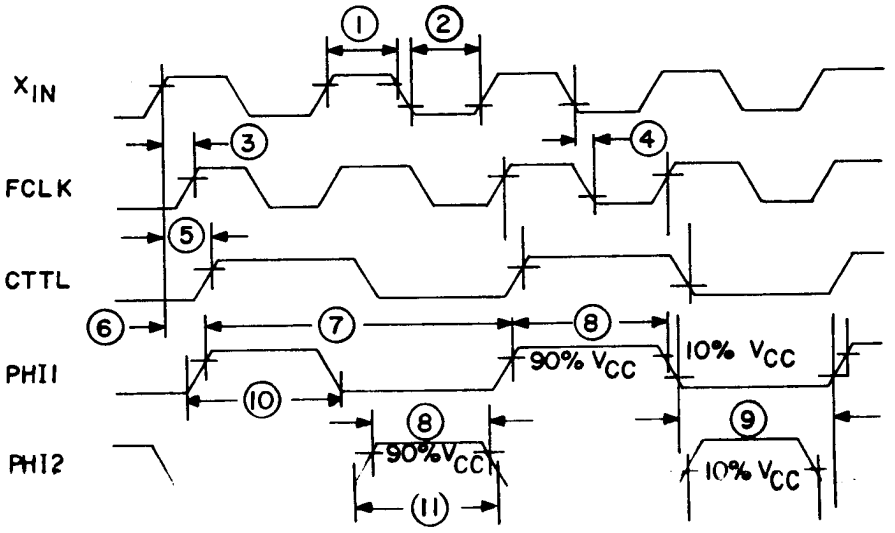
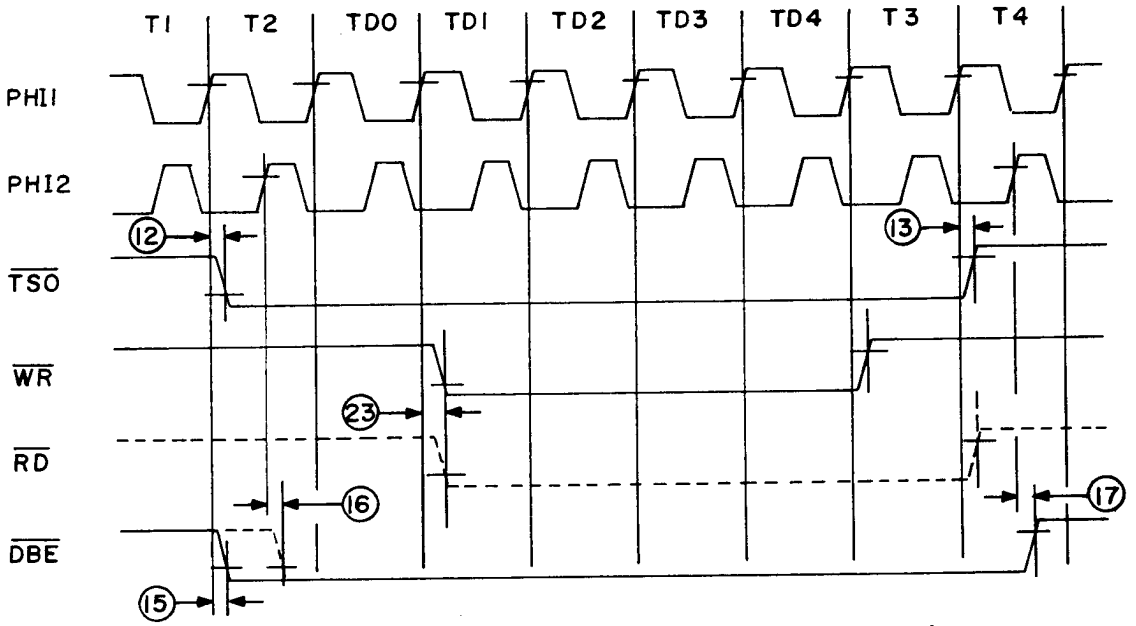


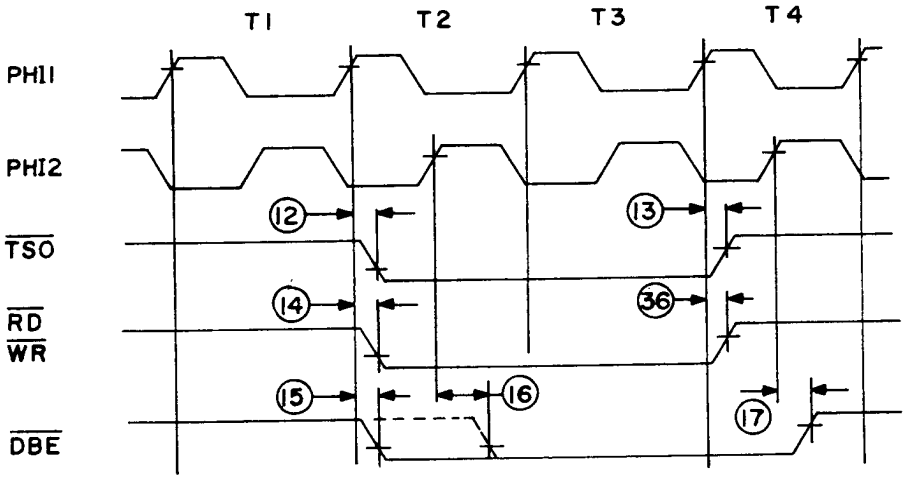
CLOCK SIGNALS

FIGURE 3. Switching test circuits and waveforms - Continued.

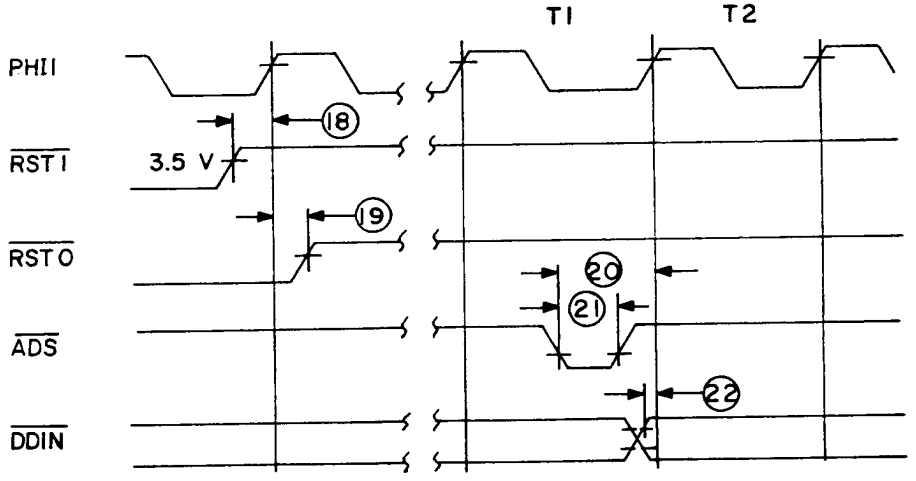


CONTROL OUTPUTS (PERIPHERAL CYCLE)

FIGURE 3. Switching test circuits and waveforms - Continued.



CONTROL INPUTS (FAST CYCLE)



CONTROL INPUTS

FIGURE 3. Switching test circuits and waveforms - Continued.

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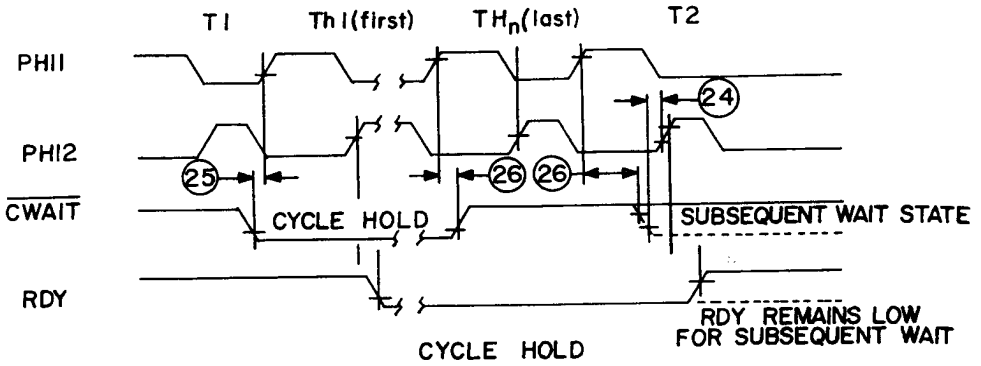
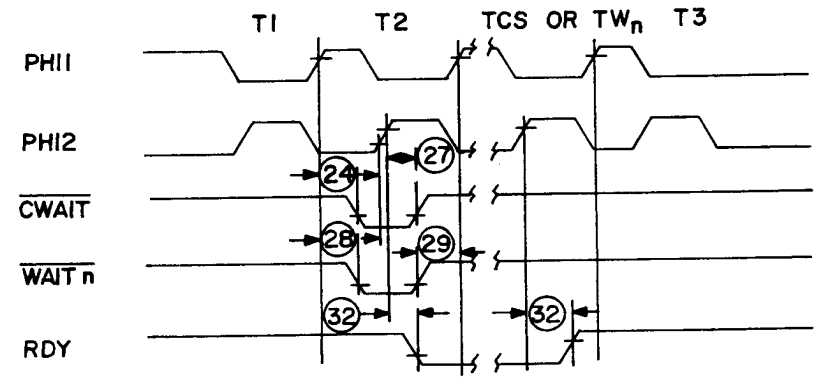




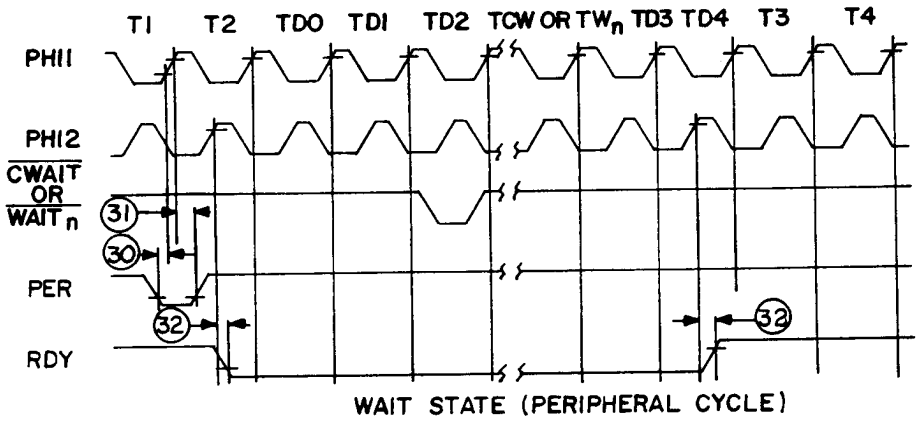
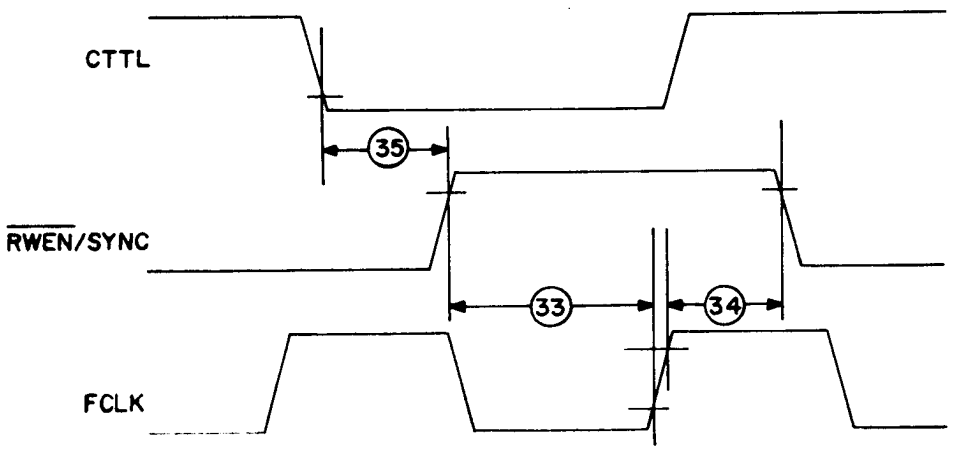


FIGURE 3. Switching test circuits and waveforms - Continued.



SYNCHRONIZATION TIMING

FIGURE 3. Switching test circuits and waveforms - Continued.

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3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_I, C_O, C_{CLK} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall consist of verifying the functionality of the device. It forms a part of the vendor's test tape and shall be maintained and available from the approved sources of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8A, 10

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the part numbered device specified in this drawing will be replaced by the microcircuit identified as part number M38510/55201.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8859901JX	27014	NS32C201D10/883	MIL-M-38510/55201BJX

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
27014	National Semiconductor Corporation 2900 Semiconductor Drive Santa Clara, CA 95051

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