ROHM
SEMICONDUCTOR

STRUCTURE   Silicon Monolithic Integrated Circuit

NAME OF PRODUCT   LED Driver control IC

TYPE   **B D 9 2 1 1 F**

FEATURE   ・   Using 20V high-voltage-withstand process
　　　　　　　　　・   1Channel Push-Pull control
　　　　　　　　　・   Current and voltage feedback is controlled
　　　　　　　　　　　　　　　by drive frequency modulation
　　　　　　　　　・   Built-in soft start circuit
　　　　　　　　　・   Built-in timer latch circuit
　　　　　　　　　・   Built-in shut down protection
　　　　　　　　　・   Built-in UVLO detection circuit
　　　　　　　　　・   Output Over Voltage Protection
　　　　　　　　　・   Built-in error signal output function
　　　　　　　　　・   Switching to current consumption save mode through STB pin
　　　　　　　　　・   Possible to control the burst by external PWM

○**Absolute Maximum Ratings (Ta=25℃)**

Item	Symbol	Rated voltage	Unit
Power supply voltage	VCC	20	V
Driver Output	N1,N2	20	V
Operating temperature	Topr	-40〜+85	℃
Storage temperature range	Tstg	-55〜+150	℃
Maximum Junction Temperature	Tjmax	+150	℃
Power Dissipation	Pd	687*	mW

* **It reduces gradually by 5.5 mW/℃ if above Ta= 25℃ (when mounting the board of 70.0mm×70.0mm×1.6mm)**

○**Recommended Operation Ranges**

Item	Symbol	Range	Unit
Power Supply	VCC	8.0〜18.0	V
PWMIN input frequency range	F_PWMIN	60〜500	Hz
Output frequency	FOUT	25〜200	kHz

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○**Electrical Characteristics (VCC=12V, Ta=25℃)**

Parameter	Symbol	Limits			Unit	Conditions
		MIN.	TYP.	MAX.		
〔〔WHOLE DEVICE〕〕						
Circuit current during operation	Icc1	－	2.3	5.0	mA	FOUT=60kHz, PWMCMP=GND
Circuit current during stand by operation	Icc2	－	0	20	μA	VSTB=0V
〔〔STAND BY CONTROL〕〕						
Stand-by voltage H	VstbH	2.0	－	VCC	V	System ON
Stand-by voltage L	VstbL	-0.3	－	0.8	V	System OFF
〔〔VCC UVLO BLOCK〕〕						
Operating voltage (VCC)	V_VCCUVP	6.17	6.50	6.83	V	
Hesteresis width (VCC UVLO)	⊿V_VCCUVP	0.37	0.50	0.63	V	
〔〔OSC BLOCK〕〕						
RT Output Voltage	VRT	1.05	1.50	1.95	V	RT=79 kΩ
〔〔PWMIN BLOCK〕〕						
PWMIN pin H level input voltage range	VPWMINH	2.0	-	5.0	V	
PWMIN pin L level input voltage range	VPWMINL	－0.3	-	0.8	V	
〔〔SOFT START BLOCK〕〕						
Set up current for soft start	ISS	1.5	2.0	2.5	uA	
Soft start end voltage	VSS_END	2.8	3.0	3.2	V	
〔〔FEED BACK BLOCK〕〕						
IS threshold voltage	VIS	1.225	1.250	1.275	V	
VS threshold voltage	VVS	1.212	1.250	1.288	V	
IS source current 1	IIS1	－	－	0.9	μA	PWMIN=2.5V
IS source current 2	IIS2	40	50	60	μA	PWMIN=0V, IS=1.0V
VS source current	IVS	－	－	0.9	μA	
IS COMP detect voltage	VISCOMP	0.606	0.625	0.644	V	
〔〔OUTPUT BLOCK〕〕						
N1 output sink resistance	Rsink_N1	1.5	3.0	6.0	Ω	
N1 output source resistance	Rsource_N1	4.5	9.0	18.0	Ω	
N2 output sink resistance	Rsink_N2	1.5	3.0	6.0	Ω	
N2 output source resistance	Rsource_N2	4.5	9.0	18.0	Ω	
MAX DUTY	MAX DUTY	43.0	45.0	47.0	%	FOUT=60kHz
N1-N2, N2-N1 OFF period	TOFF	100	200	400	ns	
Drive output frequency	FOUT	57.9	60.0	62.1	kHz	RT=79 kΩ
〔〔TIMER LATCH BLOCK〕						
CP timer latch detect voltage	VCP	1.90	2.00	2.10	V	
CP timer latch charge current	ICP	0.85	1.00	1.15	μA	
SDON latch detect voltage	VSDON	1.90	2.00	2.10	V	
SDON latch charge current	ISDON	0.85	1.00	1.15	μA	
〔〔COMP BLOCK〕〕						
COMP over voltage detect voltage	VCOMP	3.88	4.00	4.12	V	
Hysteresis width （COMP）	⊿VCOMP	0.15	0.20	0.25	V	
COMPSD over voltage detect voltage	VCOMPSD	3.88	4.00	4.12	V	
〔〔FAIL BLOCK〕〕						
FAIL ON Resistor value	RFAILL	-	100	200	Ω	

（This product is not designed to be radiation-resistant.）

REV. A

○ **External Dimensions**
     , **Marking**

Dvice Mark

BD9211F

Lot No.
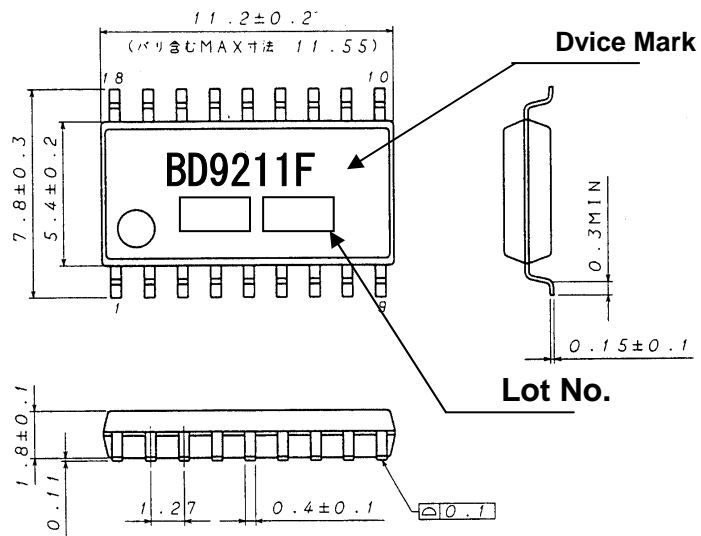
SOP18 (Unit:mm)

○ **Block Diagram**
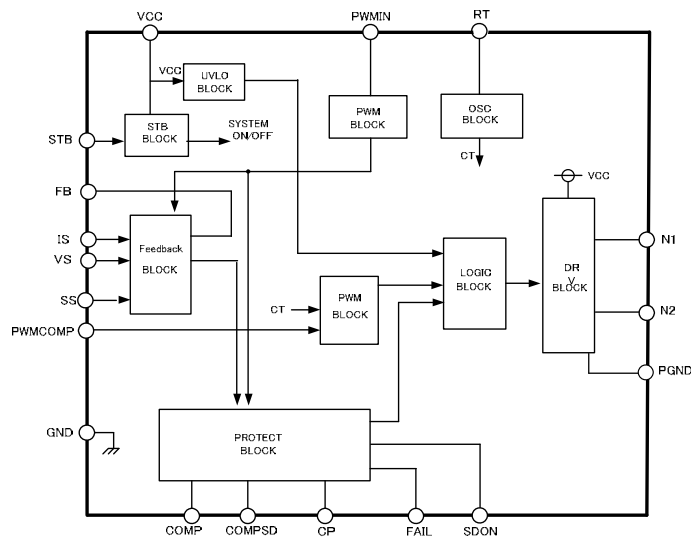
○**Pin Number, Pin Name, Pin Function**

Pin No	Pin name	Functions	Pin No	Pin name	Functions
1	VCC	Power supply pin for IC （built-in UVLO function）	10	PWMIN	PWM signal input pin for burst bright adjustment control
2	STB	Power ON/OFF control pin for IC	11	SDON	Enable pin of COMPSD inputs over voltage detection
3	GND	Signal/ground pin for internal IC	12	SS	Soft-start set up pin
4	RT	Drive frequency set up terminal.	13	FAIL	Error Indication signal Output Normal : L, Error : OPEN
5	FB	Lamp current, lamp voltage, error amp outputs	14	COMPSD	Detection pin for over voltage shut down
6	IS	Error amp input pin for lamp current feedback	15	COMP	Detection pin for over voltage and shut-down delay
7	VS	Error amp input pin for lamp voltage feedback at the opening time.	16	PGND	Power Ground for external MOSFET drive
8	PWMCMP	PWM comparator input pin which controls PWM operation during brightness adjustment.	17	N2	Output pin for external FET drive circuit (Ch. N2)
9	CP	Timer latch-setting pin	18	N1	Output pin for external FET drive circuit (Ch. N1)

○NOTE FOR USE

1. When designing the external circuit, including adequate margins for variation between external devices and IC. Use adequate margins for steady state and transient characteristics.
2. The circuit functionality is guaranteed within of ambient temperature operation range as long as it is within recommended operating range. The standard electrical characteristic values cannot be guaranteed at other voltages in the operating ranges, however the variation will be small.
3. Mounting failures, such as misdirection or miscounts, may harm the device.
4. A strong electromagnetic field may cause the IC to malfunction.
5. The GND pin should be the location within ±0.3V compared with the PGND pin.
6. If the voltage between VCC and I/O pins or GND and I/O pins is in opposite from the normal potential difference, unusual current flow into pins may occur which can destroy the IC. To avoid such occurrence it is recommended to place protection diodes for prevention against backward current flow.
7. BD9211F incorporate a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation of the thermal shutdown circuit is assumed.
8. Absolute maximum ratings are those values that, if exceeded, may cause the life of a device to become significantly shortened. Moreover, the exact failure mode caused by short or open is not defined. Physical countermeasures, such as a fuse, need to be considered when using a device beyond its maximum ratings.
9. About the external FET, the parasitic Capacitor may cause the gate voltage to change, when the drain voltage is switching. Make sure to leave adequate margin for this IC variation.
10. By STB voltage, BD9211F are changed to 2 states. Therefore, do not input STB pin voltage between one state and the other state (0.8～2.0V).
11. The pin connected a connector need to connect to the resistor for electrical surge destruction.
12. This IC is a monolithic IC which (as shown is Fig.4)has P$^+$ substrate and between the various pins. A P-N junction is formed from this P layer of each pin. For example, the relation between each potential is as follows,
   ○(When GND > PinB and GND > PinA, the P-N junction operates as a parasitic diode.)
   ○(When PinB > GND > PinA, the P-N junction operates as a parasitic transistor.)

Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits as well as operation faults and physical damage. Accordingly you must not use methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin
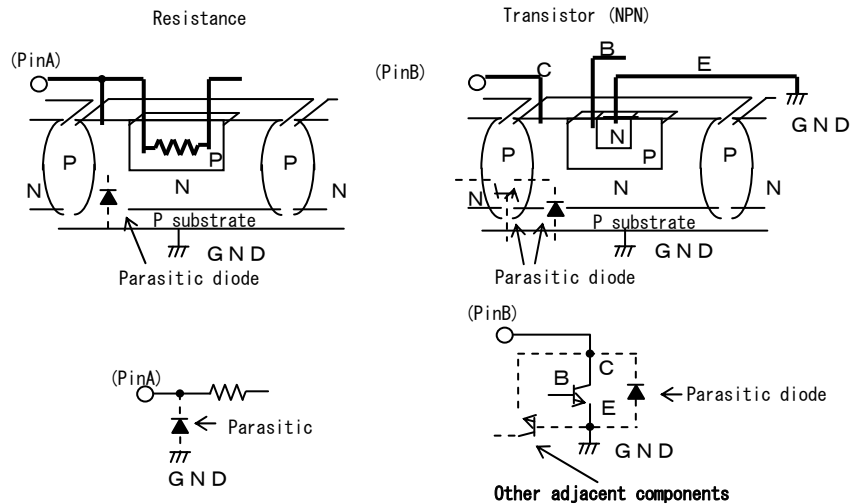

Fig.4. Simplified structure of a Bipolar IC

Notes

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