
HM674100H Series

1,048,576-word $\times$ 4-bit High Speed Static Random Access Memory

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ADE-203-
Rev. 0.0
Dec. 1, 1995

Features

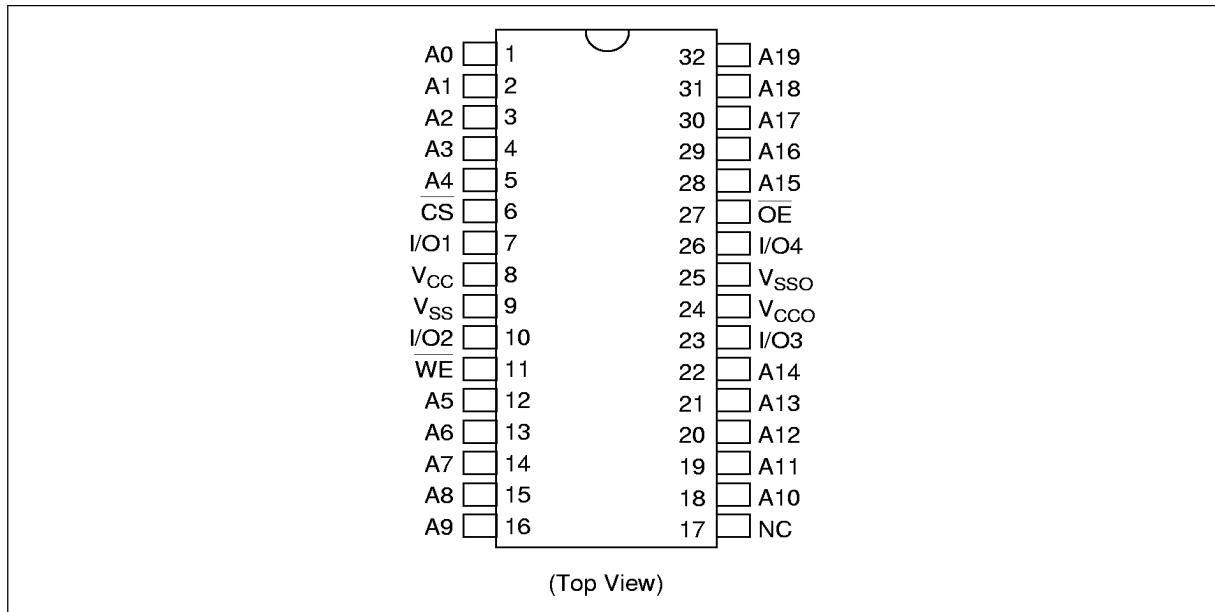
- 1,048,576-word $\times$ 4-bit organization.
- Directly TTL compatible input and output.
- +5 V Single supply.
- Completely static memory.
- No clock or timing strobe required.
- Super fast access time: 15/20/25 ns (max).
- Revolutionary pin arrangement.

Ordering Information

Type No.	Access Time	Package
HM674100HJP-15	15 ns	400 mil 32 pin plastic SOJ (CP-32DB)
HM674100HJP-20	20 ns	
HM674100HJP-25	25 ns	

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Pin Arrangement



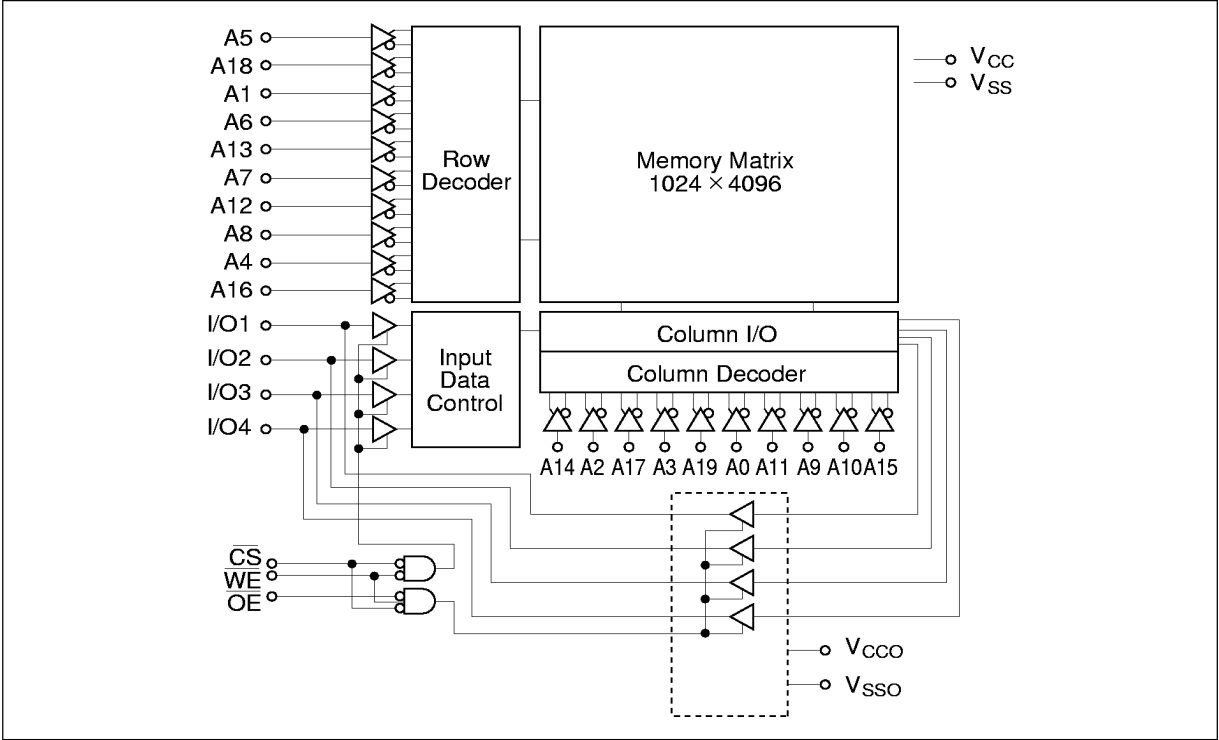
Pin Description

Pin Name	Function
A0 to A19	Address input
I/O1 to I/O4	input/output
WE	Write enable
CS	Chip select
OE	Output enable
V _{CC}	+5 V Power supply
V _{CCO}	Output buffer power supply
V _{SSO}	Output buffer ground
V _{SS}	Ground
NC	Not connect

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Block Diagram



Function Table

Input						
CS	WE	OE	Mode	I/O Pin	V _{CC} Current	Ref. Cycle
H	X	X	Not selected	High-Z	I _{SB} , I _{SB1}	—
L	H	H	Output disabled	High-Z	I _{CC} , I _{CC1}	—
L	H	L	Read	Data Out	I _{CC} , I _{CC1}	Read Cycle (1), (2), (3)
L	L	H	Write	Data In	I _{CC} , I _{CC1}	Write Cycle (1), (2), (3), (4)
L	L	L	Write	Data In	I _{CC} , I _{CC1}	Write Cycle (5), (6)

Note: X: H or L

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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage ^{*1}	V_{CC}	-0.5 to +7.0	V
Voltage on any pin relative to V_{SS} ^{*1}	V_T	-0.5 to $V_{CC} + 0.5$	V
Power dissipation	P_T	1.0/1.5 ^{*2}	W
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range (with bias)	T_{stg} (Bias)	-10 to +85	°C
Storage temperature range	T_{stg}	-55 to +125	°C

Notes: 1 With respect to $V_{SS} = V_{SS0}$

- 2 $P_T = 1.5$ W is guaranteed under the minimum air flow exceeding 500 linear feet per minute. Under the DC and AC specifications shown in the Tables, this device is tested under the minimum transverse air flow exceeding 500 linear feet per minute.

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}, V_{CC0}	4.5	5.0	5.5	V
	V_{SS}, V_{SS0}	0.0	0.0	0.0	V
Input high voltage	V_{IH}	2.2	—	$V_{CC} + 0.5$	V
Input low voltage	V_{IL}	-0.5	—	0.8	V

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DC Characteristics ($V_{CC} = V_{CCO} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = V_{SSO} = 0 \text{ V}$, $T_a = 0 \text{ to } +70^\circ\text{C}$)

HM674100H									
		-15		-20		-25			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Input leakage current	$ I_{LI} $	—	2	—	2	—	2	μA	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 0 \text{ V to } V_{CC}$
Output leakage current	$ I_{LO} $	—	10	—	10	—	10	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$, $\overline{WE} = V_{IL}$, $V_{IO} = 0 \text{ V to } V_{CC}$
Operating power supply current	I_{CC}	—	120	—	120	—	120	mA	$\overline{CS} = V_{IL}$, $I_{IO} = 0 \text{ mA}$
Average operating current	I_{CC1}	—	220	—	200	—	160	mA	min cycle, $I_{IO} = 0 \text{ mA}$
Standby power supply current	I_{SB}	—	100	—	80	—	60	mA	$\overline{CS} = V_{IH}$, $V_{IN} = V_{IH}$ or V_{IL}
	I_{SB1}	—	10	—	10	—	10	mA	$\overline{CS} \geq V_{CC} - 0.2 \text{ V}$ $V_{IN} \leq 0.2 \text{ V}$ or $V_{IN} \geq V_{CC} - 0.2 \text{ V}$
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	V	$I_{OL} = 8 \text{ mA}$
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	V	$I_{OH} = -4 \text{ mA}$

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1 \text{ MHz}$)

Parameter	Symbol	Max	Unit	Test Conditions
Input capacitance	C_{IN}^{*1}	6	pF	$V_{IN} = 0 \text{ V}$
Input/Output capacitance	C_{IO}^{*1}	10	pF	$V_{IO} = 0 \text{ V}$

Note: 1. This parameter is sampled and not 100% tested.

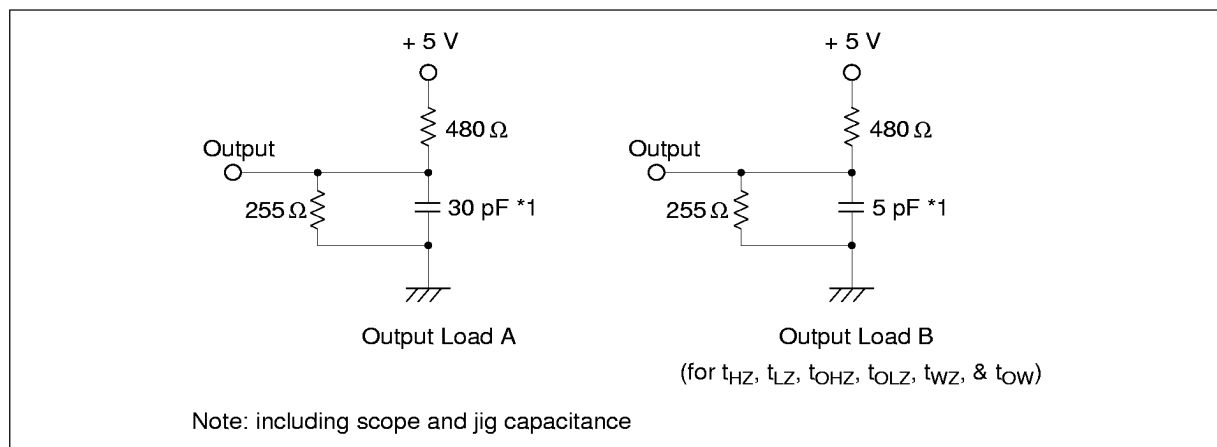
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AC Characteristics ($V_{CC} = V_{CCO} = 5\text{ V} \pm 10\%$, $V_{SS} = V_{SSO} = 0\text{ V}$, $T_a = 0\text{ to } +70^\circ\text{C}$, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 1.5V
- Input rise and fall time: 4 ns
- Output reference levels: 1.5 V
- Output Load: See figure



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Read Cycle

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		-15		-20		-25		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Read cycle time	t_{RC}	15	—	20	—	25	—	ns
Address access time	t_{AA}	—	15	—	20	—	25	ns
Chip select access time	t_{ACS}	—	15	—	20	—	25	ns
Chip selection to output in low-Z	$t_{LZ}^{*1,*2}$	5	—	5	—	5	—	ns
Output enable to output Valid	t_{OE}	—	8	—	10	—	15	ns
Output enable to output in low-Z	$t_{OLZ}^{*1,*2}$	2	—	2	—	2	—	ns
Chip deselection to output in high-Z	$t_{HZ}^{*1,*2}$	0	7	0	8	0	15	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns

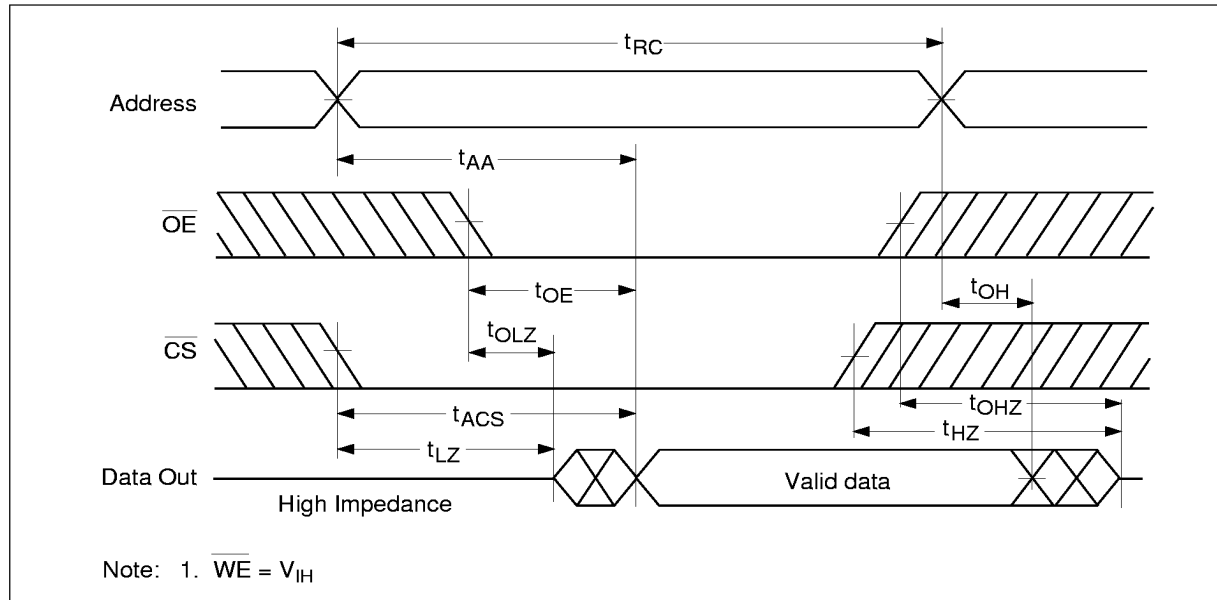
Notes: 1. This parameter is sampled and not 100% tested.

2. Transition is measured ± 200 mV from steady state voltage with specified loading in Load (B).

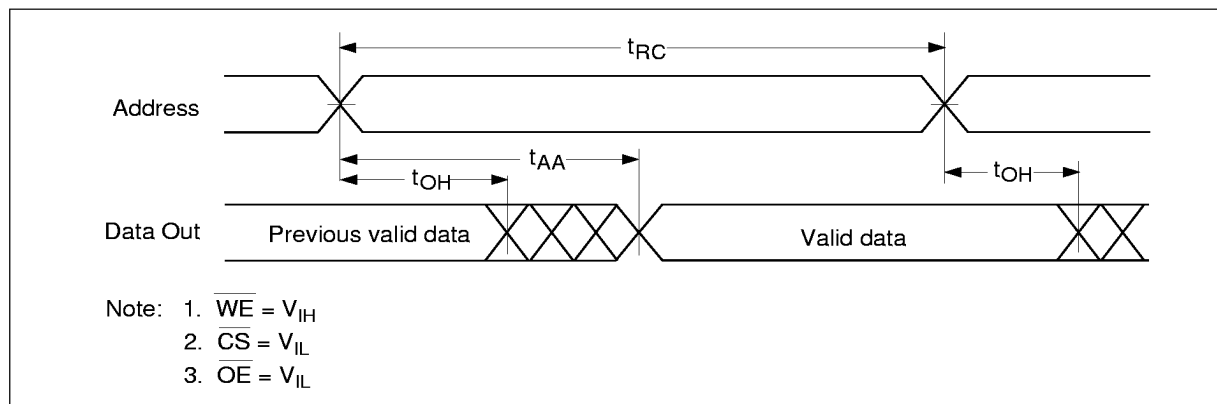
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Timing Waveforms

Read Cycle-1

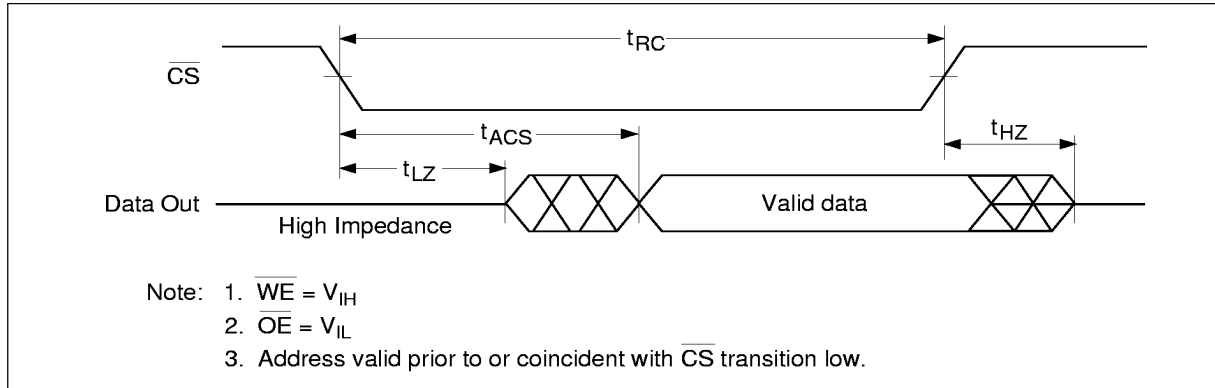


Read Cycle-2



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Read Cycle-3



Write Cycle

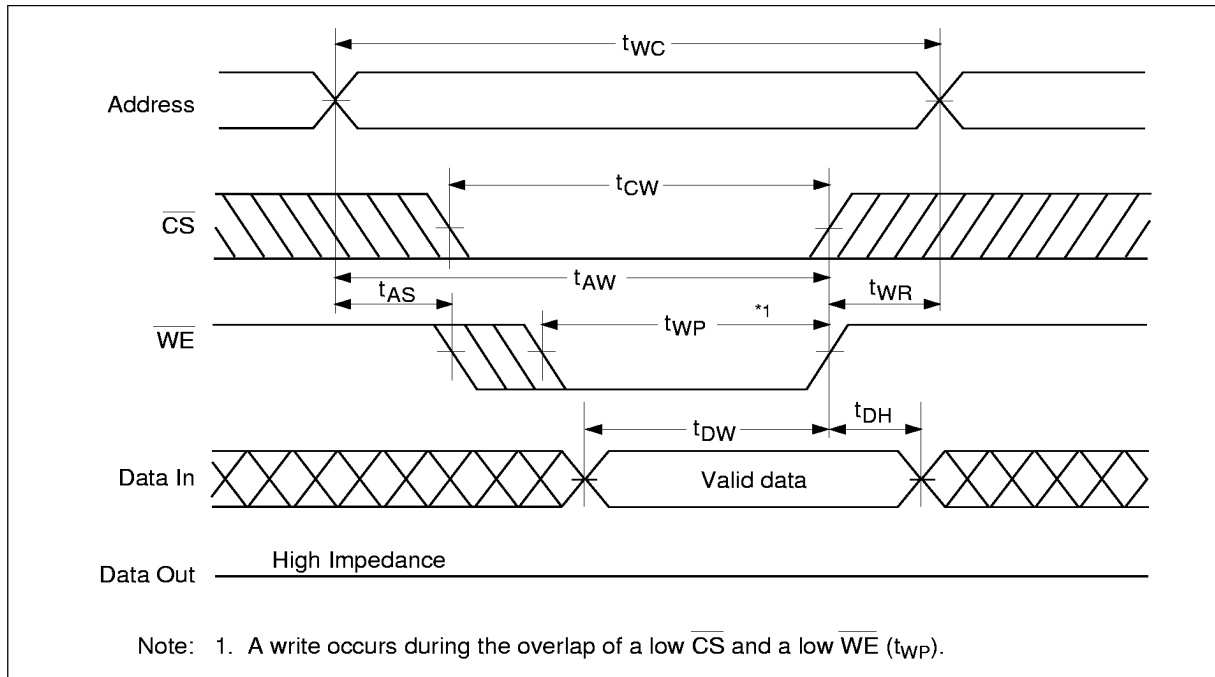
HM674100H								
		-15		-20		-25		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Write cycle time	t_{WC}^{*1}	15	—	20	—	25	—	ns
Chip selection to end of write	t_{CW}	12	—	15	—	17	—	ns
Address valid to end of write	t_{AW}	12	—	15	—	17	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	12	—	15	—	17	—	ns
Write recovery time	t_{WR}	3	—	3	—	3	—	ns
Data valid to end of write	t_{DW}	8	—	10	—	15	—	ns
Data hold time	t_{DH}	0	—	0	—	0	—	ns
Write enable to output in high Z	$t_{WZ}^{*2,*3}$	0	7	0	8	0	12	ns
Output disable to output in high Z	$t_{OHZ}^{*2,*3}$	0	7	0	8	0	10	ns
Output active from end of write	$t_{OW}^{*2,*3}$	2	—	2	—	2	—	ns

Notes:

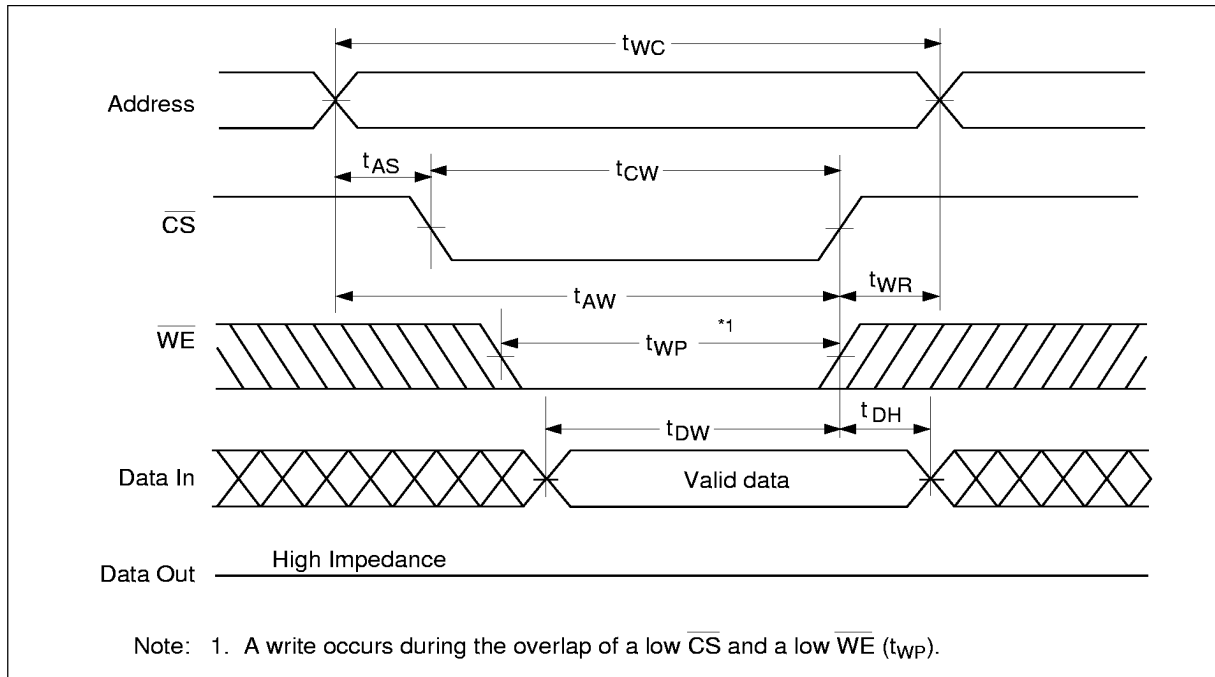
1. All write cycle timings are referred from the last valid address to the first transitioning address.
2. This parameter is sampled and not 100% tested.
3. Transition is measured ± 200 mV from steady state voltage with specified loading in Load (B).

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Write Cycle-1 ($\overline{\text{OE}} = \text{H}$, $\overline{\text{WE}}$ Controlled)

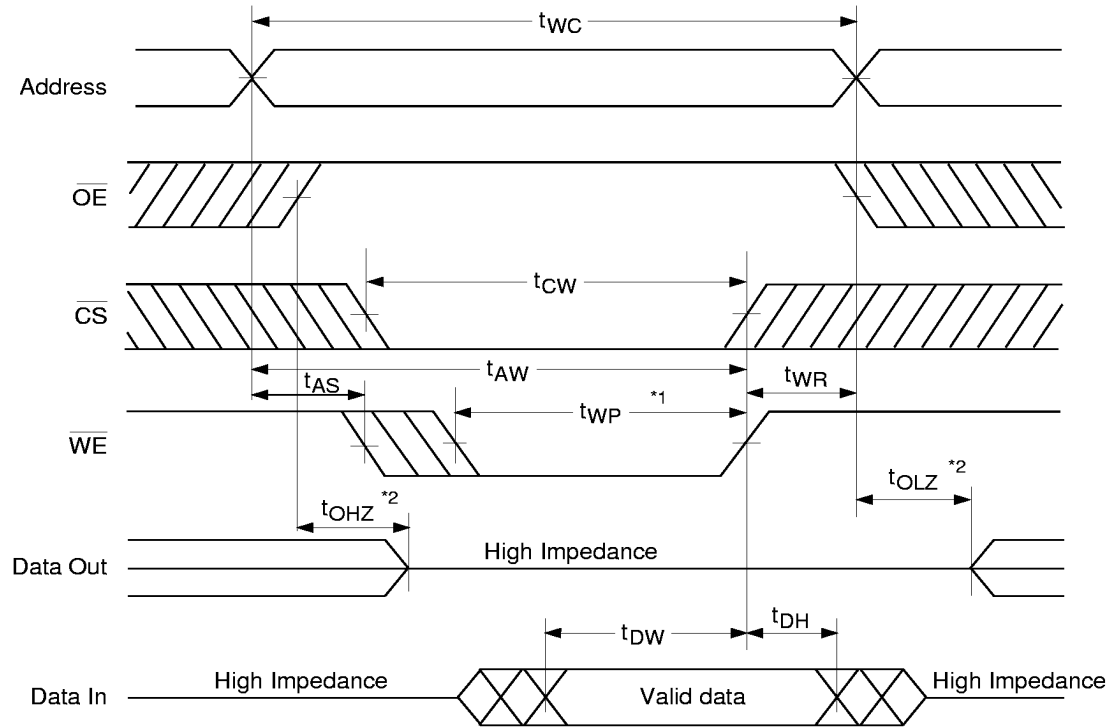


Write Cycle-2 ($\overline{OE} = H$, $\overline{CS}$ Controlled)



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Write Cycle-3 ($\overline{\text{OE}}$ = Clocked, $\overline{\text{WE}}$ Controlled)

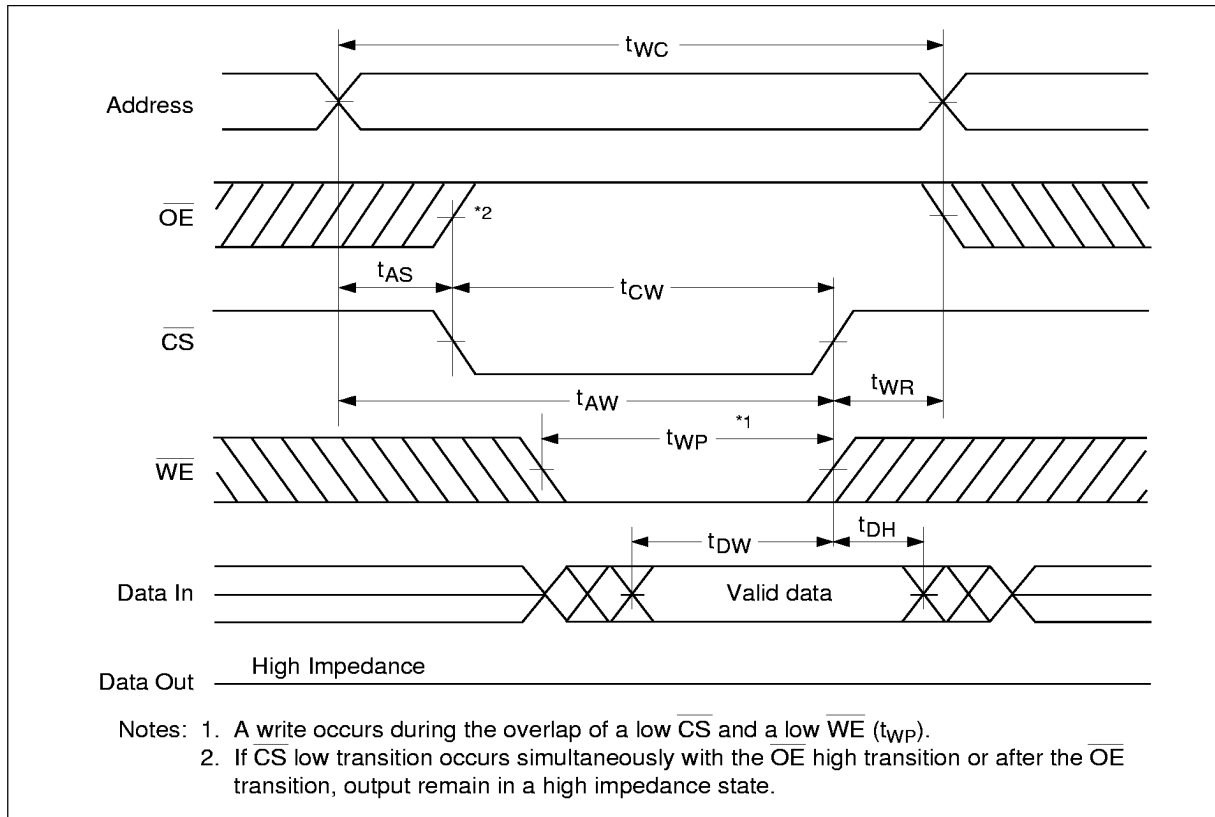


- Notes: 1. A write occurs during the overlap of a low $\overline{\text{CS}}$ and a low $\overline{\text{WE}}$ (t_{WP}).
 2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

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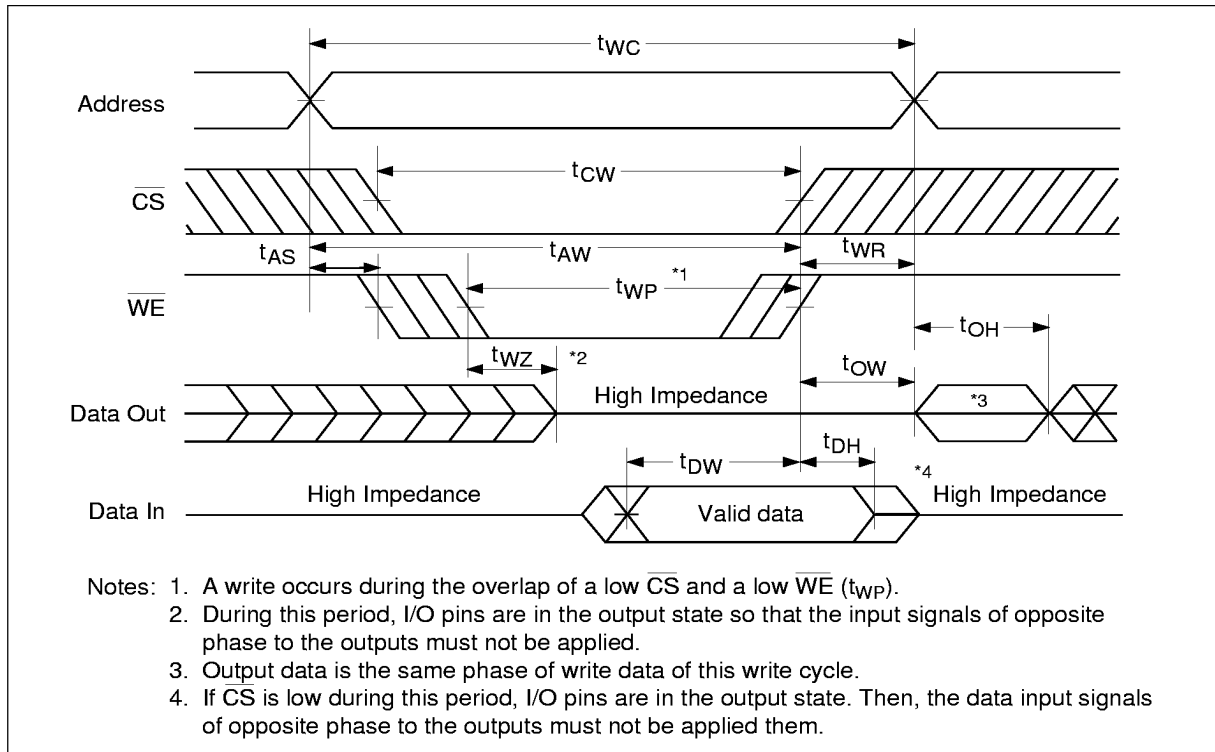
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Write Cycle-4 ($\overline{\text{OE}}$ = Clocked, $\overline{\text{CS}}$ Controlled)

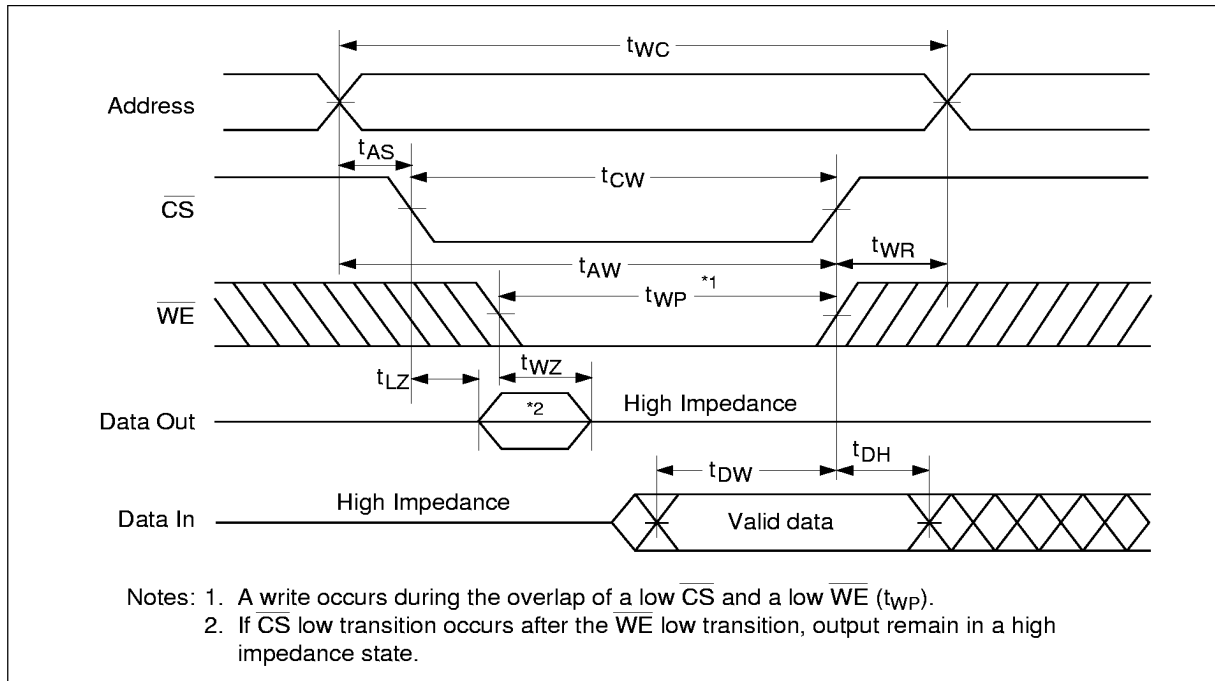


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Write Cycle-5 ($\overline{OE} = L$, $\overline{WE}$ Controlled)



Write Cycle-6 ($\overline{OE} = L$, $\overline{CS}$ Controlled)

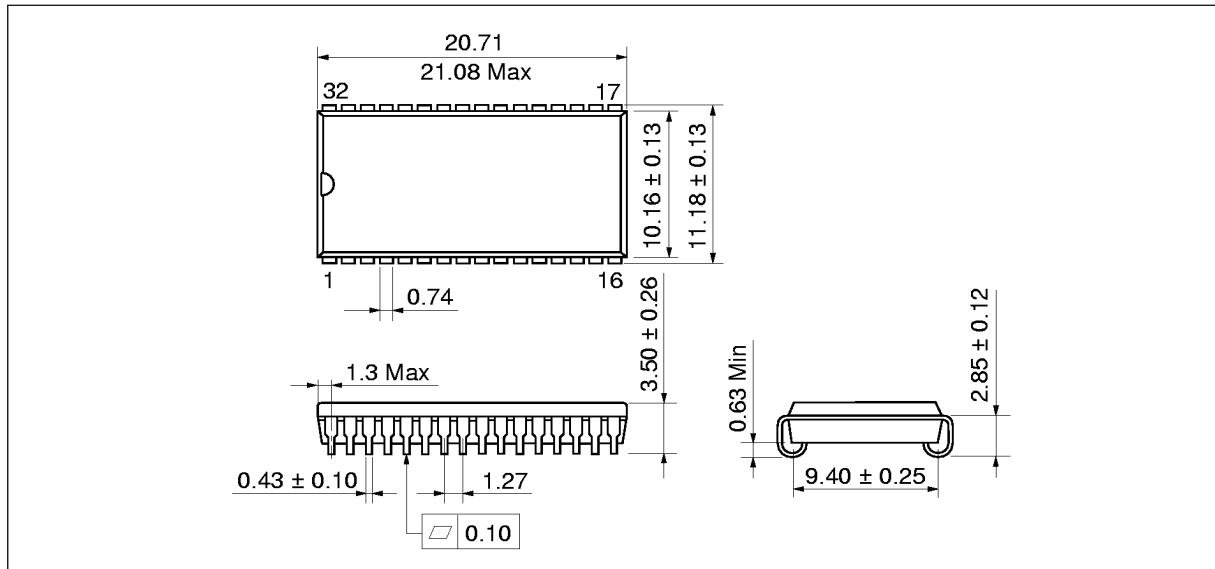


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Package Dimension

HM674100HJP Series (CP-32DB)

Unit: mm



HM674100HJP -15, -20, -25 400 mil 32 pin plastic SOJ (CP-32DB) — Mechanical

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